INTEGRATED CIRCUITS, SILICON MONOLITHIC, CMOS, CELL-BASED ARRAY (ASIC) WITH OPTIONAL ANALOG BLOCKS

BASED ON TYPE ATMX150RHA

ESCC Detail Specification No. 9202/083

Issue 4	May 2021

Document Custodian: European Space Agency – see https://escies.org

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DOCUMENTATION CHANGE NOTICE

(Refer to https://escies.org for ESCC DCR content)

DCR No.	CHANGE DESCRIPTION
1419	Specification upissued to incorporate changes per DCR.

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1 GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics and test and inspection data for the component type variants and/or the range of components specified below. It supplements the requirements of, and shall be read in conjunction with, the ESCC Generic Specification listed under Applicable Documents.

1.2 APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:

(a) ESCC Generic Specification No. 9000.
(b) MIL-STD-883, Test Methods and Procedures for Microelectronics.

1.3 TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESCC Basic Specification No. 21300 shall apply.

1.4 THE ESCC COMPONENT NUMBER AND COMPONENT TYPE VARIANTS

1.4.1 The ESCC Component Number

The ESCC Component Number shall be constituted as follows:

Example: 920208301RXYZ

- Detail Specification Reference: 9202083
- Component Type Variant Number: 01 (as required, and three digits when necessary)
- Total Dose Radiation Level Letter: R (as required)
- Manufacturer Specific ASIC Identification: XYZ (as applicable, where XYZ is an individual 3-character code allocated by the Manufacturer to a specific ASIC design)

1.4.2 Component Type Variants

The component type variants applicable to this specification are as follows:

Variant Number	Based on Type	Typical Equivalent NAND2 Gate Count	Interface Circuitry Supply Voltage (Note 1)	Case	Terminal Material and Finish	Weight max g	Total Dose Radiation Level Letter (Note 5)
75	ATMX150RHA_216	1M	3.3V	FS CQFP-256	D2 (Note 2)	20	R [100kRAD(Si)]
76	ATMX150RHA_216	1M	3.3V	FS CQFP-132	D2 (Note 2)	8	R [100kRAD(Si)]
77	ATMX150RHA_324	2.2M	3.3V	FS CQFP-352	D2 (Note 2)	31	R [100kRAD(Si)]
78	ATMX150RHA_324	2.2M	3.3V	FS CQFP-256	D2 (Note 2)	20	R [100kRAD(Si)]
79	ATMX150RHA_324	2.2M	3.3V	FS CQFP-132	D2 (Note 2)	8	R [100kRAD(Si)]

Variant Number	Based on Type	Typical Equivalent NAND2 Gate Count	Interface Circuitry Supply Voltage (Note 1)	Case	Terminal Material and Finish	Weight max g	Total Dose Radiation Level Letter (Note 5)
80	ATMX150RHA_404	3.5M	3.3V	FS CQFP-352	D2 (Note 2)	31	R [100kRAD(Si)]
81	ATMX150RHA_404	3.5M	3.3V	FS CQFP-256	D2 (Note 2)	30	R [100kRAD(Si)]
82	ATMX150RHA_404	3.5M	3.3V	FS CQFP-132	D2 (Note 2)	8	R [100kRAD(Si)]
83	ATMX150RHA_404	3.5M	3.3V	FS CLGA-472	(Note 3)	11	R [100kRAD(Si)]
84	ATMX150RHA_404	3.5M	3.3V	FS CCGA-472	R (Note 2)	12	R [100kRAD(Si)]
85	ATMX150RHA_504	5.5M	3.3V	FS CQFP-352	D2 (Note 2)	31	R [100kRAD(Si)]
86	ATMX150RHA_504	5.5M	3.3V	FS CQFP-256	D2 (Note 2)	20	R [100kRAD(Si)]
87	ATMX150RHA_504	5.5M	3.3V	FS CLGA-625	(Note 3)	12	R [100kRAD(Si)]
88	ATMX150RHA_504	5.5M	3.3V	FS CLGA-472	(Note 3)	11	R [100kRAD(Si)]
89	ATMX150RHA_504	5.5M	3.3V	FS CCGA-625	R (Note 2)	13	R [100kRAD(Si)]
90	ATMX150RHA_504	5.5M	3.3V	FS CCGA-472	R (Note 2)	12	R [100kRAD(Si)]
91	ATMX150RHA_544	6.5M	3.3V	FS CQFP-352	D2 (Note 2)	31	R [100kRAD(Si)]
92	ATMX150RHA_544	6.5M	3.3V	FS CQFP-256	D2 (Note 2)	20	R [100kRAD(Si)]
93	ATMX150RHA_544	6.5M	3.3V	FS CLGA-625	(Note 3)	12	R [100kRAD(Si)]
94	ATMX150RHA_544	6.5M	3.3V	FS CLGA-472	(Note 3)	11	R [100kRAD(Si)]
95	ATMX150RHA_544	6.5M	3.3V	FS CCGA-625	R (Note 2)	13	R [100kRAD(Si)]
96	ATMX150RHA_544	6.5M	3.3V	FS CCGA-472	R (Note 2)	12	R [100kRAD(Si)]
97	ATMX150RHA_604	7.5M	3.3V	FS CQFP-352	D2 (Note 2)	31	R [100kRAD(Si)]
98	ATMX150RHA_604	7.5M	3.3V	FS CQFP-256	D2 (Note 2)	20	R [100kRAD(Si)]
99	ATMX150RHA_604	7.5M	3.3V	FS CLGA-896	(Note 3)	13	R [100kRAD(Si)]
100	ATMX150RHA_604	7.5M	3.3V	FS CLGA-625	(Note 3)	12	R [100kRAD(Si)]
101	ATMX150RHA_604	7.5M	3.3V	FS CLGA-472	(Note 3)	11	R [100kRAD(Si)]

Variant Number	Based on Type	Typical Equivalent NAND2 Gate Count	Interface Circuitry Supply Voltage (Note 1)	Case	Terminal Material and Finish	Weight max g	Total Dose Radiation Level Letter (Note 5)
102	ATMX150RHA_604	7.5M	3.3V	FS CCGA-896	R (Note 2)	14	R [100kRAD(Si)]
103	ATMX150RHA_604	7.5M	3.3V	FS CCGA-625	R (Note 2)	13	R [100kRAD(Si)]
104	ATMX150RHA_604	7.5M	3.3V	FS CCGA-472	R (Note 2)	12	R [100kRAD(Si)]
105	ATMX150RHA_644	8.7M	3.3V	FS CQFP-352	D2 (Note 2)	31	R [100kRAD(Si)]
106	ATMX150RHA_644	8.7M	3.3V	FS CQFP-256	D2 (Note 2)	20	R [100kRAD(Si)]
107	ATMX150RHA_644	8.7M	3.3V	FS CLGA-896	(Note 3)	13	R [100kRAD(Si)]
108	ATMX150RHA_644	8.7M	3.3V	FS CLGA-625	(Note 3)	12	R [100kRAD(Si)]
109	ATMX150RHA_644	8.7M	3.3V	FS CLGA-472	(Note 3)	11	R [100kRAD(Si)]
110	ATMX150RHA_644	8.7M	3.3V	FS CCGA-896	R (Note 2)	14	R [100kRAD(Si)]
111	ATMX150RHA_644	8.7M	3.3V	FS CCGA-625	R (Note 2)	13	R [100kRAD(Si)]
112	ATMX150RHA_644	8.7M	3.3V	FS CCGA-472	R (Note 2)	12	R [100kRAD(Si)]
113	ATMX150RHA_704	10.4M	3.3V	FS CQFP-352	D2 (Note 2)	31	R [100kRAD(Si)]
114	ATMX150RHA_704	10.4M	3.3V	FS CLGA-896	(Note 3)	13	R [100kRAD(Si)]
115	ATMX150RHA_704	10.4M	3.3V	FS CLGA-625	(Note 3)	12	R [100kRAD(Si)]
116	ATMX150RHA_704	10.4M	3.3V	FS CLGA-472	(Note 3)	11	R [100kRAD(Si)]
117	ATMX150RHA_704	10.4M	3.3V	FS CCGA-896	R (Note 2)	14	R [100kRAD(Si)]
118	ATMX150RHA_704	10.4M	3.3V	FS CCGA-625	R (Note 2)	13	R [100kRAD(Si)]
119	ATMX150RHA_704	10.4M	3.3V	FS CCGA-472	R (Note 2)	12	R [100kRAD(Si)]
120	ATMX150RHA_216	1M	2.5V	FS CQFP-256	D2 (Note 2)	20	R [100kRAD(Si)]
121	ATMX150RHA_216	1M	2.5V	FS CQFP-132	D2 (Note 2)	8	R [100kRAD(Si)]
122	ATMX150RHA_324	2.2M	2.5V	FS CQFP-352	D2 (Note 2)	31	R [100kRAD(Si)]
123	ATMX150RHA_324	2.2M	2.5V	FS CQFP-256	D2 (Note 2)	20	R [100kRAD(Si)]

Variant Number	Based on Type	Typical Equivalent NAND2 Gate Count	Interface Circuitry Supply Voltage (Note 1)	Case	Terminal Material and Finish	Weight max g	Total Dose Radiation Level Letter (Note 5)
124	ATMX150RHA_324	2.2M	2.5V	FS CQFP-132	D2 (Note 2)	8	R [100kRAD(Si)]
125	ATMX150RHA_404	3.5M	2.5V	FS CQFP-352	D2 (Note 2)	31	R [100kRAD(Si)]
126	ATMX150RHA_404	3.5M	2.5V	FS CQFP-256	D2 (Note 2)	30	R [100kRAD(Si)]
127	ATMX150RHA_404	3.5M	2.5V	FS CQFP-132	D2 (Note 2)	8	R [100kRAD(Si)]
128	ATMX150RHA_404	3.5M	2.5V	FS CLGA-472	(Note 3)	11	R [100kRAD(Si)]
129	ATMX150RHA_404	3.5M	2.5V	FS CCGA-472	R (Note 2)	12	R [100kRAD(Si)]
130	ATMX150RHA_504	5.5M	2.5V	FS CQFP-352	D2 (Note 2)	31	R [100kRAD(Si)]
131	ATMX150RHA_504	5.5M	2.5V	FS CQFP-256	D2 (Note 2)	20	R [100kRAD(Si)]
132	ATMX150RHA_504	5.5M	2.5V	FS CLGA-625	(Note 3)	12	R [100kRAD(Si)]
133	ATMX150RHA_504	5.5M	2.5V	FS CLGA-472	(Note 3)	11	R [100kRAD(Si)]
134	ATMX150RHA_504	5.5M	2.5V	FS CCGA-625	R (Note 2)	13	R [100kRAD(Si)]
135	ATMX150RHA_504	5.5M	2.5V	FS CCGA-472	R (Note 2)	12	R [100kRAD(Si)]
136	ATMX150RHA_544	6.5M	2.5V	FS CQFP-352	D2 (Note 2)	31	R [100kRAD(Si)]
137	ATMX150RHA_544	6.5M	2.5V	FS CQFP-256	D2 (Note 2)	20	R [100kRAD(Si)]
138	ATMX150RHA_544	6.5M	2.5V	FS CLGA-625	(Note 3)	12	R [100kRAD(Si)]
139	ATMX150RHA_544	6.5M	2.5V	FS CLGA-472	(Note 3)	11	R [100kRAD(Si)]
140	ATMX150RHA_544	6.5M	2.5V	FS CCGA-625	R (Note 2)	13	R [100kRAD(Si)]
141	ATMX150RHA_544	6.5M	2.5V	FS CCGA-472	R (Note 2)	12	R [100kRAD(Si)]
142	ATMX150RHA_604	7.5M	2.5V	FS CQFP-352	D2 (Note 2)	31	R [100kRAD(Si)]
143	ATMX150RHA_604	7.5M	2.5V	FS CQFP-256	D2 (Note 2)	20	R [100kRAD(Si)]
144	ATMX150RHA_604	7.5M	2.5V	FS CLGA-896	(Note 3)	13	R [100kRAD(Si)]
145	ATMX150RHA_604	7.5M	2.5V	FS CLGA-625	(Note 3)	12	R [100kRAD(Si)]

Variant Number	Based on Type	Typical Equivalent NAND2 Gate Count	Interface Circuitry Supply Voltage (Note 1)	Case	Terminal Material and Finish	Weight max g	Total Dose Radiation Level Letter (Note 5)
146	ATMX150RHA_604	7.5M	2.5V	FS CLGA-472	(Note 3)	11	R [100kRAD(Si)]
147	ATMX150RHA_604	7.5M	2.5V	FS CCGA-896	R (Note 2)	14	R [100kRAD(Si)]
148	ATMX150RHA_604	7.5M	2.5V	FS CCGA-625	R (Note 2)	13	R [100kRAD(Si)]
149	ATMX150RHA_604	7.5M	2.5V	FS CCGA-472	R (Note 2)	12	R [100kRAD(Si)]
150	ATMX150RHA_644	8.7M	2.5V	FS CQFP-352	D2 (Note 2)	31	R [100kRAD(Si)]
151	ATMX150RHA_644	8.7M	2.5V	FS CQFP-256	D2 (Note 2)	20	R [100kRAD(Si)]
152	ATMX150RHA_644	8.7M	2.5V	FS CLGA-896	(Note 3)	13	R [100kRAD(Si)]
153	ATMX150RHA_644	8.7M	2.5V	FS CLGA-625	(Note 3)	12	R [100kRAD(Si)]
154	ATMX150RHA_644	8.7M	2.5V	FS CLGA-472	(Note 3)	11	R [100kRAD(Si)]
155	ATMX150RHA_644	8.7M	2.5V	FS CCGA-896	R (Note 2)	14	R [100kRAD(Si)]
156	ATMX150RHA_644	8.7M	2.5V	FS CCGA-625	R (Note 2)	13	R [100kRAD(Si)]
157	ATMX150RHA_644	8.7M	2.5V	FS CCGA-472	R (Note 2)	12	R [100kRAD(Si)]
158	ATMX150RHA_704	10.4M	2.5V	FS CQFP-352	D2 (Note 2)	31	R [100kRAD(Si)]
159	ATMX150RHA_704	10.4M	2.5V	FS CLGA-896	(Note 3)	13	R [100kRAD(Si)]
160	ATMX150RHA_704	10.4M	2.5V	FS CLGA-625	(Note 3)	12	R [100kRAD(Si)]
161	ATMX150RHA_704	10.4M	2.5V	FS CLGA-472	(Note 3)	11	R [100kRAD(Si)]
162	ATMX150RHA_704	10.4M	2.5V	FS CCGA-896	R (Note 2)	14	R [100kRAD(Si)]
163	ATMX150RHA_704	10.4M	2.5V	FS CCGA-625	R (Note 2)	13	R [100kRAD(Si)]
164	ATMX150RHA_704	10.4M	2.5V	FS CCGA-472	R (Note 2)	12	R [100kRAD(Si)]

NOTES:

1. The component is specified for operation at a nominal interface circuitry single supply voltage V_{CC} = 3.3V or 2.5V (See Para. 2.3.1 Room Temperature Electrical Measurements).
2. The terminal material and finish shall be in accordance with the requirements of ESCC Basic Specification No. 23500.

3. The terminal material shall be tungsten and the finish shall be 0.03µm to 0.1µm gold plating over 3.2µm minimum nickel underplating.
4. The terminal material shall be tungsten and the finish shall be 2.5µm minimum gold plating over 3.2µm minimum nickel underplating.
5. The total dose radiation level letter shall be as defined in ESCC Basic Specification No. 22900. If an alternative radiation test level is specified in the Purchase Order the letter shall be changed accordingly.

1.4.3 Manufacturer Specific ASIC Identification

An ASIC Sheet shall be produced by the Manufacturer, after negotiation with the Orderer, that, as a minimum, specifies all the requirements unique to the specific ASIC design that are identified herein as being specified in the ASIC Sheet. The ASIC Sheet shall be held under configuration control by the Manufacturer. For identification and traceability purposes the Manufacturer shall allocate a unique Manufacturer Specific ASIC Identification to the ASIC Sheet and the specific ASIC design as specified in Para. 1.4.1.

1.5 MAXIMUM RATINGS

The maximum ratings shall not be exceeded at any time during use or storage. Functional performance for extended periods at the maximum ratings may adversely affect device reliability.

Maximum ratings shall only be exceeded during testing to the extent specified in this specification and when stipulated in Test Methods and Procedures of the ESCC Generic Specification.

Characteristics	Symbols	Maximum Ratings	Units	Remarks
Supply Voltage	V_{DD} V_{CC}	-0.3 to 2 -0.3 to 4	V	Notes 1, 2, 3 Notes 1, 3, 4
Input Voltage	V_{IN}	-0.3 to 4	V	Notes 3, 4
Input Current	I_{IN}	 ±60 ±10	mA	 Power Input Pins Signal Input Pins
Device Power Dissipation (Continuous)	P_D	See ASIC Sheet	W	
Supply Current	I_{CCop}	See ASIC Sheet	mA	
Operating Temperature Range	T_{op}	-55 to +125	°C	Note 1 T_{amb}
Storage Temperature Range	T_{stg}	-65 to +150	°C	
Junction Temperature	T_j	+175	°C	
Thermal Resistance Junction to Case	$R_{th(j-c)}$	See ASIC Sheet	°C/W	
Soldering Temperature FS CQFP cases FS CCGA and FS CLGA cases	T_{sol}	 +300 +220	°C	 Note 5 Note 6

NOTES:

1. The following operating conditions also apply. Device performance beyond these operating conditions is not guaranteed:

Characteristics	Symbols	Maximum Ratings	Units	Remarks
Supply Voltage	V_{DD} V_{CC33} V_{CC25}	1.65 to 1.95 3 to 3.6 2.25 to 2.75	V	Notes 1, 2, 3 Notes 1, 3, 4, 7 Notes 1, 3, 4, 7
Operating Temperature Range	T_{op}	-55 to +125	°C	Note 1 T_{amb}

2. Applicable to the core circuitry.
3. With reference to V_{SS} = 0V.
4. Applicable to the interface circuitry.
5. Duration 10 seconds maximum at a distance of not less than 1.6mm from the device body and the same terminal shall not be resoldered until 3 minutes have elapsed.
6. During reflow.
7. Applicable to 3.3V and 2.5 V I/O's respectively.

1.6 HANDLING PRECAUTIONS

These devices are susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacture, testing, packaging, shipment and any handling.

These components are categorised as Class 2 per ESCC Basic Specification No. 23800 with a Minimum Critical Path Failure Voltage of 1000 Volts.

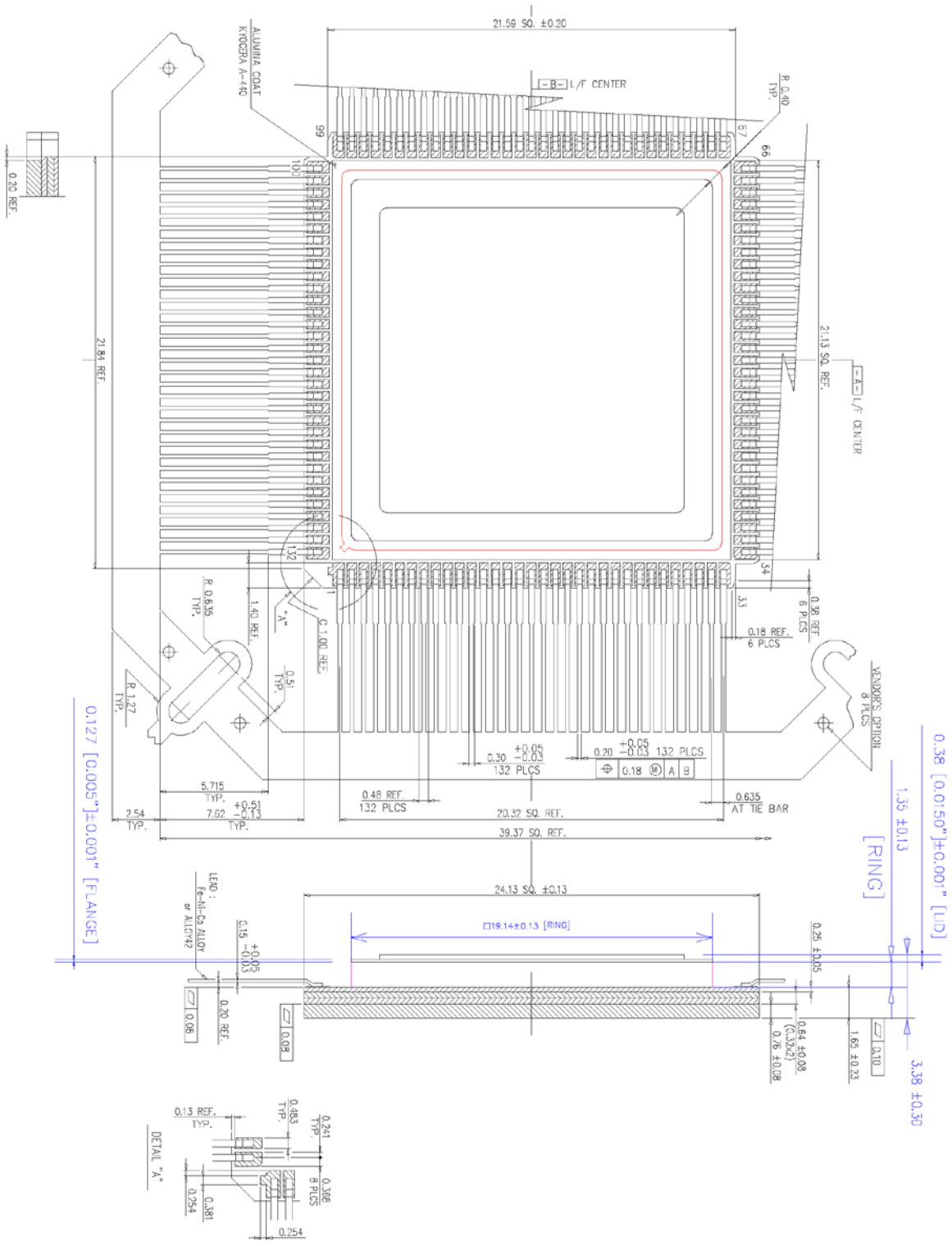
1.7 IP LIBRARY INFORMATION

The following IP library elements are available within the analog part of the ASIC:

- A large portfolio of flip-flops, latches and combinatory cells
- Compiled memory (SRAM, ROM, DPRAM, register file memory) cells
- Standard and specific I/Os: LVDS and PCI
- A set of analog blocks:
  - a 1.8V 200mA Linear Voltage Regulator (REG200RHA)
  - an 8-channel analog input multiplexer (MUX8RHA)
  - a PLL, 40 to 450 MHz (PLL400MRHA)
  - an RC Oscillator, 4/8/10/12MHz (OSCRC10MRHA)
  - a bandgap reference, 1.215V (BG1V2RHA)

1.8 PHYSICAL DIMENSIONS AND TERMINAL IDENTIFICATION

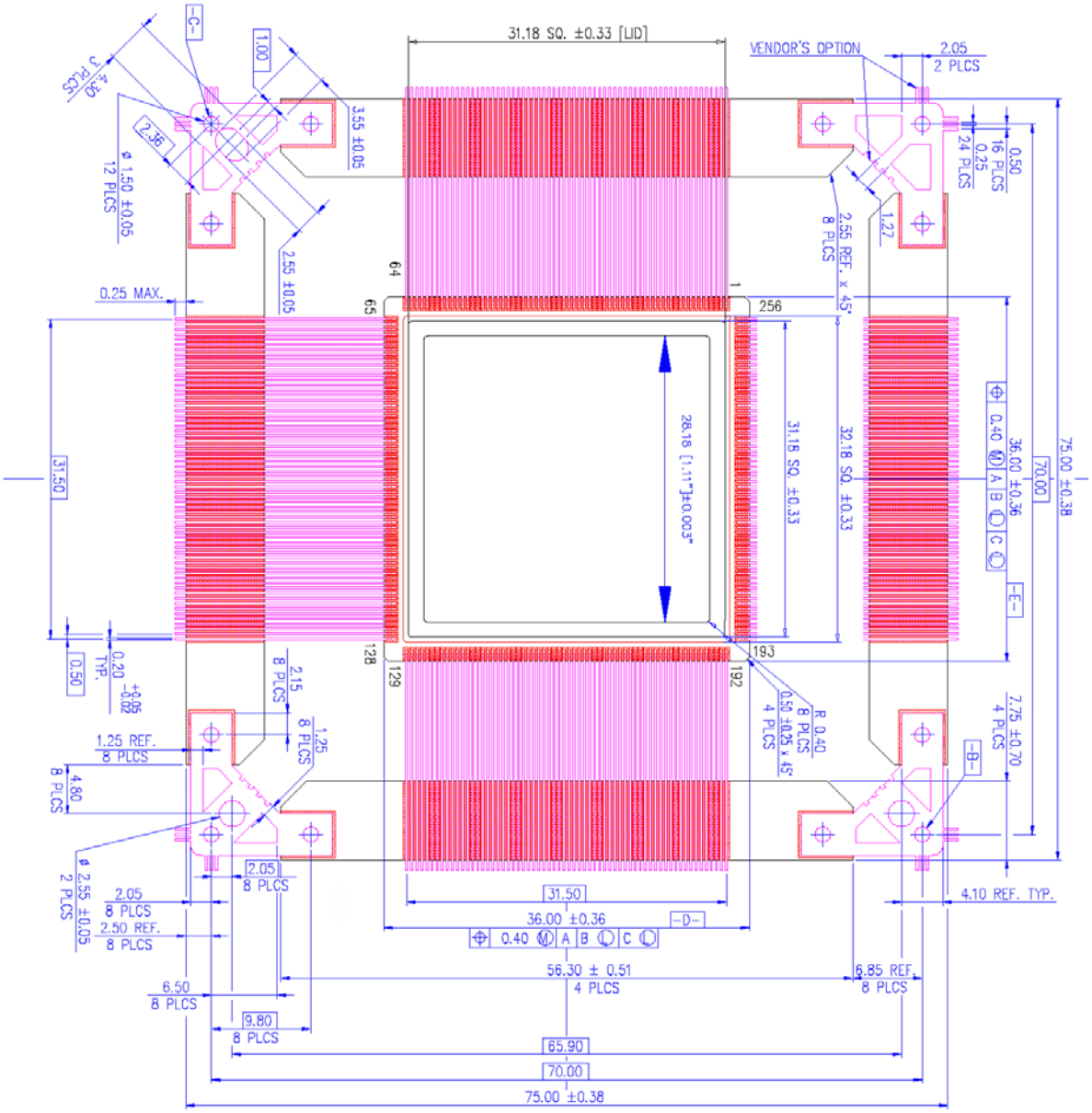
1.8.1 Flat-substrate Ceramic Quad Flat Package (FS CQFP-132) - 132 Tied Leads

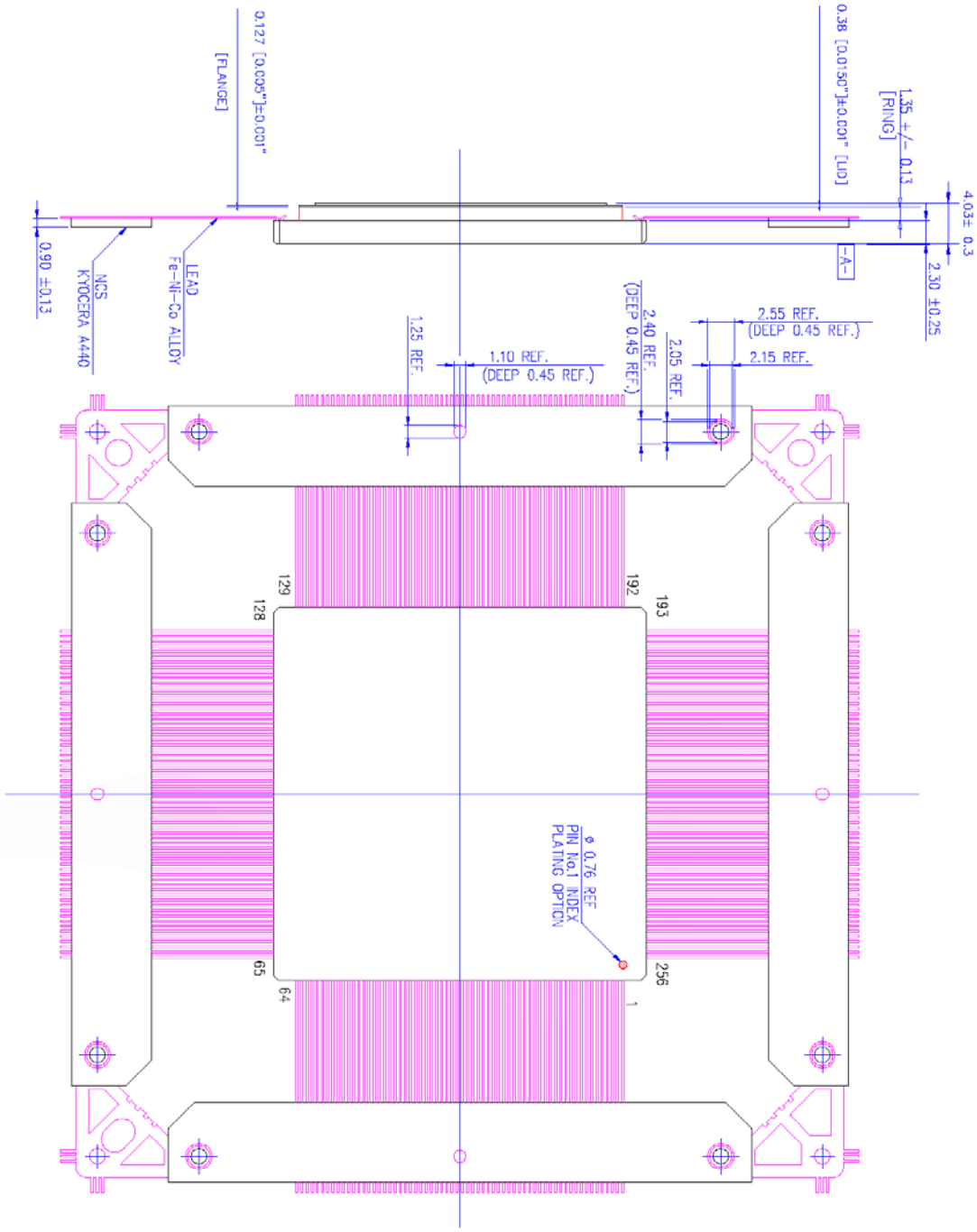


NOTES:

1. Terminal identification is specified by reference to the chamfered index corner and DETAIL “A” as shown.

1.8.2 Flat-substrate Ceramic Quad Flat Package (FS CQFP-256) - 256 Tied Leads

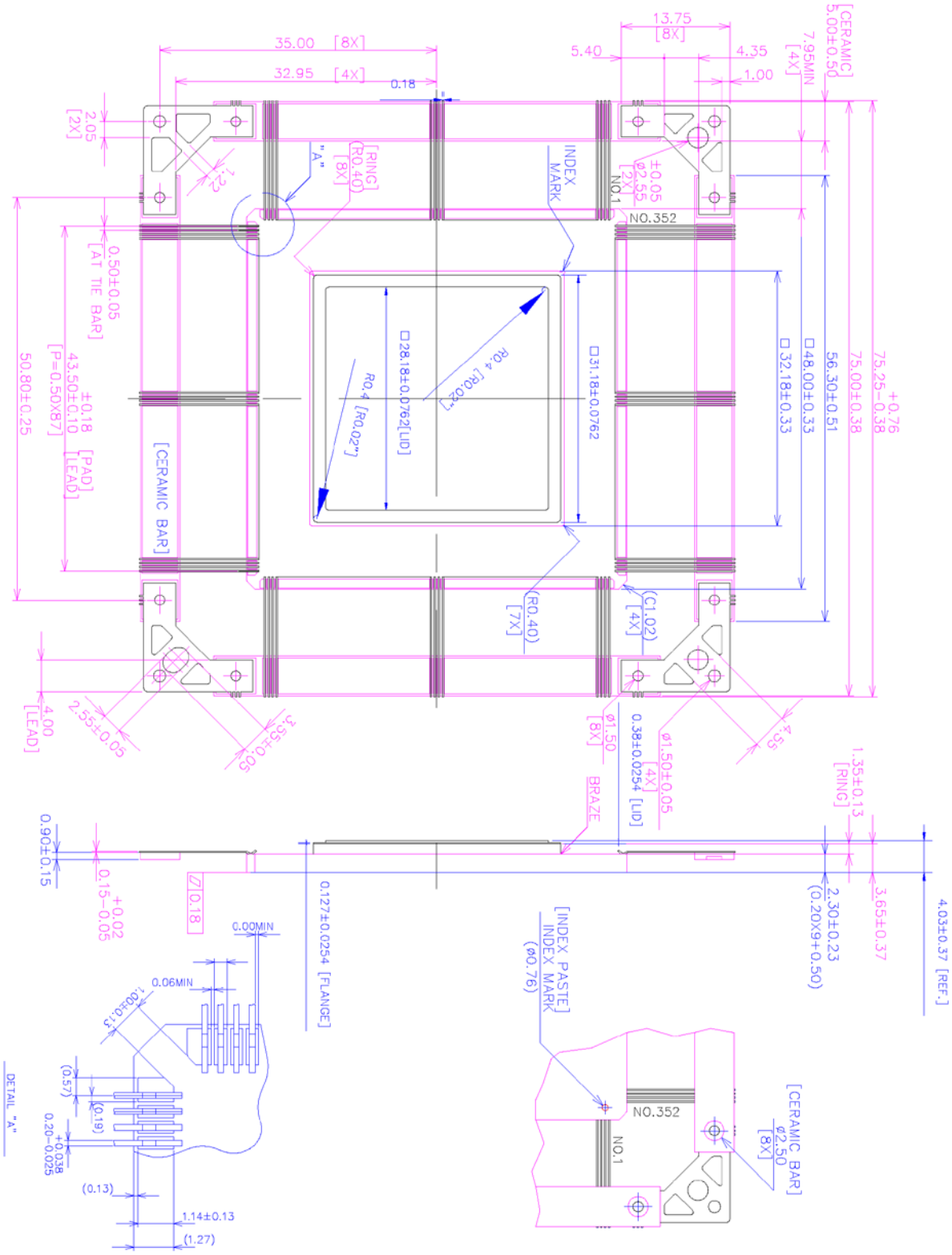




NOTES:

1. Terminal identification is specified by reference to the Pin No. 1 index as shown.

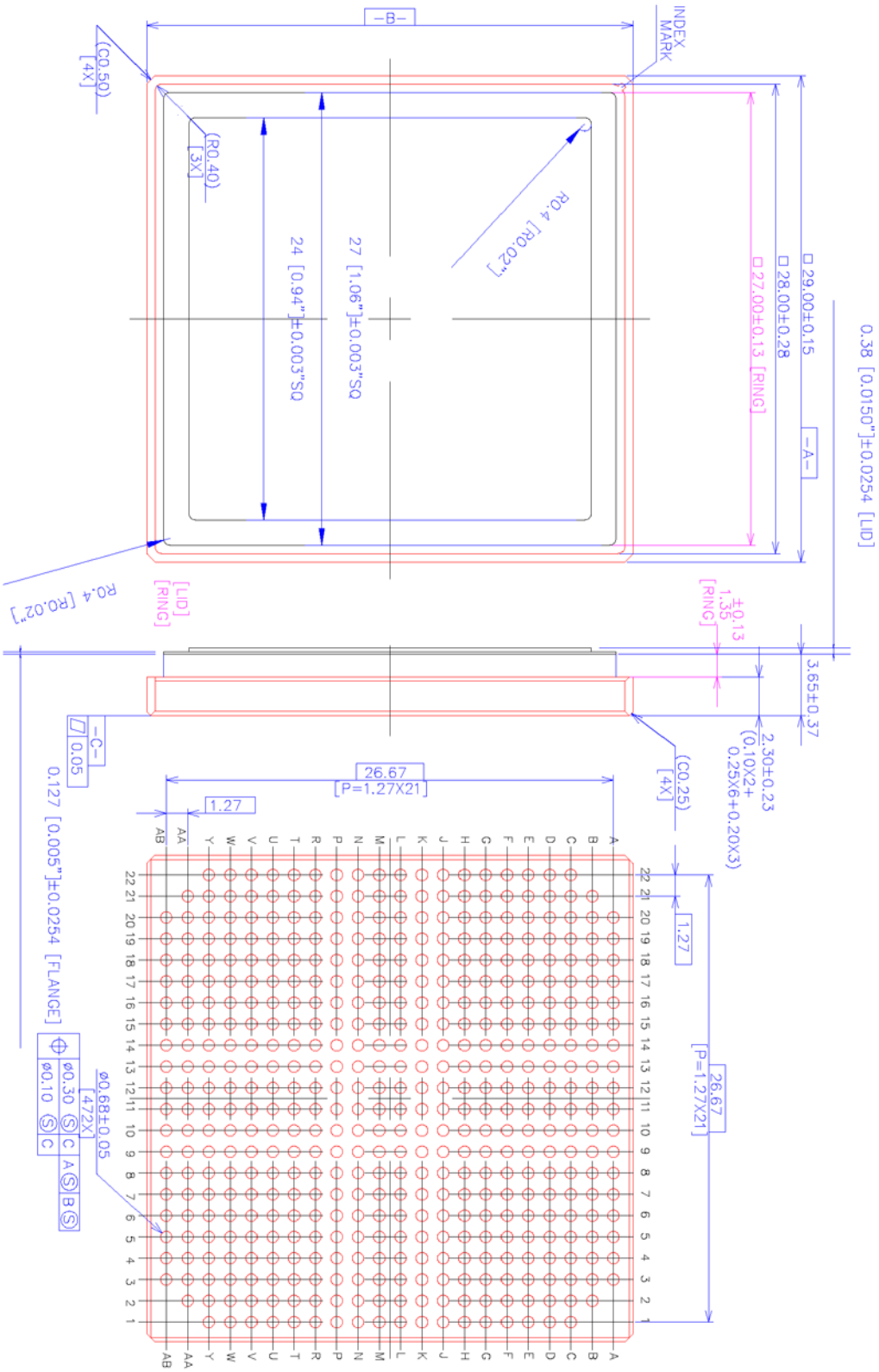
1.8.3 Flat-substrate Ceramic Quad Flat Package (FS CQFP-352) - 352 Tied Leads



NOTES:

1. Terminal identification is specified by reference to the index mark as shown.

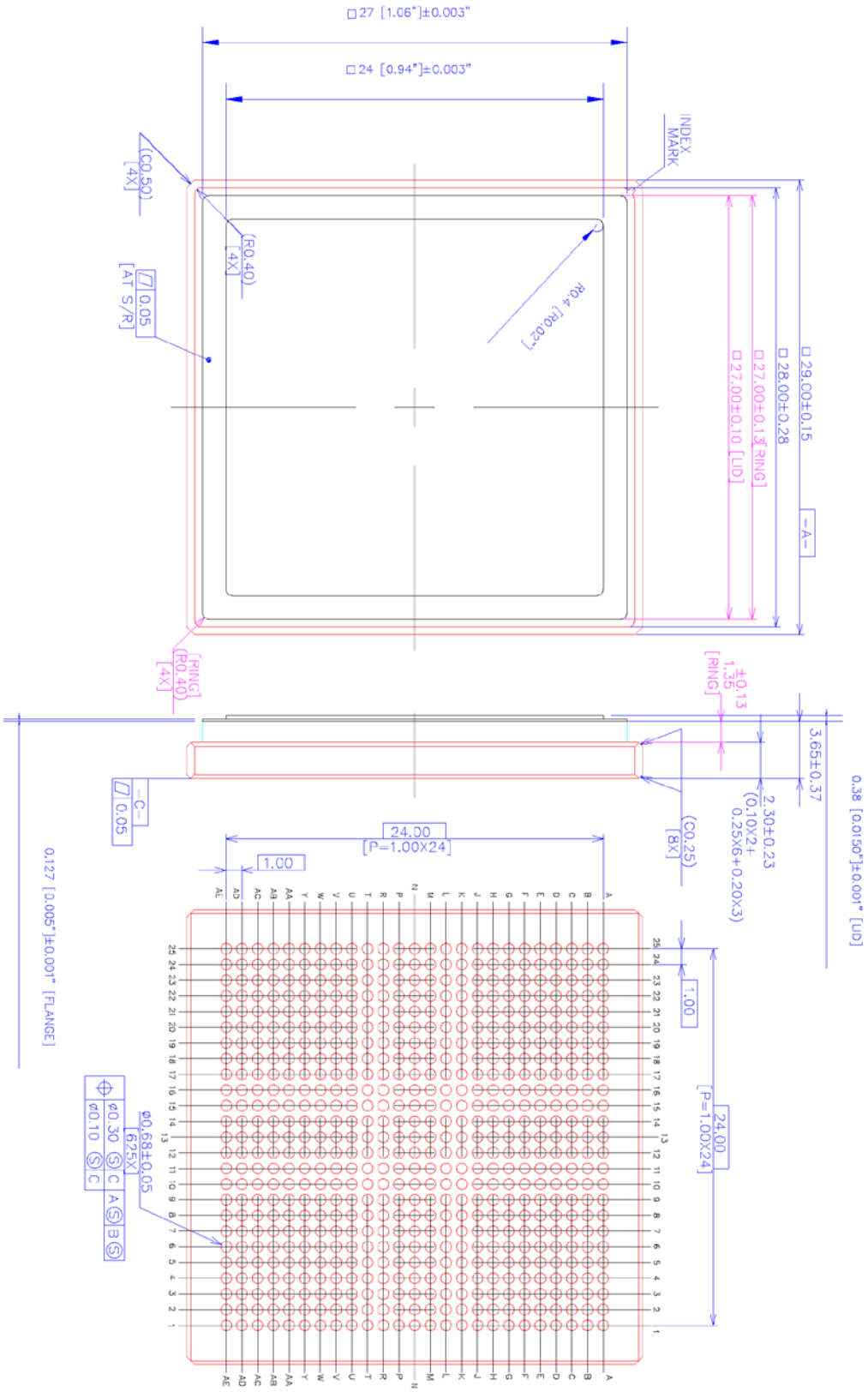
1.8.4 Flat-substrate Ceramic Land Grid Array (FS CLGA-472) - 472 Pads



NOTES:

1. Terminal identification is specified by reference to the index mark as shown.

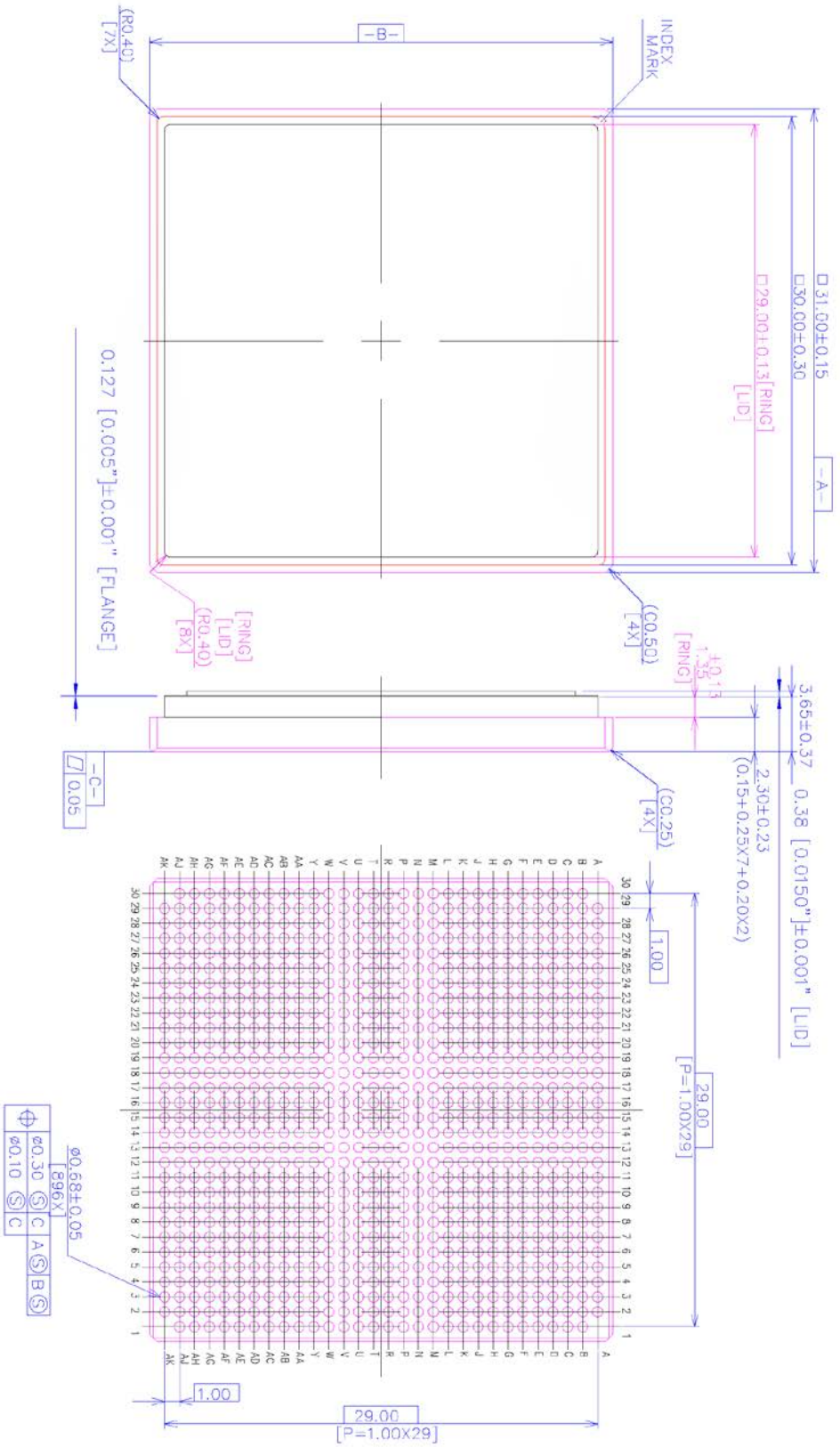
1.8.5 Flat-substrate Ceramic Land Grid Array (FS CLGA-625) - 625 Pads



NOTES:

1. Terminal identification is specified by reference to the index mark as shown.

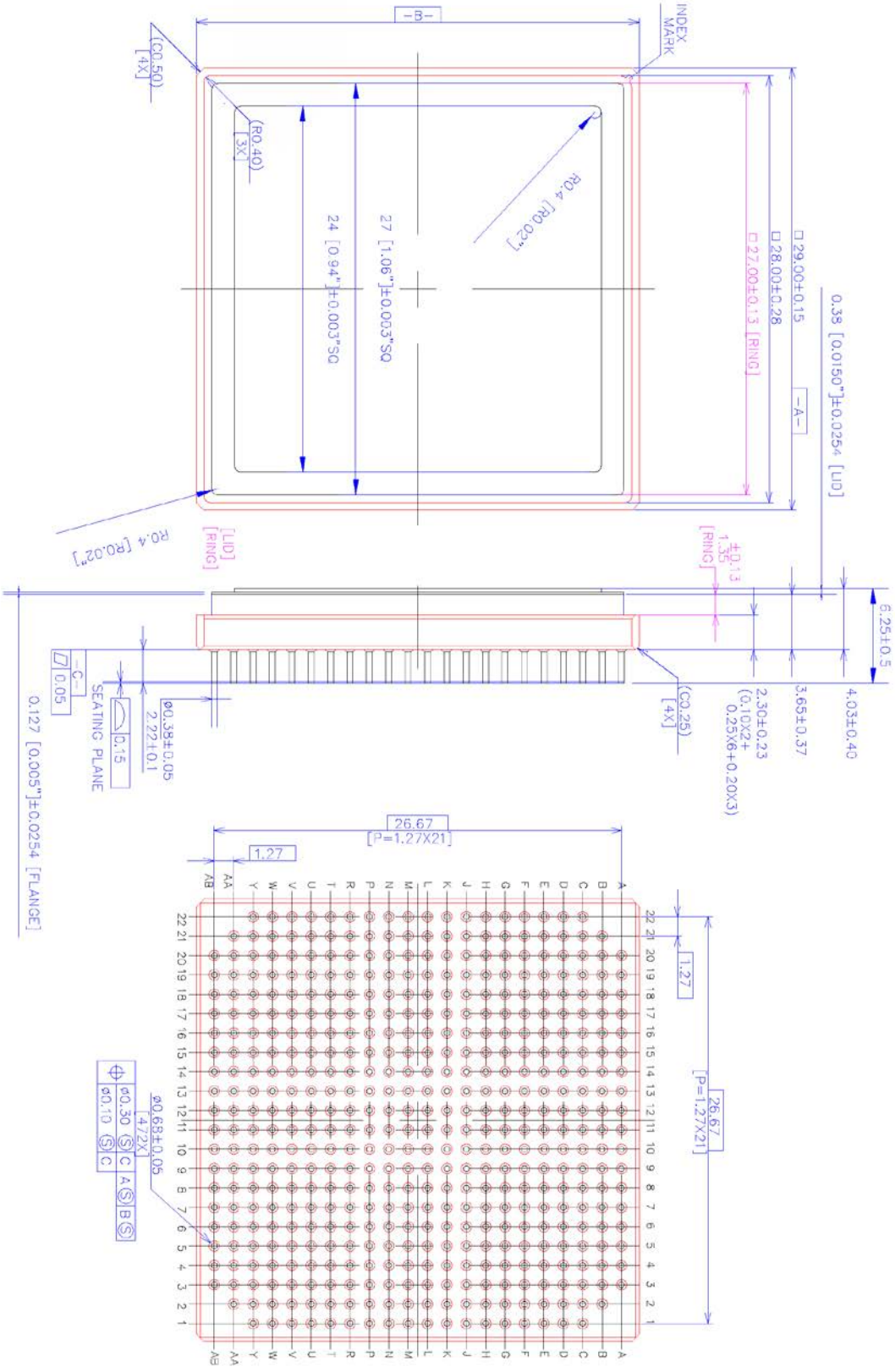
1.8.6 Flat-substrate Ceramic Land Grid Array (FS CLGA-896) - 896 Pads



NOTES:

1. Terminal identification is specified by reference to the index mark as shown.

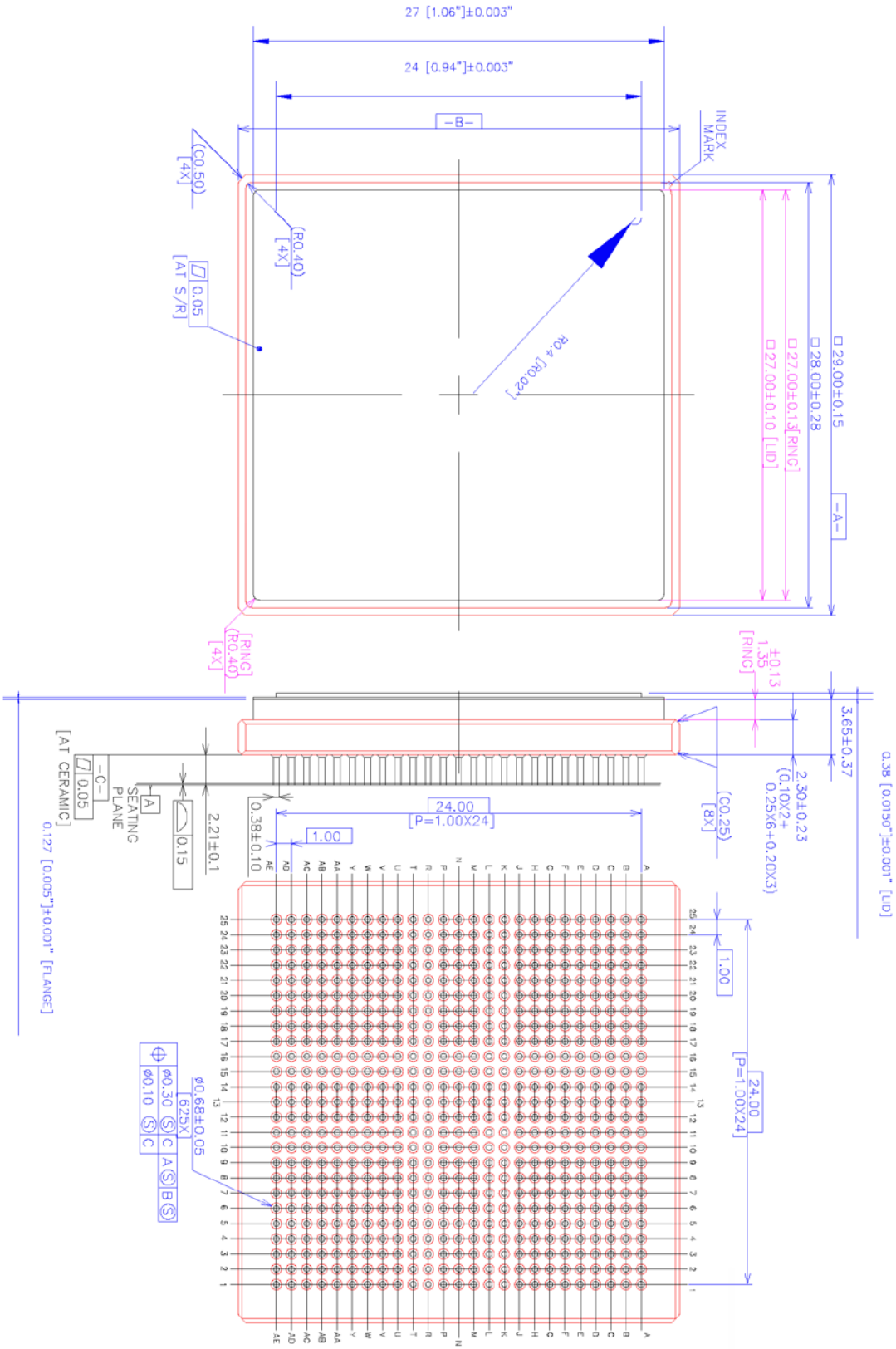
1.8.7 Flat-substrate Ceramic Column Grid Array (FS CCGA-472) - 472 Columns



NOTES:

1. Terminal identification is specified by reference to the index mark as shown.

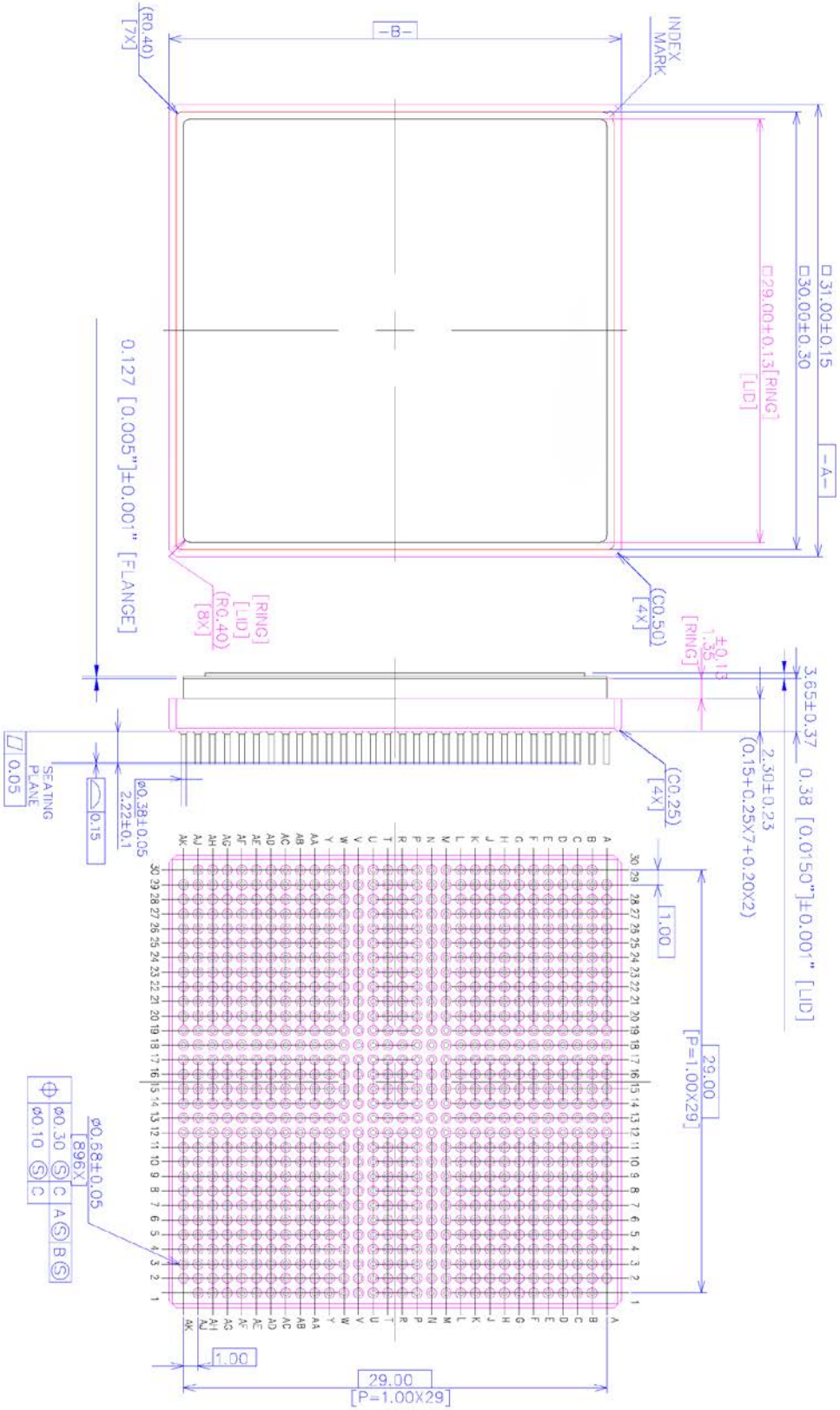
1.8.8 Flat-substrate Ceramic Column Grid Array (FS CCGA-625) - 625 Columns



NOTES:

1. Terminal identification is specified by reference to the index mark as shown.

1.8.9 Flat-substrate Ceramic Column Grid Array (FS CCGA-896) - 896 Columns



NOTES:

1. Terminal identification is specified by reference to the index mark as shown.

1.9 FUNCTIONAL DIAGRAM
See ASIC Sheet.

NOTES:
1. For all packages the lid is internally connected to the ground terminal as specified in the ASIC Sheet.

1.10 PIN ASSIGNMENT
See ASIC Sheet.

1.11 INSTRUCTION SET AND TIMING DIAGRAMS
See ASIC Sheet.

2 REQUIREMENTS

2.1 GENERAL
The complete requirements for procurement of the components specified herein are as stated in this specification and the ESCC Generic Specification. Permitted deviations from the Generic Specification, applicable to this specification only, are listed below.

Permitted deviations from the Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESCC requirement and do not affect the component's reliability, are listed in the appendices attached to this specification.

2.1.1 Deviations from the Generic Specification

2.1.1.1 Deviations from Screening Tests
High Temperature Reverse Bias Burn-in shall not be performed.

2.2 MARKING
The marking shall be in accordance with the requirements of ESCC Basic Specification No. 21700 and as follows.

As a minimum the information to be marked on the component shall be:

(a) The ESCC qualified components symbol (for ESCC qualified components only).
(b) The ESCC Component Number (see Para. 1.4.1).
(c) Traceability information.

The complete marking shall be as specified in the ASIC Sheet.

2.3 ELECTRICAL MEASUREMENTS AT ROOM, HIGH AND LOW TEMPERATURES
Electrical measurements shall be performed at room, high and low temperatures. Consolidated notes are given in Para. 2.3.3.

2.3.1 Room Temperature Electrical Measurements
The measurements shall be performed at T_{case} = +25 (+3 -5)°C.

2.3.1.1 Room Temperature Electrical Measurements for Components Specified at Supply Voltage V_{CC} = 3.3V

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1 $1.65V \le V_{DD} \le 1.95V$ $3V \le V_{CC33} \le 3.6V$	Limits		Units
				Min	Max	
Functional Test 1	-	3014	See ASIC Sheet V_{CC} = 3V	-	-	-
Functional Test 2	-	3014	See ASIC Sheet V_{CC} = 3.3V	-	-	-
Functional Test 3	-	3014	See ASIC Sheet V_{CC} = 3.6V	-	-	-
Supply Current, Stand-by	I_{CCSB}	3005	See ASIC Sheet			mA
Supply Current, Operating	I_{CCOP}	3005	See ASIC Sheet			mA
Low Level Input Current	I_{IL}	3009	$V_{IN} = V_{SS}$ CMOS Buffers LVDS Buffers	 -1 -10	 1 10	µA
Low Level Input Current with Pull-up	I_{ILPU}	3009	$V_{IN} = V_{SS}$ CMOS Buffers	 -400	 -	µA
Low Level Input Current with Pull-down	I_{ILPD}	3009	$V_{IN} = V_{SS}$ CMOS Buffers	 -5	 5	µA
High Level Input Current	I_{IH}	3010	$V_{IN} = V_{CC}$ CMOS Buffers LVDS Buffers	 -1 -10	 1 10	µA
High Level Input Current with Pull-up	I_{IHPU}	3010	$V_{IN} = V_{CC}$ CMOS Buffers	 -5	 5	µA
High Level Input Current with Pull-down	I_{IHPD}	3010	$V_{IN} = V_{CC}$ CMOS Buffers	 -	 600	µA
Low Level Input Voltage	V_{IL}	-	V_{CC} = 3V CMOS Buffers PCI Buffers	 - -	 0.8 $0.3*V_{CC}$	V
High Level Input Voltage	V_{IH}	-	V_{CC} = 3.6V CMOS Buffers PCI Buffers	 2 $0.5*V_{CC}$	 - -	V
Low Level Output Voltage 1	V_{OL1}	3007	V_{CC} = 3V I_{OL} = 2, 4, 8, 12, 16mA	-	0.4	V
High Level Output Voltage 1	V_{OH1}	3006	V_{CC} = 3V I_{OH} = -2, -4, -6, -8, -16mA	V_{CC}-0.4	-	V
Output Leakage Current Third State, Low Level Applied	I_{OZL}	3020	$V_{OUT} = V_{SS}$	-1	1	µA
Output Leakage Current Third State, High Level Applied	I_{OZH}	3021	V_{OUT} = 3.6V	-1	1	µA

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1 $1.65V \le V_{DD} \le 1.95V$ $3V \le V_{CC33} \le 3.6V$	Limits		Units
				Min	Max	
Input Leakage Current, Cold Sparing	I_{ICS}	-	V_{IN} = 0 to V_{CC}	-1	1	µA
Output Leakage Current, Cold Sparing	I_{OCS}	-	V_{OUT} = 0 to V_{CC}	-1	1	µA
High Level Output Voltage 2	V_{OH2}	-	PCI Buffers I_{OH} = 16mA	V_{CC}-0.4	-	V
Low Level Output Voltage 2	V_{OL2}	-	PCI Buffers I_{OL} = 16mA	-	0.4	V
Output Differential Voltage	V_{OD}	-	LVDS Transmitter buffers	247	454	mV
Delta Output Differential Voltage	ΔV_{OD}	-	LVDS Transmitter buffers	0	50	mV
Common Mode Output Voltage	V_{OS}	-	LVDS Transmitter buffers	1125	1375	mV
Delta Common Mode Output Voltage	ΔV_{OS}	-	LVDS Transmitter buffers	0	50	mV
Input Capacitance	C_{IN}	3012	Note 2	-	7	pF
Timings	-	3003	See ASIC Sheet			ns
Analog Blocks Parameters	-	-	See ASIC Sheet			-

2.3.1.2 Room Temperature Electrical Measurements for Components Specified at Supply Voltage V_{CC} = 2.5V

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1 $1.65V \le V_{DD} \le 1.95V$ $2.3V \le V_{CC25} \le 2.7V$	Limits		Units
				Min	Max	
Functional Test 1	-	3014	See ASIC Sheet V_{CC} = 2.3V	-	-	-
Functional Test 2	-	3014	See ASIC Sheet V_{CC} = 2.5V	-	-	-
Functional Test 3	-	3014	See ASIC Sheet V_{CC} = 2.7V	-	-	-
Supply Current, Stand-by	I_{CCSB}	3005	See ASIC Sheet			mA
Supply Current, Operating	I_{CCOP}	3005	See ASIC Sheet			mA
Low Level Input Current	I_{IL}	3009	V_{IN} = V_{SS} CMOS Buffers LVDS Buffers	 -1 -10	 1 10	µA
Low Level Input Current with Pull-up	I_{ILPU}	3009	V_{IN} = V_{SS} CMOS Buffers	 -260	 -	µA

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1 $1.65V \le V_{DD} \le 1.95V$ $2.3V \le V_{CC25} \le 2.7V$	Limits		Units
				Min	Max	
Low Level Input Current with Pull-down	I_{ILPD}	3009	$V_{IN} = V_{SS}$ CMOS Buffers	-5	5	µA
High Level Input Current	I_{IH}	3010	$V_{IN} = V_{CC}$ CMOS Buffers LVDS Buffers	-1 -10	1 10	µA
High Level Input Current with Pull-up	I_{IHPU}	3010	$V_{IN} = V_{CC}$ CMOS Buffers	-5	5	µA
High Level Input Current with Pull-down	I_{IHPD}	3010	$V_{IN} = V_{CC}$ CMOS Buffers	-	360	µA
Low Level Input Voltage	V_{IL}	-	$V_{CC} = 2.3V$ CMOS Buffers	-	0.7	V
High Level Input Voltage	V_{IH}	-	$V_{CC} = 2.7V$ CMOS Buffers	2	-	V
Low Level Output Voltage 1	V_{OL1}	3007	$V_{CC} = 2.3V$ $I_{OL} = 1.5, 3, 6, 9, 12mA$	-	0.4	V
High Level Output Voltage 1	V_{OH1}	3006	$V_{CC} = 2.3V$ $I_{OH} = -1.5, -3, -6, -9, -16mA$	V_{CC}-0.4	-	V
Output Leakage Current Third State, Low Level Applied	I_{OZL}	3020	$V_{OUT} = V_{SS}$	-1	1	µA
Output Leakage Current Third State, High Level Applied	I_{OZH}	3021	$V_{OUT} = 2.7V$	-1	1	µA
Input Leakage Current, Cold Sparing	I_{ICS}	-	$V_{IN} = 0$ to V_{CC}	-1	1	µA
Output Leakage Current, Cold Sparing	I_{OCS}	-	$V_{OUT} = 0$ to V_{CC}	-1	1	µA
Differential Output Voltage	V_{OD}	-	LVDS Transmitter buffers	247	454	mV
Delta Differential Output Voltage	ΔV_{OD}	-	LVDS Transmitter buffers	0	50	mV
Common Mode Output Voltage	V_{OS}	-	LVDS Transmitter buffers	1125	1375	mV
Delta Common Mode Output Voltage	ΔV_{OS}	-	LVDS Transmitter buffers	0	50	mV
Input Capacitance	C_{IN}	3012	Note 2	-	7	pF
Timings	-	3003	See ASIC Sheet			ns
Analog Blocks Parameters	-	-	See ASIC Sheet			-

2.3.2 High and Low Temperatures Electrical Measurements

Unless otherwise specified the measurements shall be performed at T_{case} = +125 ±3°C and T_{case} = -55 ±3°C. Unless otherwise specified the characteristics, test methods, conditions and limits shall be the same as specified for Para. 2.3.1 Room Temperature Electrical Measurements.

2.3.3 Notes to Electrical Measurements Tables

1. Unless otherwise specified: all inputs and outputs shall be tested for each characteristic; Inputs not under test shall be V_{IN} = V_{SS}, V_{CC} or V_{DD} and outputs not under test shall be open; V_{SS} = 0V.
2. Tested at initial design and after major process changes, otherwise guaranteed.

2.4 PARAMETER DRIFT VALUES

Unless otherwise specified, the measurements shall be performed at T_{case} = +25 (+3 -5)°C.

The test methods and test conditions shall be as per the corresponding test defined in Para. 2.3.1 Room Temperature Electrical Measurements.

The drift values (Δ) shall not be exceeded for each characteristic specified. The corresponding absolute limit values for each characteristic shall not be exceeded.

Characteristics	Symbols	Limits			Units
		Drift Value Δ	Absolute		
			Min	Max	
Supply Current, Stand-by	I_{CCSB}	See ASIC Sheet			mA
Low Level Input Current CMOS Buffers LVDS Buffers	I_{IL}	 ±0.03 ±1	 -1 -10	 1 10	µA
High Level Input Current CMOS Buffers LVDS Buffers	I_{IH}	 ±0.03 ±1	 -1 -10	 1 10	µA
Output Leakage Current Third State, Low Level Applied	I_{OZL}	±0.03	-1	1	µA
Output Leakage Current Third State, High Level Applied	I_{OZH}	±0.03	-1	1	µA
Low Level Output Voltage 1	V_{OL1}	±0.1	-	0.4	V
High Level Output Voltage 1	V_{OH1}	±0.1	V_{CC}-0.4	-	V

NOTES:

1. Unless otherwise specified all inputs and outputs shall be tested for each characteristic.

2.5 INTERMEDIATE AND END-POINT ELECTRICAL MEASUREMENTS

Unless otherwise specified, the measurements shall be performed at T_{case} = +25 (+3 -5)°C. Unless otherwise specified the characteristics, test methods, conditions and limits shall be the same as specified for Para. 2.3.1 Room Temperature Electrical Measurements.

2.6 POWER BURN-IN CONDITIONS

See ASIC Sheet.

2.7 OPERATING LIFE CONDITIONS

Unless otherwise specified the conditions shall be as specified in Para. 2.6 for Power Burn-in.

2.8 TOTAL DOSE RADIATION TESTING

2.8.1 Bias Conditions and Total Dose Level for Total Dose Radiation Testing

Continuous bias shall be applied during irradiation testing as specified in the ASIC Sheet.

The total dose level applied shall be as specified in Para. 1.4.2, in the ASIC Sheet or in the Purchase Order.

2.8.2 Electrical Measurements for Total Dose Radiation Testing

Prior to irradiation testing the devices shall have successfully met Para. 2.3.1 Room Temperature Electrical Measurements specified herein.

Unless otherwise stated the measurements shall be performed at T_{case} = +25 (+3 -5)°C.

The test methods and test conditions shall be as per the corresponding test defined in Para. 2.3.1 Room Temperature Electrical Measurements.

The parameters to be measured during and on completion of irradiation testing are specified in the ASIC Sheet.