INTEGRATED CIRCUITS, SILICON MONOLITHIC, CMOS DIGITAL, FIELD PROGRAMMABLE GATE ARRAY, 280000 GATES

BASED ON TYPE ATF280F

ESCC Detail Specification No. 9304/009

Issue 1	November 2014

Document Custodian: European Space Agency – see https://escies.org

LEGAL DISCLAIMER AND COPYRIGHT

DOCUMENTATION CHANGE NOTICE

(Refer to https://escies.org for ESCC DCR content)

DCR No.	CHANGE DESCRIPTION

TABLE OF CONTENTS

1 GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics and test and inspection data for the component type variants and/or the range of components specified below. It supplements the requirements of, and shall be read in conjunction with, the ESCC Generic Specification listed under Applicable Documents.

1.2 APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:

(a) ESCC Generic Specification No. 9000.
(b) MIL-STD-883, Test Methods and Procedures for Microelectronics.

1.3 TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESCC Basic Specification No. 21300 shall apply.

1.4 THE ESCC COMPONENT NUMBER AND COMPONENT TYPE VARIANTS

1.4.1 The ESCC Component Number

The ESCC Component number shall be constituted as follows:

Example: 930400901R

- Detail Specification Reference: 9304009
- Component Type Variant Number: 01 (as required)
- Total Dose Radiation Level Letter: R (as required)

1.4.2 Component Type Variants

The component type variants applicable to this specification are as follows:

Variant Number	Based on Type	Case	Terminal Material and Finish	Weight max g	Total Dose Radiation Level Letter (Note 3)
01	ATF280F	MQFP-T352	D2 (Note 1)	14	R [100kRAD(Si)]
02	ATF280F	MCGA-472	Note 2	10	R [100kRAD(Si)]
03	ATF280F	MQFP-T256	D2 (Note 1)	7	R [100kRAD(Si)]

NOTES:

1. The terminal material and finish shall be in accordance with the requirements of ESCC Basic Specification No. 23500.
2. The terminal material shall be tungsten and the finish shall be 0.03µm to 0.1µm gold plating over 3.2µm minimum nickel underplating.
3. The total dose radiation level letter shall be as defined in ESCC Basic Specification No. 22900. If an alternative radiation test level is specified in the Purchase Order the letter shall be changed accordingly.

1.5 MAXIMUM RATINGS

The maximum ratings shall not be exceeded at any time during use or storage. Functional performance for extended periods at the maximum ratings may adversely affect device reliability.

Maximum ratings shall only be exceeded during testing to the extent specified in this specification and when stipulated in Test Methods and Procedures of the ESCC Generic Specification.

Characteristics	Symbols	Maximum Ratings	Units	Remarks
Supply Voltage	V_{DD} V_{CC}	-0.3 to 2 -0.3 to 4	V	Notes 1, 2
Input Voltage Range	V_{IN}	-0.3 to 4	V	Note 2
Output Voltage Range	V_{OUT}	-0.3 to 4	V	Note 2
Device Power Dissipation	P_D	3.3	W	
Operating Temperature Range	T_{op}	-55 to +125	^oC	T_{amb}
Storage Temperature Range	T_{stg}	-65 to +150	^oC	
Junction Temperature	T_j	+175	^oC	
Thermal Resistance, Junction to Case Variants 01, 03 Variant 02	$R_{th(j-c)}$	 2 1	$^oC/W$	
Soldering Temperature MQFP case MCGA case	T_{sol}	 +300 +220	^oC	 Note 3 Note 4

NOTES:

1. V_{DD} is for core. V_{CC} is for I/O.
2. With reference to V_{SS} = 0V.
3. For MQFP-T256 and MQFP-T352 packages, duration 10 seconds maximum at a distance of not less than 1.6mm from the device body and the same terminal shall not be resoldered until 3 minutes have elapsed.
4. For the MCGA package, during reflow.

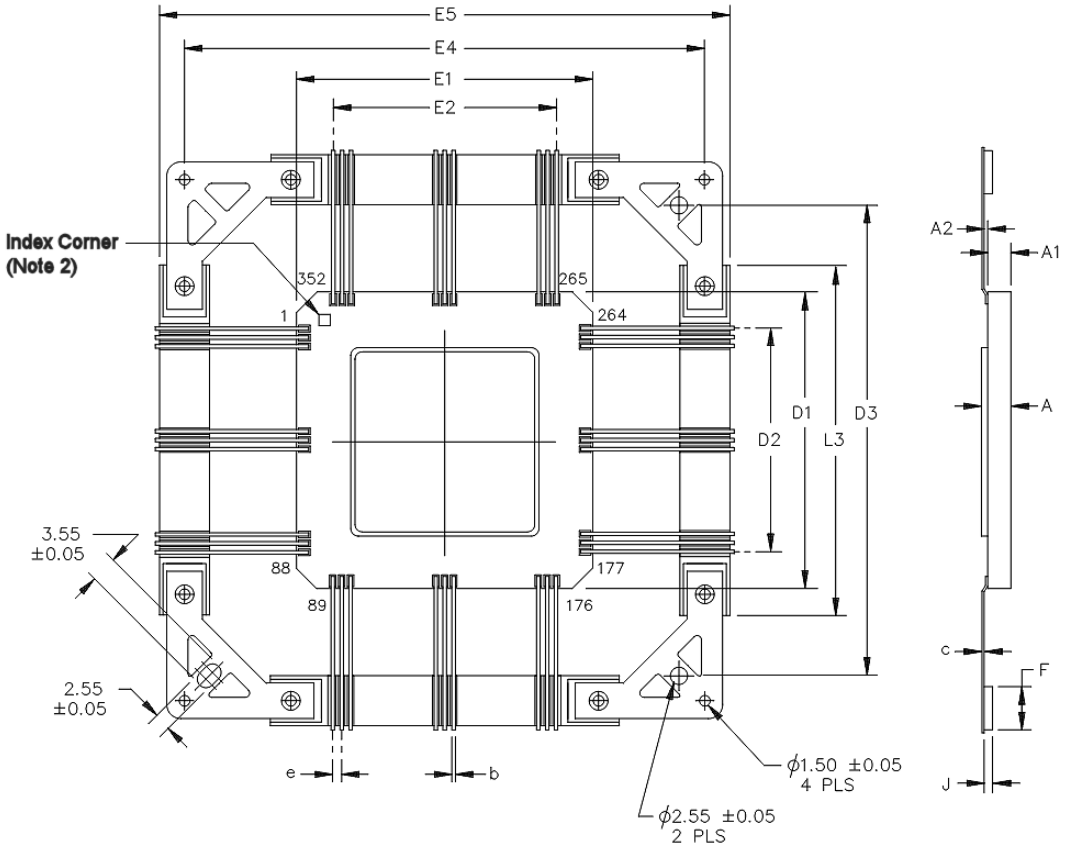
1.6 HANDLING PRECAUTIONS

These devices are susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacture, testing, packaging, shipment and any handling.

These components are categorised as Class 1 per ESCC Basic Specification No. 23800 with a Minimum Critical Path Failure Voltage of 1000 Volts.

1.7 PHYSICAL DIMENSIONS AND TERMINAL IDENTIFICATION

1.7.1 Multilayer Quad Flat Package (MQFP-T352) - 352 Tied Leads

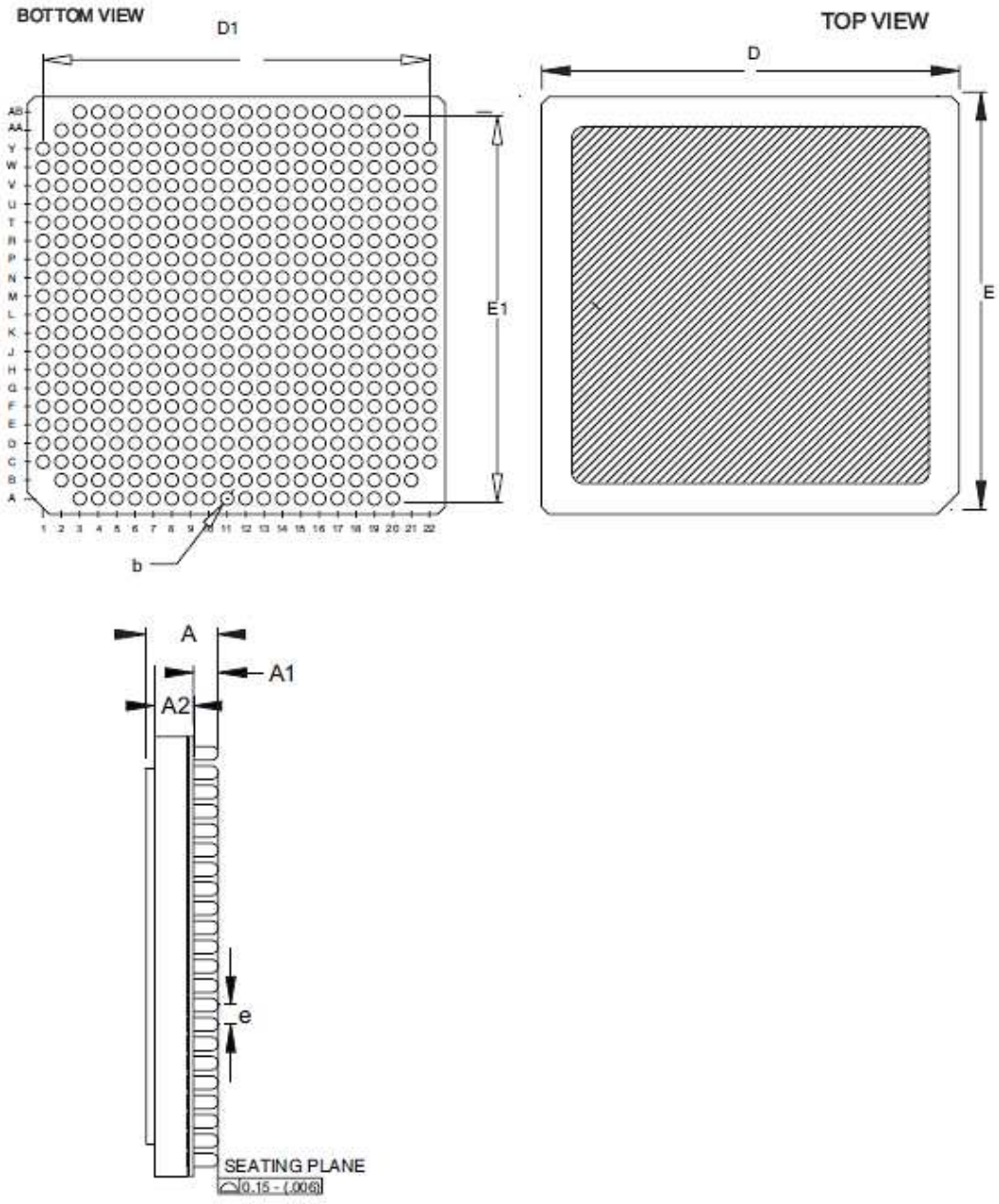


Symbols	Dimensions mm		Notes
	Min	Max	
A	2.77	3.15	
A1	2.36	2.68	
A2	0.41	0.47	
b	0.15	0.25	1
c	0.1	0.2	1
D1/E1	47.67	48.33	
D2/E2	43.37	43.63	
D3	65.89 BSC		
E4	70 BSC		
E5	74.87	76.01	
e	0.45	0.55	1
F	4.5	5.5	

Symbols	Dimensions mm		Notes
	Min	Max	
J	0.75	1.05	
L3	55.79	56.81	

NOTES:
1. Applies to all leads.
2. Terminal identification is specified by reference to the index corner as shown.

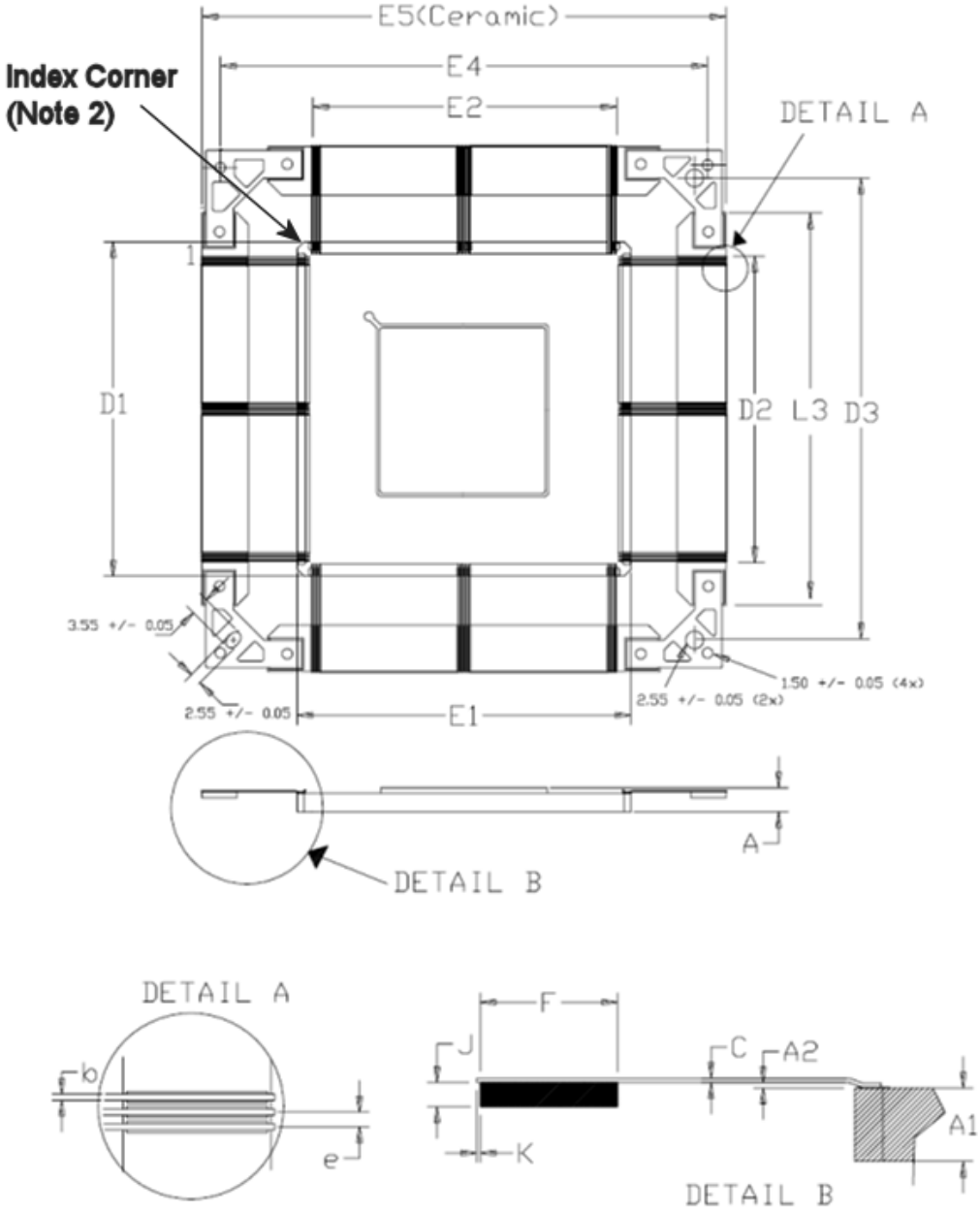
1.7.2 Multilayer Column Grid Array (MCGA-472) - 472 Columns



Symbols	Dimensions mm		Notes
	Min	Max	
A	4.3	5.9	
A1	1.4	1.85	
A2	2.6	3.45	
b	0.79	0.99	1
D/E	28.77	29.23	
D1/E1	26.67 BSC		
e	1.27 BSC		1

NOTES:
1. Applies to all columns.
2. Terminal identification is specified by reference to the index corner as shown.

1.7.3 Multilayer Ceramic Quad Flat Package (MQFP-T256) – 256 Tied Leads

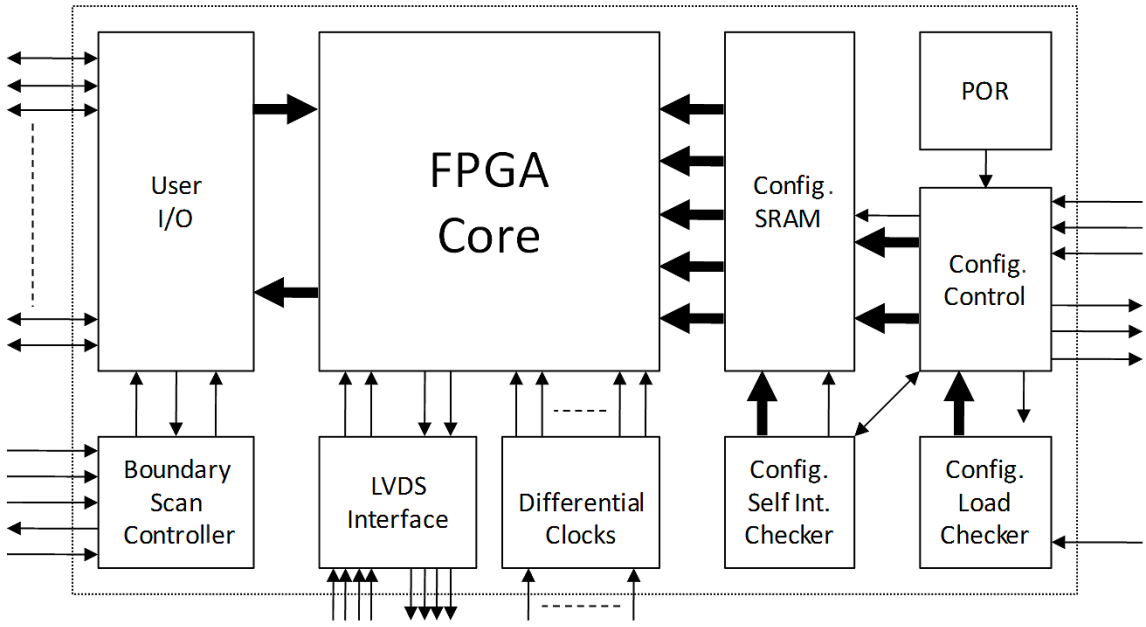


Symbols	Dimensions mm		Notes
	Min	Max	
A	2.5	3.22	
A1	2.06	2.56	
A2	0.2 BSC		
b	0.2 BSC		1
C	0.1	0.2	1

Symbols	Dimensions mm		Notes
	Min	Max	
D1/E1	35.64	36.36	
D2/E2	31.5 BSC		
D3	65.9 BSC		
E4	70 BSC		
E5	74.6	75.4	
e	0.5 BSC		1
F	7.05	8.45	
J	0.77	1.03	
K	-	0.25	1
L3	56.3 BSC		

NOTES:
1. Applies to all leads.
2. Terminal identification is specified by reference to the index corner as shown.

1.8 FUNCTIONAL DIAGRAM



NOTES:
1. For all packages the lid is internally connected to the ground terminal.

1.9 PIN ASSIGNMENTS

Consolidated notes are given after the Pin Assignments.

1.9.1 Pin Assignments for Variants with MQFP Packages

Lead	Function		Lead	Function	
	MQFP-T352	MQFP-T256		MQFP-T352	MQFP-T256
1	M1	M1	47	OLVDS4	IO407
2	M2	M2	48	OLVDS4N	VCC2
3	IO241, GCK3	IO241, GCK3	49	VCC2	IO411
4	VCC2	VCC2	50	IO365	IO419, D10
5	IO259, LDC	VCC2	51	IO367	IO425
6	IO263	IO251	52	IO371	IO433
7	VSS	VSS	53	IO373, D12	IO443, D9
8	VCC1	VCC1	54	IO377	IO445
9	IO265, HDC	IO259, LDC	55	IO379	IO457
10	IO267	IO265, HDC	56	IO383	VCC2
11	IO271	IO271	57	IO385	VSS
12	VCC2	IO279, D15	58	VCC2	VCC1
13	IO273	IO283	59	IO387	VCC2
14	IO277	IO287	60	IO393	IO459
15	IO279, D15	IO293	61	IO397, D11	IO465, D8
16	IO283	VCC2	62	IO403	IO471
17	IO285	VCC2	63	IO405	IO480, GCK4
18	IO291	IO303, INIT	64	IO407	CON
19	IO293	IO307	65	VCC2	RESETN
20	VCC2	IO311	66	IO411	RESERVED
21	IO297	IO317	67	IO413	IO482, GCK5
22	IO303, INIT	IO323, D14	68	IO417	IO487
23	IO305	IO327	69	IO419, D10	VCC2
24	IO307	IO333	70	IO423	VCC2
25	IO311	IO339	71	IO425	VSS
26	IO313	VCC2	72	IO431	VCC1
27	IO317	IO345, D13	73	IO433	IO491
28	VCC2	ILVDS3	74	VCC2	IO493, D7
29	IO319	ILVDS3N	75	IO437	IO505
30	IO323, D14	ILVDS4	76	IO439	IO511
31	IO325	ILVDS4N	77	IO443, D9	IO513, D6
32	IO327	REFSOUTH	78	IO445	IO525
33	IO331	OLVDS3	79	IO447	IO531, D5
34	IO337	OLVDS3N	80	IO453	VCC2
35	IO339	OLVDS4	81	VSS	VCC2
36	VCC2	OLVDS4N	82	VCC1	IO537
37	IO343	VCC2	83	IO457	IO543, FCK3
38	IO345, D13	IO367	84	VCC2	IO547, CS0
39	IO351	IO373, D12	85	IO459	IO553
40	ILVDS3	IO379	86	IO465, D8	IO563
41	ILVDS3N	IO385	87	IO480, GCK4	IO567
42	ILVDS4	VCC2	88	CON	IO573
43	ILVDS4N	VCC2	89	RESETN	IO579
44	REFSOUTH	IO387	90	RESERVED	VCC2
45	OLVDS3	IO397, D11	91	IO482, GCK5	IO585, D4
46	OLVDS3N	IO403			

Lead	Function		Lead	Function	
	MQFP-T352	MQFP-T256		MQFP-T352	MQFP-T256
92	IO487	ILVDS5	137	VCC2	IO737
93	VCC2	ILVDS5N	138	IO605	IO743, A2, CS1N
94	IO493, D7	ILVDS6	139	IO611	IO747
95	VSS	ILVDS6N	140	IO613	IO753
96	VCC2	REFEAST	141	IO617, D3	IO757
97	IO505	OLVDS5	142	IO619	IO767, A3
98	IO507	OLVDS5N	143	IO623	IO773
99	IO511	OLVDS6	144	IO625	VCC2
100	VCC2	OLVDS6N	145	VCC2	IO783, A4
101	IO513, D6	VCC2	146	IO627	IO787
102	IO517	IO607	147	IO633	IO797, A5
103	IO519	IO611	148	IO637	VCC2
104	IO523	IO617, D3	149	IO639	IO803
105	IO525	IO625	150	IO643	IO811, A6
106	IO527	VCC2	151	IO645	IO817
107	IO531, D5	VCC2	152	IO647	IO823
108	IO533	IO627	153	VCC2	VCC2
109	VCC2	IO637	154	IO651	IO825, A7
110	IO537	IO645	155	IO653	IO831
111	IO539	IO651	156	IO655, CHECKN	ILVDS7
112	IO543, FCK3	IO655, CHECKN	157	IO658, FCK4	ILVDS7N
113	IO547, CS0	IO658, FCK4	158	IO665	ILVDS8
114	IO551	IO665	159	IO667	ILVDS8N
115	IO553	IO673, D2	160	IO671	REFNORTH
116	IO557	VCC2	161	IO673, D2	OLVDS7
117	VCC2	IO679	162	VCC2	OLVDS7N
118	IO559	IO687	163	IO677	OLVDS8
119	IO563	IO693, D1	164	IO679	OLVDS8N
120	IO565	VCC2	165	IO683	VCC2
121	IO567	VSS	166	IO685	IO851
122	IO571	VCC1	167	IO687	IO857, A8
123	IO573	IO699	168	IO693, D1	IO863
124	IO577	IO705	169	VSS	IO867
125	IO579	IO713, D0	170	VCC1	VCC2
126	VCC2	IO720, GCK6, CSOUTN	171	IO697	VCC2
127	IO585, D4	CCLK	172	VCC2	IO873, A9
128	ILVDS5	VCC2	173	IO699	IO883
129	ILVDS5N	TCK	174	IO713, D0	IO885
130	ILVDS6	IO722, GCK7, A1	175	IO720, GCK6, CSOUTN	IO891, A10
131	ILVDS6N	IO727, A0	176	CCLK	IO893
132	REFEAST	VCC2	177	TCK	IO899
133	OLVDS5	VCC2	178	IO722, GCK7, A1	IO905, A11
134	OLVDS5N	IO733	179	IO727, A0	IO913
135	OLVDS6	VSS	180	VCC2	VCC2
136	OLVDS6N	VCC1	181	IO733	IO923, A12

Lead	Function		Lead	Function	
	MQFP-T352	MQFP-T256		MQFP-T352	MQFP-T256
182	IO739	IO927	228	IO853	OLVDS2
183	VSS	IO937, A13	229	IO857, A8	OLVDS2N
184	VCC1	VCC2	230	IO859	VCC2
185	IO743, A2, CS1N	VSS	231	IO863	IO125
186	IO747	VCC1	232	IO865	IO133, A21
187	IO753	VCC2	233	IO867	IO139
188	VCC2	IO947	234	VCC2	IO145
189	IO757	IO953, A14	235	IO871	VCC2
190	IO759	IO960, GCK8, A15	236	IO873, A9	VCC2
191	IO765	TDO	237	IO879	IO147
192	IO767, A3	TDI	238	IO883	IO153
193	IO771	TMS	239	IO887	IO159
194	IO773	TRST	240	IO891, A10	IO165
195	IO777	IO1, GCK1, A16	241	VCC2	VCC2
196	VCC2	IO5	242	IO893	IO171
197	IO779	VCC2	243	IO897	IO177, A22
198	IO783, A4	VCC2	244	IO899	IO180, FCK2
199	IO785	VSS	245	IO905, A11	IO187
200	IO787	VCC1	246	IO907	IO193
201	IO791	IO11	247	IO911	IO203, A23
202	IO793	IO19, A17	248	IO913	IO205
203	IO797, A5	IO25	249	IO917	VSS
204	IO799	IO31	250	VCC2	VCC1
205	VCC2	IO33	251	IO919	IO217
206	IO803	IO39, A18	252	IO923, A12	VCC2
207	IO805	IO45	253	IO925	VCC2
208	IO807	IO51	254	IO927	IO225, OTSN
209	IO811, A6	VCC2	255	IO937, A13	IO240, GCK2
210	IO813	VCC2	256	IO939	M0
211	IO819	IO61, FCK1	257	VSS	
212	IO823	IO63, A19	258	VCC1	
213	VCC2	IO67	259	VCC2	
214	IO825, A7	IO73	260	IO945	
215	IO833	IO79	261	IO953, A14	
216	ILVDS7	IO85	262	IO960, GCK8, A15	
217	ILVDS7N	IO93	263	TDO	
218	ILVDS8	IO99	264	TDI	
219	ILVDS8N	VCC2	265	TMS	
220	REFNORTH	IO105, A20	266	TRST	
221	OLVDS7	ILVDS1	267	IO1, GCK1, A16	
222	OLVDS7N	ILVDS1N	268	IO13	
223	OLVDS8	ILVDS2	269	IO17	
224	OLVDS8N	ILVDS2N	270	IO19, A17	
225	VCC2	REFWEST	271	VSS	
226	IO847	OLVDS1	272	VCC1	
227	IO851	OLVDS1N	273	IO25	
			274	IO27	
			275	IO31	

Lead	Function	Lead	Function
	MQFP-T352		MQFP-T352
276	VCC2	320	IO145
277	IO33	321	VCC2
278	IO37	322	IO147
279	IO39, A18	323	IO151
280	IO43	324	IO157
281	IO45	325	IO159
282	IO47	326	IO163
283	IO51	327	IO165
284	VCC2	328	IO167
285	IO57	329	VCC2
286	IO61, FCK1	330	IO171
287	IO63, A19	331	IO173
288	IO67	332	IO175
289	IO71	333	IO177, A22
290	IO73	334	IO180, FCK2
291	IO77	335	IO185
292	VCC2	336	IO187
293	IO79	337	IO191
294	IO85	338	IO193
295	IO87	339	VCC2
296	IO93	340	IO199
297	IO97	341	IO203, A23
298	IO99	342	IO205
299	VCC2	343	IO207
300	IO103	344	IO213
301	IO105, A20	345	VSS
302	IO111	346	VCC1
303	ILVDS1	347	IO217
304	ILVDS1N	348	VCC2
305	ILVDS2	349	IO219
306	ILVDS2N	350	IO225, OTSN
307	REFWEST	351	IO240, GCK2
308	OLVDS1	352	M0
309	OLVDS1N		
310	OLVDS2		
311	OLVDS2N		
312	VCC2		
313	IO125		
314	IO127		
315	IO131		
316	IO133, A21		
317	IO137		
318	IO139		
319	IO143		

1.9.2 Pin Assignment for Variant 02 – MCGA-472 Package

Column	Function	Column	Function
A3	VCC1	C13	ILVDS5
A4	VSS	C14	IO565
A5	IO691	C15	VCC2
A6	VCC2	C16	IO523
A7	IO667	C17	VCC2
A8	VCC2	C18	IO503
A9	IO633	C19	IO497
A10	IO617, D3	C20	VSS
A11	VCC2	C21	VCC1
A12	IO583	C22	VCC1
A13	IO579	D1	VSS
A14	VCC2	D2	IO743, A2, CS1N
A15	IO545	D3	IO739
A16	IO527	D4	VCC2
A17	IO517	D5	IO687
A18	VCC2	D6	CCLK
A19	VSS	D7	IO677
A20	VCC1	D8	IO665
B2	VSS	D9	VCC2
B3	VCC1	D10	IO619
B4	VCC2	D11	IO611
B5	IO697	D12	IO585, D4
B6	IO683	D13	VCC2
B7	IO671	D14	IO553
B8	IO653	D15	IO537
B9	IO643	D16	IO525
B10	OLVDS5N	D17	IO485
B11	OLVDS5	D18	IO507
B12	ILVDS6N	D19	VCC2
B13	ILVDS6	D20	IO465, D8
B14	IO559	D21	VCC2
B15	IO547, CS0	D22	VSS
B16	VCC2	E1	VCC2
B17	IO519	E2	IO747
B18	IO511	E3	IO745
B19	IO505	E4	IO751
B20	VCC1	E5	IO757
B21	VSS	E6	VCC2
C1	VCC1	E7	IO658, FCK4
C2	VCC1	E8	IO647
C3	VSS	E9	IO625
C4	IO705	E10	VCC2
C5	IO699	E11	IO605
C6	IO679	E12	REFEAST
C7	IO673, D2	E13	IO571
C8	IO655, CHECKN	E14	IO577
C9	IO637	E15	VCC2
C10	OLVDS6N	E16	IO543, FCK3
C11	OLVDS6	E17	IO531, D5
C12	ILVDS5N	E18	IO513, D6

Column	Function	Column	Function
E19	IO447	H3	IO777
E20	IO459	H4	IO779
E21	IO457	H5	VCC2
E22	IO445	H6	IO737
F1	VCC2	H7	IO731
F2	IO763	H8	VCC2
F3	IO753	H9	VCC2
F4	IO727, A0	H10	IO685
F5	IO773	H11	IO627
F6	IO717	H12	IO607
F7	IO720, GCK6, CSOUTN	H13	IO551
F8	IO713, D0	H14	VCC2
F9	IO661	H15	VCC2
F10	IO639	H16	VCC2
F11	IO623	H17	IO473
F12	VCC2	H18	IO407
F13	IO563	H19	IO425
F14	IO539	H20	IO411
F15	IO493, D7	H21	IO413
F16	RESERVED	H22	IO405
F17	IO477	J1	IO799
F18	VCC2	J2	IO803
F19	CON	J3	IO807
F20	VCC2	J4	IO797, A5
F21	IO443, D9	J5	IO819
F22	IO433	J6	VCC2
G1	IO765	J7	IO733
G2	VCC2	J8	VCC2
G3	IO759	J9	IO725
G4	IO767, A3	J10	IO707
G5	IO785	J11	IO645
G6	IO722, GCK7 A1	J12	IO613
G7	IO711	J13	IO533
G8	VCC2	J14	IO482, GCK5
G9	IO693, D1	J15	VCC2
G10	IO651	J16	IO453
G11	VCC2	J17	IO417
G12	IO591	J18	IO385
G13	IO557	J19	VCC2
G14	IO491	J20	IO397, D11
G15	IO487	J21	IO403
G16	IO471	J22	IO387
G17	IO480, GCK4	K1	IO817
G18	IO419, D10	K2	ILVDS8
G19	IO437	K3	ILVDS7
G20	IO427	K4	VCC2
G21	IO431	K5	IO813
G22	IO423	K6	VCC2
H1	IO783, A4	K7	IO793
H2	IO791	K8	IO787

Column	Function	Column	Function
K9	IO771	M15	VCC2
K10	TCK	M16	IO345, D13
K11	IO703	M17	IO339
K12	IO573	M18	REFSOUTH
K13	RESETN	M19	VCC2
K14	IO467	M20	ILVDS3N
K15	IO439	M21	ILVDS4N
K16	VCC2	M22	IO343
K17	IO393	N1	IO851
K18	VCC2	N2	OLVDS7N
K19	IO379	N3	OLVDS8N
K20	OLVDS4N	N4	IO867
K21	OLVDS3N	N5	IO873, A9
K22	IO371	N6	IO871
L1	IO825, A7	N7	VCC2
L2	ILVDS8N	N8	IO923, A12
L3	ILVDS7N	N9	IO951
L4	VCC2	N10	TMS
L5	REFNORTH	N11	IO87
L6	IO823	N12	IO223
L7	IO833	N13	M1
L8	IO857, A8	N14	IO287
L9	IO863	N15	IO305
L10	IO811, A6	N16	IO311
L11	IO805	N17	VCC2
L12	IO567	N18	IO331
L13	IO463	N19	VCC2
L14	IO399	N20	ILVDS3
L15	VCC2	N21	ILVDS4
L16	IO383	N22	IO333
L17	IO377	P1	VCC2
L18	IO365	P2	IO885
L19	IO367	P3	IO883
L20	OLVDS4	P4	VCC2
L21	OLVDS3	P5	VCC2
L22	IO351	P6	IO899
M1	IO831	P7	IO937, A13
M2	OLVDS7	P8	VCC2
M3	OLVDS8	P9	IO1, GCK1, A16
M4	VCC2	P10	IO47
M5	IO847	P11	IO139
M6	IO853	P12	IO159
M7	IO859	P13	IO227
M8	IO865	P14	IO241, GCK3
M9	IO879	P15	VCC2
M10	IO945	P16	IO251
M11	IO83	P17	VCC2
M12	IO323, D14	P18	IO337
M13	IO327	P19	IO313
M14	IO373, D12	P20	IO325

Column	Function	Column	Function
P21	IO319	U6	IO960, GK8, A15
P22	IO317	U7	TRST
R1	IO887	U8	IO13
R2	IO897	U9	VCC2
R3	IO893	U10	VCC2
R4	IO907	U11	IO99
R5	IO891, A10	U12	IO137
R6	IO957	U13	IO153
R7	VCC2	U14	IO175
R8	VCC2	U15	IO233
R9	VCC2	U16	IO240, GCK2
R10	IO65	U17	IO237
R11	VCC2	U18	IO291
R12	VCC2	U19	IO245
R13	IO199	U20	IO271
R14	VCC2	U21	IO279, D15
R15	VCC2	U22	VCC2
R16	IO247	V1	IO927
R17	IO253	V2	IO939
R18	VCC2	V3	IO943
R19	IO297	V4	IO931
R20	IO293	V5	IO33
R21	IO307	V6	IO51
R22	IO299	V7	IO63, A19
T1	IO905, A11	V8	VCC2
T2	IO913	V9	VCC2
T3	IO911	V10	IO97
T4	IO919	V11	REFWEST
T5	IO903	V12	IO125
T6	TDO	V13	IO151
T7	IO953, A14	V14	VCC2
T8	IO7	V15	IO167
T9	IO11	V16	IO177, A22
T10	IO71	V17	VCC2
T11	IO105, A20	V18	IO273
T12	IO143	V19	IO267
T13	VCC2	V20	IO263
T14	IO213	V21	IO265, HDC
T15	VCC2	V22	VCC2
T16	IO231	W1	VSS
T17	M2	W2	VCC2
T18	IO303, INIT	W3	IO947
T19	IO285	W4	VCC2
T20	IO277	W5	IO27
T21	VCC2	W6	IO5
T22	IO283	W7	IO45
U1	IO917	W8	IO57
U2	IO925	W9	IO73
U3	VCC2	W10	IO103
U4	TDI	W11	VCC2
U5	VCC2	W12	IO127

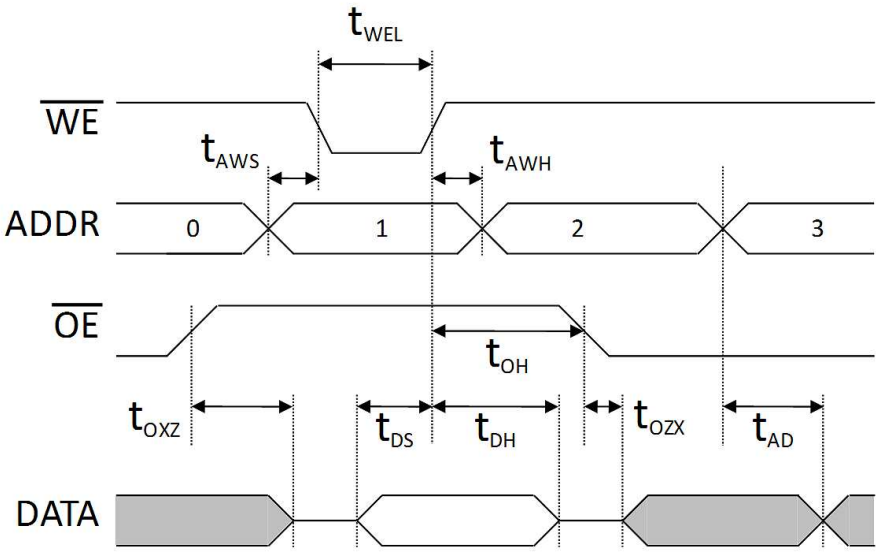
Column	Function	Column	Function
W13	IO145	AB3	VCC1
W14	VCC2	AB4	VSS
W15	IO185	AB5	VCC2
W16	IO197	AB6	VCC2
W17	M0	AB7	IO43
W18	IO207	AB8	IO61, FCK1
W19	VCC22	AB9	IO77
W20	IO257	AB10	IO93
W21	IO259, LDC	AB11	IO111
W22	VSS	AB12	IO133, A21
Y1	VCC1	AB13	IO131
Y2	VCC1	AB14	IO147
Y3	VSS	AB15	IO165
Y4	IO17	AB16	IO180, FCK2
Y5	IO23	AB17	IO193
Y6	IO31	AB18	IO205
Y7	IO37	AB19	VSS
Y8	IO53		
Y9	IO85		
Y10	ILVDS1		
Y11	ILVDS1N		
Y12	OLVDS2		
Y13	OLVDS2N		
Y14	IO157		
Y15	IO171		
Y16	IO187		
Y17	VCC2		
Y18	IO219		
Y19	IO225, OTSN		
Y20	VSS		
Y21	VCC1		
Y22	VCC1		
AA2	VSS		
AA3	VCC1		
AA4	IO19, A17		
AA5	IO25		
AA6	IO39, A18		
AA7	VCC2		
AA8	IO67		
AA9	IO79		
AA10	ILVDS2		
AA11	ILVDS2N		
AA12	OLVDS1		
AA13	OLVDS1N		
AA14	IO163		
AA15	IO173		
AA16	IO191		
AA17	IO203, A23		
AA18	IO217		
AA19	VCC2		
AA20	VCC1		
AA21	VSS		

1.9.3 Notes to Pin Assignments

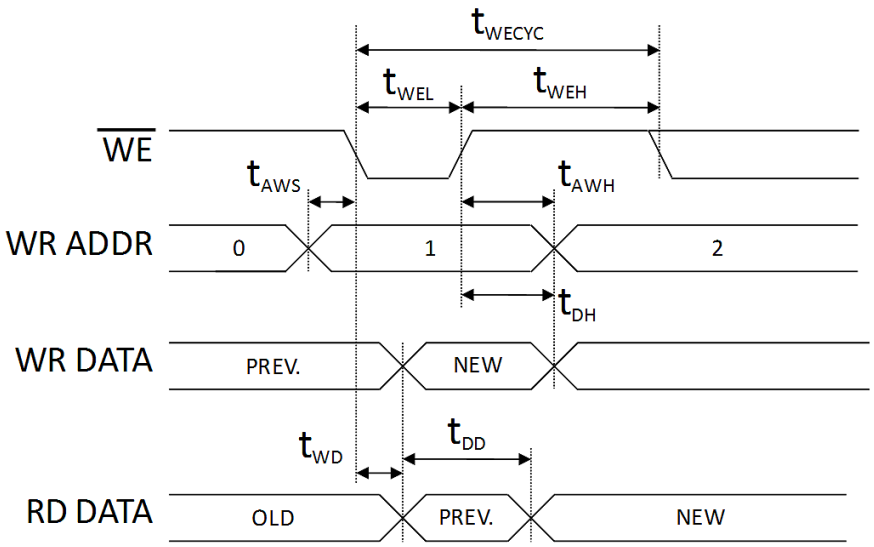
Name	Description	Type
GCK1:GCK8	Global Clock	Input
FCK1:FCK4	Fast Clock	Input
IOx	Programmable I/O The programmable I/Os are dedicated to user's application. Each programmable I/O can independently be configured as input, output or bidirectional I/O. Each I/O is part of an I/O Cluster.	Input/Output
OLVDSx	LVDS Driver OLVDSx where 'x' is the LVDS channel number (1 < x < 8)	Output
OLVDSxN	Complimentary LVDS Driver OLVDSxN where 'x' is the LVDS channel number (1 < x < 8)	Output
ILVDSx	LVDS Receiver ILVDSx where 'x' is the LVDS channel number (1 < x < 8)	Input
ILVDSxN	Complimentary LVDS Receiver ILVDSxN where 'x' is the LVDS channel number (1 < x < 8)	Input
VDD	Core power supply VDD is the power supply input for the ATF280F core	
VCC	I/O Power Supply VCC is the power supply input for the programmable I/Os. Each I/O cluster has dedicated VCC source.	
REF	LVDS Reference voltage REF is the reference voltage for LVDS buffer operations. Each LVDS cluster has dedicated VREF source.	Input
VSS	Ground (Negative Supply)	

1.10 TIMING DIAGRAMS

SINGLE PORT WRITE/READ (ASYNCHRONOUS FREERAM)

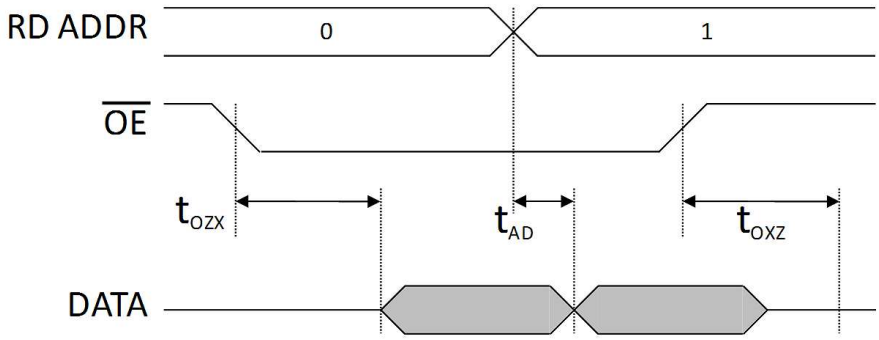


DUAL-PORT WRITE WITH READ (ASYNCHRONOUS FREERAM)

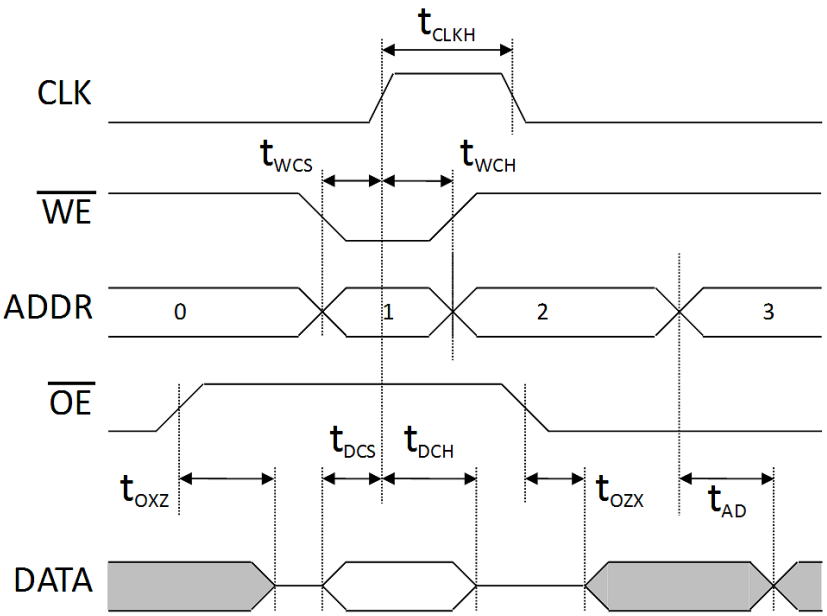


RD ADDR = WR ADDR 1

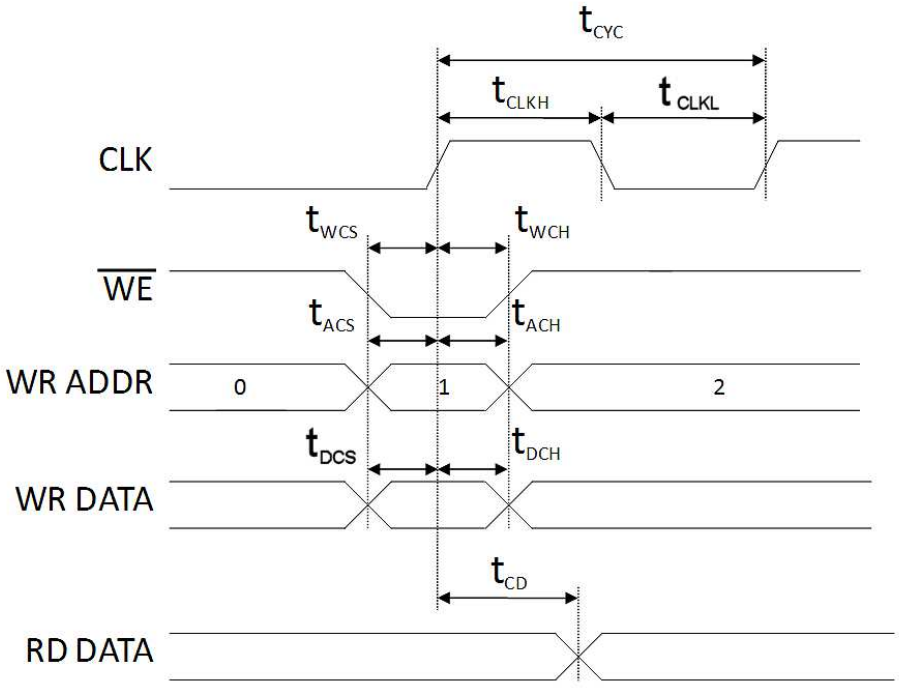
DUAL-PORT READ (ASYNCHRONOUS FREERAM)



SINGLE PORT WRITE/READ (SYNCHRONOUS FREERAM)

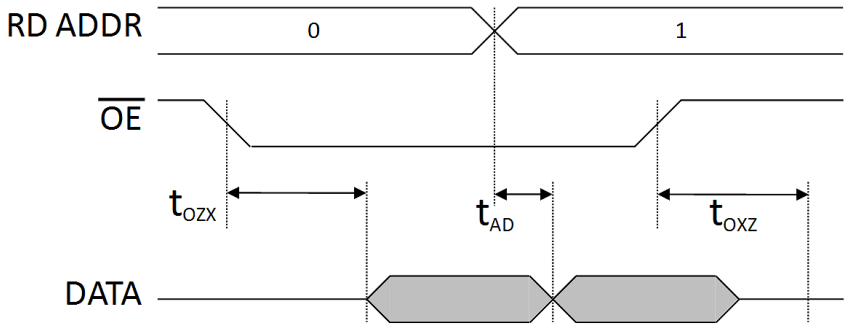


DUAL-PORT WRITE WITH READ (SYNCHRONOUS FREERAM)

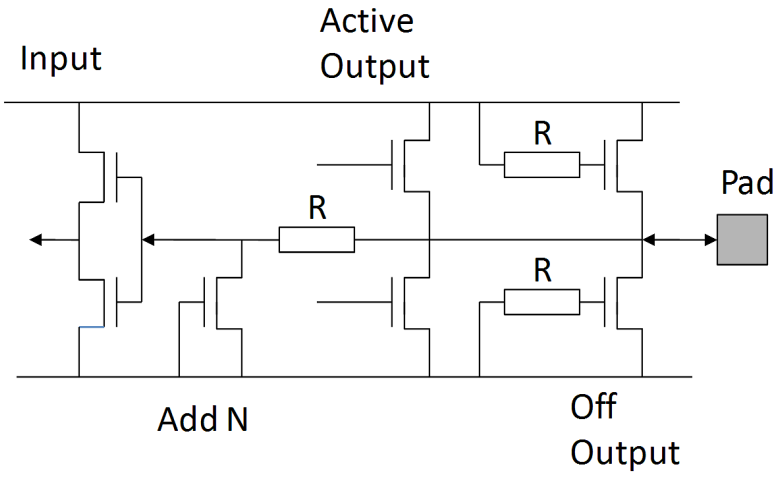


RD ADDR = WR ADDR 1

DUAL-PORT READ (SYNCHRONOUS FREERAM)



1.11 I/O PROTECTION NETWORK



NOTES:
1. The Active/Off ratio depends on the output strength.
2. IO33: R ~460Ω + with additional N.

2 REQUIREMENTS

2.1 GENERAL

The complete requirements for procurement of the components specified herein are as stated in this specification and the ESCC Generic Specification. Permitted deviations from the Generic Specification, applicable to this specification only, are listed below.

Permitted deviations from the Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESCC requirement and do not affect the component's reliability, are listed in the appendices attached to this specification.

2.1.1 Deviations from the Generic Specification

2.1.1.1 Deviations from Screening Tests

High Temperature Reverse Bias Burn-in shall not be performed.

2.2 MARKING

The marking shall be in accordance with the requirements of ESCC Basic Specification No. 21700 and as follows.

As a minimum the information to be marked on the component shall be:

(a) The ESCC qualified components symbol (for ESCC qualified components only).
(b) The ESCC Component Number.
(c) Traceability information.

2.3 ELECTRICAL MEASUREMENTS AT ROOM, HIGH AND LOW TEMPERATURES

Electrical measurements shall be performed at room, high and low temperatures. Consolidated notes are given after the tables.

2.3.1 Room Temperature Electrical Measurements

The measurements shall be performed at T_{amb} = +22 ±3 ºC.

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions (Note 1) $1.65V < V_{DD} < 1.95V$ $3V < V_{CC} < 3.6V$	Limits		Units
				Min	Max	
Functional Test 1	-	3014	V_{DD} = 1.65V V_{CC} = 3V	-	-	-
Functional Test 2	-	3014	V_{DD} = 1.8V V_{CC} = 3.3V	-	-	-
Functional Test 3	-	3014	V_{DD} = 1.95V V_{CC} = 3.6V	-	-	-
Stand-by Supply Current 1	I_{CCSB1}	3005	After reset, cells not configured V_{CC} = 3.6V	-	200	mA
Stand-by Supply Current 2	I_{CCSB2}	3005	All cells configured, no floating nodes V_{CC} = 3.6V	-	50	mA
Low Level Input Current	I_{IL}	3009	Without pull-up $V_{IN} = V_{SS}$	-1	1	µA
	I_{ILPU}	3009	Pull-up 10kΩ CON	-500	-	µA
High Level Input Current	I_{IH}	3010	Without pull-down $V_{IN} = V_{CC}$ max	-1	1	µA
	I_{IHPD}	3010	Pull-down 20kΩ I/O	-	240	µA
Low Level Tri-state Output Leakage Current	I_{OZL}	3020	Without pull-up $V_{IN} = V_{SS}$	-1	1	µA
	I_{OZLPU}	3020	Pull-up 20kΩ I/O	-220	-	µA

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions (Note 1) $1.65V < V_{DD} < 1.95V$ $3V < V_{CC} < 3.6V$	Limits		Units
				Min	Max	
High Level Tri-state Output Leakage Current	I_{OZH}	3021	Without pull-down $V_{IN} = V_{CC}$ max	-1	1	µA
	I_{OZHPD}	3021	Pull-down 20kΩ I/O	-	240	µA
Cold Sparing Input Leakage Current	I_{ICS}	-	$V_{CC} = V_{DD} = 0V$ $V_{IN} = 3.6V$	-1	1	µA
Cold Sparing Output Leakage Current	I_{OCS}	-	$V_{CC} = V_{DD} = 0V$ $V_{OUT} = 3.6V$	-1	1	µA
Low Level Input Voltage	V_{IL}	-	-	-0.3	0.3* V_{CC}	V
High Level Input Voltage	V_{IH}	-	-	0.7* V_{CC}	V_{CC} + 0.8	V
Low Level Output Voltage	V_{OL}	3006	I_{OL} = 4, 10, 14 mA	-	0.4	V
High Level Output Voltage	V_{OH}	3006	I_{OH} = -4, -10, -14 mA	V_{CC} - 0.4	-	V
LVDS Characteristics						
Output Differential Voltage	V_{OD}		R_{load} = 100Ω	247	454	mV
Output Offset Voltage	V_{OS}		R_{load} = 100Ω	1125	1375	mV
Operating Frequency (Note 2)	f		V_{CC} = 3.3V ±0.3V	-	50	MHz
Clock Signal Duty Cycle (Note 2)	Clock		f = 50MHz	45	55	%
Fall Time 80-20% (Note 2)	t_f		R_{load} = 100Ω	445	838	ps
Rise Time 20-80% (Note 2)	t_r		R_{load} = 100Ω	445	841	ps
Propagation Delay 1 (Note 2)	t_{p1}		R_{load} = 100Ω	1120	2120	ps
Propagation Delay 2 (Note 2)	t_{p2}		C_{out} = 50 pF, V_{CC} = 3.3V ±0.3V	0.7	2.4	ns
Duty Cycle Skew (Note 2)	t_{sk1}		R_{load} = 100Ω	0	80	ps
Channel to Channel Skew (same edge) (Note 2)	t_{sk2}		R_{load} = 100Ω	0	50	ps
Input Differential Voltage (Note 2)	V_{ID}			200	600	mV
Input Offset Range (Note 2)	V_{CM}			0.4	2000	mV
Duty Cycle Distortion (Note 2)	t_{skew}		C_{out} = 50 pF	-	500	ps

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions (Note 1) $1.65V < V_{DD} < 1.95V$ $3V < V_{CC} < 3.6V$	Limits		Units
				Min	Max	
AC Characteristics – Asynchronous Mode (Note 2)						
Write, $\overline{WE}$ $\overline{WE}$ min pulse width (high and low)	t_{WEL}, t_{WEH}			-	1.7	ns
Write, $\overline{WE}$ → AIN | A setup time of address input before low transition at the $\overline{WE}$ input	t_{AWS}			-	4.2	ns
Write, $\overline{WE}$ → AIN | A hold time of address input before high transition at the $\overline{WE}$ input	t_{AWH}			-	1.7	ns
Write, $\overline{WE}$ → DIN | D setup time of data input before rising transition at the $\overline{WE}$ input	t_{DS}			-	0	ns
Write, $\overline{WE}$ → DIN | D hold time of data input before rising transition at the $\overline{WE}$ input	t_{DH}			-	0	ns
Write / Read, DIN → DOUT, propagation delay between DIN and DOUT on double port RAM when AIN = AOUT	t_{DD}			-	6.4	ns
Hold time from rising edge of $\overline{WE}$ input to falling edge of $\overline{OE}$	t_{OH}			-	0	ns
Propagation delay between falling edge of $\overline{WE}$ and previous DOUT bit	t_{WD}			-	7.6	ns
Read, AIN → DOUT, propagation delay from AIN to DOUT	t_{AD}			-	4.9	ns
Read, $\overline{OE}$ → DOUT, propagation delay from $\overline{OE}$ to DOUT for a transition from Z to 0|1	t_{OZX}			-	2.9	ns
Read, $\overline{OE}$ → DOUT, propagation delay from $\overline{OE}$ to DOUT for a transition from 0|1 to Z	t_{OXZ}			-	2.9	ns
AC Characteristics – Synchronous Mode (Note 2)						
Write, CLK, CLK min pulse width (high and low)	t_{CLKL}, t_{CLKH}			-	1.2	ns
Write, $\overline{WE}$ → CLK, setup time of $\overline{WE}$ input before active transition at the CLK input	t_{WCS}			-	2.7	ns

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions (Note 1) $1.65V < V_{DD} < 1.95V$ $3V < V_{CC} < 3.6V$	Limits		Units
				Min	Max	
Write, $\overline{WE}$ → CLK, hold time of we input before active transition at the CLK input	t_{WCH}			-	0	ns
Write, AIN → CLK, setup time of address input before active transition at the CLK input	t_{ACS}			-	3.2	ns
Write, AIN → CLK, hold time of address input before active transition at the CLK input	t_{ACH}			-	3.3	ns
Write, DIN → CLK, setup time of data input before active transition at the CLK input	t_{DCS}			-	1.5	ns
Write, DIN → CLK, hold time of data input before active transition at the CLK input	t_{DCH}			-	0	ns
Write / Read, DIN → CLK, hold time of data input before active transition at the CLK input	t_{CD}			-	5.8	ns
Read, AOUT → DOUT, propagation delay from AOUT to DOUT	t_{AD}			-	4.9	ns
Read, $\overline{OE}$ → DOUT, propagation delay from $\overline{OE}$ to DOUT for a transition from Z to 0|1	t_{OZX}			-	2.9	ns
Read, $\overline{OE}$ → DOUT, propagation delay from $\overline{OE}$ to DOUT for a transition from 0|1 to Z	t_{OXZ}			-	2.9	ns

NOTES:
1. Unless otherwise specified, all inputs and outputs shall be tested for each characteristic. Inputs not under test shall be $V_{IN} = V_{SS}$ or V_{CC} and outputs not under test shall be open. $V_{SS} = 0V$.
2. Parameter is guaranteed by simulation, but not tested.

2.3.2 High and Low Temperatures Electrical Measurements

Unless otherwise specified, the measurements shall be performed at T_{amb} = +125 (+0 -5) ºC and T_{amb} = -55 (+5 -0) ºC. Unless otherwise specified the characteristics, test methods, conditions and limits shall be the same as specified for Room Temperature Electrical Measurements.

2.4 PARAMETER DRIFT VALUES

Unless otherwise specified the measurements shall be performed at T_{amb} = +22 ±3 ºC.

The test methods and test conditions shall be as per the corresponding test defined in Room Temperature Electrical Measurements.

The drift values (Δ) shall not be exceeded for each characteristic specified. The corresponding absolute limit values for each characteristic shall not be exceeded.

Characteristics	Symbols	Limits			Units
		Drift Value Δ	Absolute		
			Min	Max	
Stand-by Supply Current 1	I_{CCSB1}	20	-	200	mA
Low Level Input Current	I_{IL}	±0.1	-1	1	µA
High Level Input Current	I_{IH}	±0.1	-1	1	µA
Output Leakage Current Third State, Low Level Applied	I_{OZL}	±0.1	-1	1	µA
Output Leakage Current Third State, High Level Applied	I_{OZH}	±0.1	-1	1	µA
Low Level Output Voltage	V_{OL}	±100	-	400	mV
High Level Output Voltage	V_{OH}	±0.1	V_{CC} - 0.4	-	V

NOTES:

1. Unless otherwise specified all inputs and outputs shall be tested for each characteristic.

2.5 INTERMEDIATE AND END-POINT ELECTRICAL MEASUREMENTS

Unless otherwise specified the measurements shall be performed at T_{amb} = +22 ±3 ºC. Unless otherwise specified the characteristics, test methods, conditions and limits shall be the same as specified for Room Temperature Electrical Measurements.

2.6 POWER BURN-IN CONDITIONS

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	T_{amb}	+125 (+0 -5)	^{o}C
I/O Positive Supply Voltage	V_{CC}	3.7 (+0, -0.5)	V
Core Positive Supply Voltage	V_{DD}	1.95 (+0 -0.5)	V
Negative Supply Voltage	V_{SS}	0	V

NOTES:
1. During Burn-in and Operating Life, the FPGA is configured and then stimuli are applied.
2. Test set-up shall be maintained within the Manufacturer's PID.

2.7 OPERATING LIFE CONDITIONS

Unless otherwise specified the conditions shall be as specified for Power Burn-in.

2.8 TOTAL DOSE RADIATION TESTING

2.8.1 Bias Conditions and Total Dose Level for Total Dose Radiation Testing

Continuous bias shall be applied during irradiation testing as specified below.

The total dose level applied shall be as specified in the component type variant information herein or in the Purchase Order.

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	T_{amb}	+22 ±3	^{o}C
Inputs M0, M1, M2	V_{IN}	V_{SS}	V
All I/O Inputs/Outputs	V_{IN} / V_{OUT}	V_{SS}	V
I/O Positive Supply Voltage	V_{CC}	3.7 (+0, -0.5)	V
Core Positive Supply Voltage	V_{DD}	1.95 (+0 -0.5)	V
Negative Supply Voltage	V_{SS}	0	V

NOTES:
1. Annealing shall be performed with the static bias conditions for a duration of 24 hours at the specified t_{amb} followed by 168 hours minimum at a temperature of +100 (+0 -3) °C.
2. Test set-up shall be maintained within the Manufacturer's PID.

2.8.2 Electrical Measurements for Total Dose Radiation Testing

Prior to irradiation testing the devices shall have successfully met Room Temperature Electrical Measurements specified herein.

Unless otherwise specified the measurements shall be performed at T_{amb} = +22 ±3 ºC.

The test methods and test conditions shall be as per the corresponding test defined in Room Temperature Electrical Measurements.