INTEGRATED CIRCUITS, SILICON, 32-BIT SPARC PROCESSOR

BASED ON TYPE AT697F

ESCC Detail Specification No. 9512/004

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1 GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics and test and inspection data for the component type variants and/or the range of components specified below. It supplements the requirements of, and shall be read in conjunction with, the ESCC Generic Specification listed under Applicable Documents.

1.2 APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:

(a) ESCC Generic Specification No. 9000.
(b) MIL-STD-883, Test Method Standard for Microcircuits.

1.3 TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESCC Basic Specification No. 21300 shall apply. Additional, specific, terms and abbreviations are as follows:

- CL = Column Address Strobe Latency.
- Natural Skew = the standard clock tree skew of the device, achieved by setting pins SKEW[1:0] to 00.
- Medium Skew = an increased level of clock tree skew, achieved by setting pins SKEW[1:0] to 01.
- Maximum Skew = the highest level of clock tree skew, achieved by setting pins SKEW[1:0] to 10.

1.4 THE ESCC COMPONENT NUMBER AND COMPONENT TYPE VARIANTS

1.4.1 The ESCC Component Number

The ESCC Component Number shall be constituted as follows:

Example: 951200401R

- Detail Specification Reference : 9512004
- Component Type Variant Number : 01 (as required)
- Total Dose Radiation Level Letter : R (as required)

1.4.2 Component Type Variants

The component type variants applicable to this specification are as follows:

Variant Number	Based on Type	Case	Lead/Terminal Material and Finish	Weight max (g)	Total Dose Radiation Level Letter (Note 3)
01	AT697F	MQFP-F256	D2 (Note 1)	14	R [100 kRAD (Si)]
02	AT697F	LGA-349	Note 2	7	R [100 kRAD (Si)]

NOTES:

1. The lead material and finish shall be in accordance with the requirements of ESCC Basic Specification No. 23500.
2. The terminal material shall be tungsten and the finish shall be 0.03µm to 0.1µm gold plating over 3.2µm minimum nickel underplating.
3. Total dose radiation level letters are defined in ESCC Basic Specification No. 22900. If an alternative radiation test level is specified in the Purchase Order the letter shall be changed accordingly.

1.5 MAXIMUM RATINGS

The maximum ratings shall not be exceeded at any time during use or storage. Functional performance for extended periods at the maximum ratings may adversely affect device reliability.

The maximum ratings shall only be exceeded during testing to the extent specified in this specification and when stipulated in the Test Methods and Procedures of the applicable ESCC generic specification.

Characteristics	Symbols	Maximum Ratings	Units	Remarks
Supply Voltage	V_{CC1} V_{CC2}	-0.3 to 2 -0.3 to 4	V	Notes 1, 2
Input Voltage Range	V_{IN}	-0.5 to 4	V	Notes 2, 3
Input Current	I_{IN}	±40	mA	Each Input pin
Device Power Dissipation	P_D	1.3	W	-
Operating Temperature Range	T_{op}	-55 to +125	°C	T_{amb}
Storage Temperature Range	T_{stg}	-65 to +150	°C	
Junction Temperature	T_j	+175	°C	
Thermal Resistance, Junction-to-Case	$R_{th(j-c)}$	3	°C/W	-
Soldering Temperature Variant 01 Variant 02	T_{sol}	 +300 +220	°C	 Note 4 -

NOTES:

1. V_{CC1} is the core supply voltage and V_{CC2} is the interface supply voltage.
2. With reference to V_{SS} = 0V.
3. Applicable for all inputs. Input current limited to I_{IC} = ±10mA.
4. Duration 10 seconds maximum at a distance of not less than 1.6 mm from the device body and the same lead shall not be re-soldered until 3 minutes have elapsed.

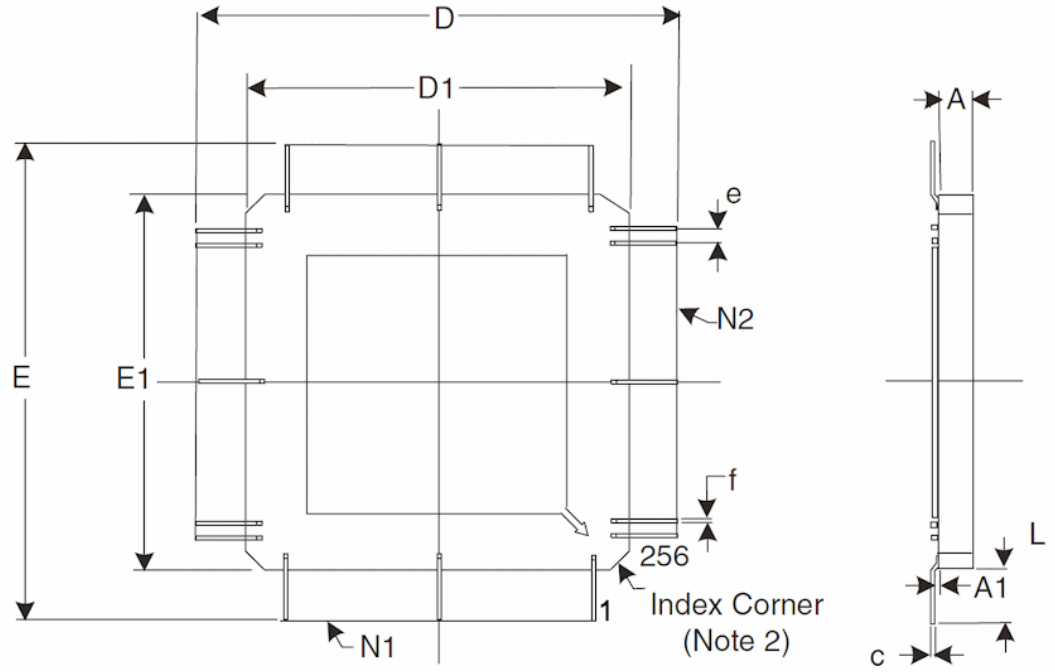
1.6 HANDLING PRECAUTIONS

These devices are susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacture, testing, packaging, shipment and any handling.

These components are categorised as Class 2 per ESCC Basic Specification No. 23800 with a Minimum Critical Path Failure Voltage of 2000 Volts.

1.7 PHYSICAL DIMENSIONS AND TERMINAL IDENTIFICATION

1.7.1 Multilayer Quad Flat Package (MQFP-F256) – 256 Flat Leads



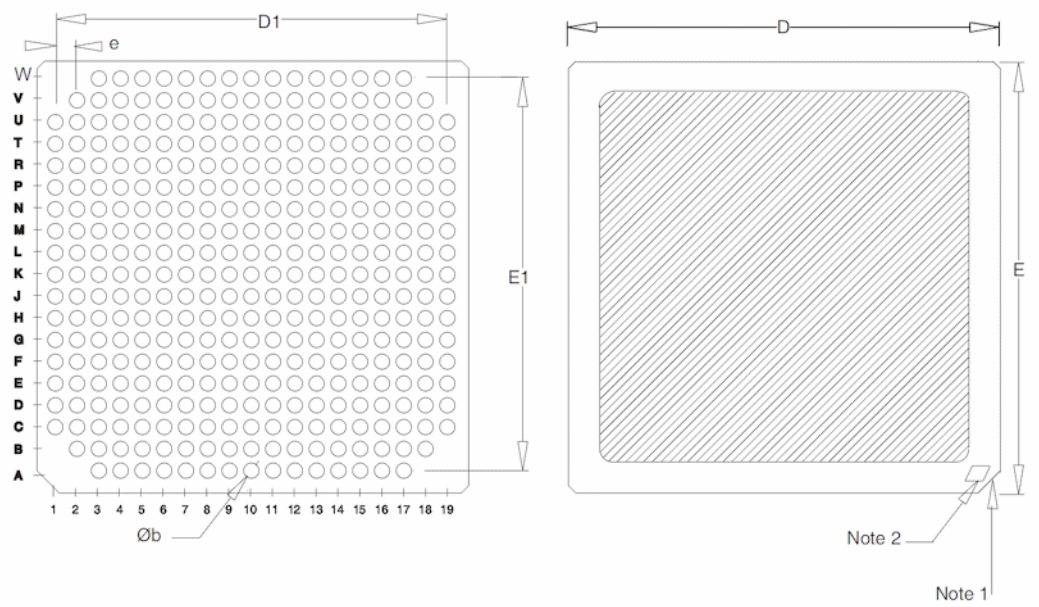
Symbols	Dimensions mm		Notes
	Min	Max	
A	2.06	2.56	
A1	0.05	0.36	
c	0.1	0.2	1
D/E	53.23	55.74	
D1/E1	36.83	37.34	
e	0.508 BSC		1
f	0.15	0.25	1
L	8.2	9.2	1
N1/N2	31.9	32.11	3

NOTES:

1. Applies to all leads.
2. Terminal identification is specified by reference to the index corner as shown.
3. Each side (64 leads per side); this dimension is derived from 63 x dimension e.

1.7.2 Land Grid Array (LGA–349) – 349 Pads

BOTTOM VIEW TOP VIEW

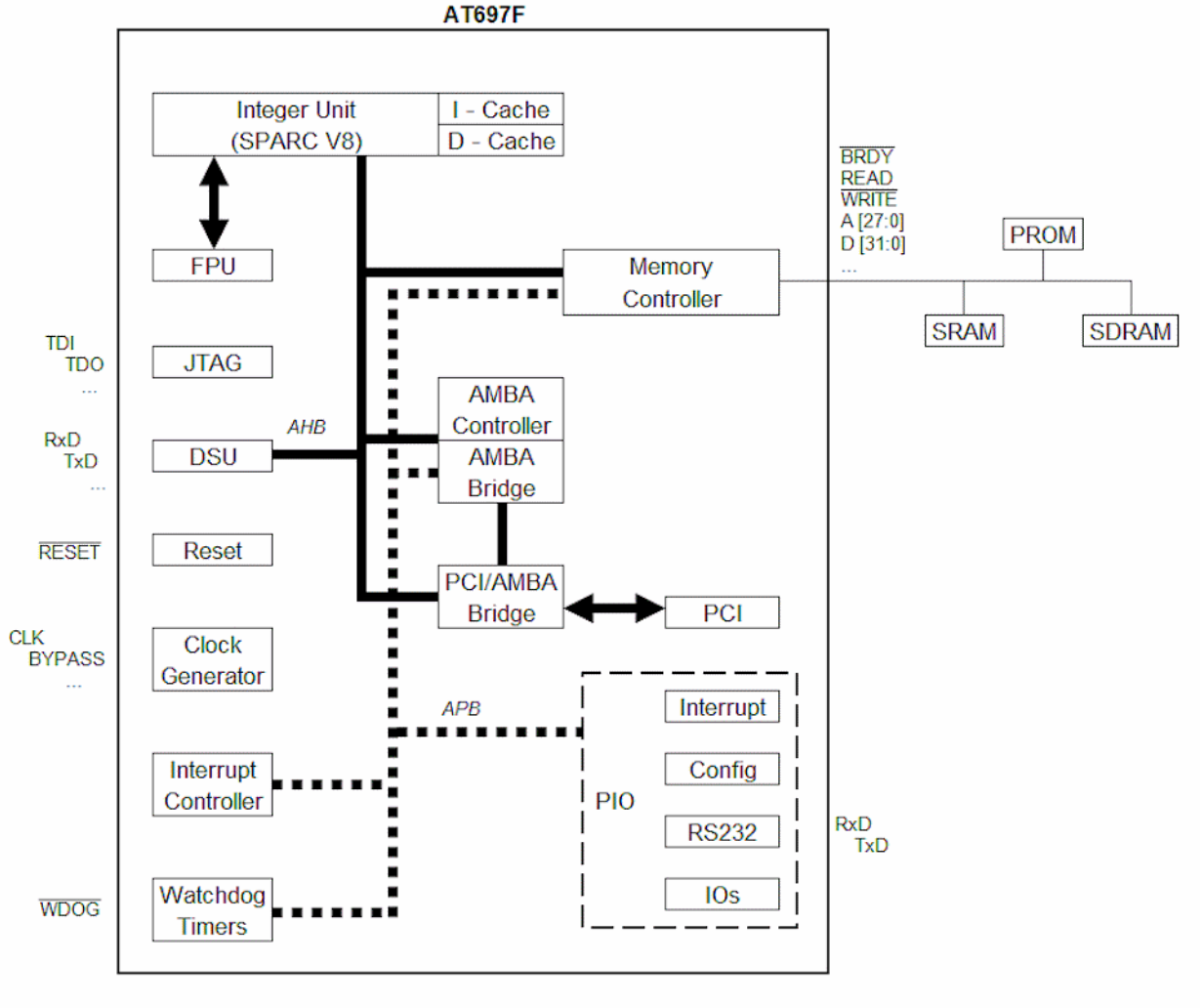


SIDE VIEW

Symbols	Dimensions mm		Notes
	Min	Max	
A	-	3.24	
A1	2.27	2.77	
Øb	0.81	0.91	3
D/E	24.85	25.15	
D1/E1	22.86 BSC		
e	1.27 BSC		3

NOTES:
1. Index corner. Terminal identification is specified by reference to the index corner as shown.
2. A terminal identification shall be located at the index corner as shown.
3. Applies to all pads.

1.8 FUNCTIONAL DIAGRAM



1.9 PIN ASSIGNMENT AND DESCRIPTION

1.9.1 Pin Out for Variant 01 (MQFP-F256)

Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name
1	VCC33 (Note 1)	41	$\overline{\text{ROMS}}$[0]	81	CB[0]
2	$\overline{\text{REQ}}$	42	$\overline{\text{ROMS}}$[1]	82	CB[1]
3	$\overline{\text{GNT}}$	43	$\overline{\text{RWE}}$[0]	83	CB[2]
4	PCI_CLK	44	$\overline{\text{RWE}}$[1]	84	CB[3]
5	$\overline{\text{PCI\_RST}}$	45	$\overline{\text{RWE}}$[2]	85	VCC33 (Note 1)
6	$\overline{\text{SDCS}}$[0]	46	$\overline{\text{RWE}}$[3]	86	CB[4]
7	VSS	47	$\overline{\text{RAMOE}}$[0]	87	CB[5]
8	VDD18 (Note 2)	48	$\overline{\text{RAMOE}}$[1]	88	CB[6]
9	$\overline{\text{SDCS}}$[1]	49	$\overline{\text{RAMOE}}$[2]	89	CB[7]
10	$\overline{\text{SDWE}}$	50	$\overline{\text{RAMOE}}$[3]	90	D[0]
11	$\overline{\text{SDRAS}}$	51	$\overline{\text{RAMOE}}$[4]	91	VCC33 (Note 1)
12	VSS	52	$\overline{\text{RAMS}}$[0]	92	D[1]
13	VSS	53	VCC33 (Note 1)	93	D[2]
14	$\overline{\text{SDCAS}}$	54	$\overline{\text{RAMS}}$[1]	94	D[3]
15	VCC33 (Note 1)	55	$\overline{\text{RAMS}}$[2]	95	D[4]
16	SDDQM[0]	56	$\overline{\text{RAMS}}$[3]	96	D[5]
17	SDDQM[1]	57	VSS	97	D[6]
18	SDDQM[2]	58	VDD18 (Note 2)	98	*Reserved* (Note 3)
19	SDDQM[3]	59	$\overline{\text{RAMS}}$[4]	99	VCC33 (Note 1)
20	SDCLK	60	PIO[0]	100	D[7]
21	$\overline{\text{BRDY}}$	61	PIO[1]	101	D[8]
22	$\overline{\text{BEXC}}$	62	PIO[2]	102	D[9]
23	VSS	63	PIO[3]	103	D[10]
24	VSS	64	PIO[4]	104	D[11]
25	DSUEN	65	PIO[5]	105	D[12]
26	DSUTX	66	PIO[6]	106	VCC33 (Note 1)
27	DSURX	67	VCC33 (Note 1)	107	D[13]
28	DSUBRE	68	PIO[7]	108	D[14]
29	DSUACT	69	PIO[8]	109	D[15]
30	$\overline{\text{TRST}}$	70	PIO[9]	110	D[16]
31	TCK	71	VSS	111	D[17]
32	TMS	72	VDD18 (Note 2)	112	VSS
33	VSS	73	PIO[10]	113	D[18]
34	TDI	74	PIO[11]	114	VCC33 (Note 1)
35	TDO	75	*Reserved* (Note 3)	115	D[19]
36	$\overline{\text{WRITE}}$	76	PIO[12]	116	D[20]
37	READ	77	PIO[13]	117	D[21]
38	$\overline{\text{OE}}$	78	PIO[14]	118	D[22]
39	$\overline{\text{IOS}}$	79	PIO[15]	119	D[23]
40	VCC33 (Note 1)	80	VCC33 (Note 1)	120	D[24]
121	VSS	163	A[23]	205	$\overline{\text{C/BE}}$[0]

Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name
122	VDD18 (Note 2)	164	A[24]	206	VSS
123	VCC33 (Note 1)	165	A[25]	207	VCC33 (Note 1)
124	D[25]	166	A[26]	208	A/D[8]
125	D[26]	167	A[27]	209	A/D[9]
126	D[27]	168	$\overline{\text{WDOG}}$	210	A/D[10]
127	D[28]	169	$\overline{\text{ERROR}}$	211	A/D[11]
128	D[29]	170	VCC33 (Note 1)	212	VCC33 (Note 1)
129	D[30]	171	$\overline{\text{RESET}}$	213	A/D[12]
130	VCC33 (Note 1)	172	*Reserved* (Note 3)	214	A/D[13]
131	D[31]	173	LOCK	215	A/D[14]
132	N/C (Note 4)	174	SKEW[1]	216	A/D[15]
133	A[0]	175	SKEW[0]	217	VCC33 (Note 1)
134	A[1]	176	BYPASS	218	$\overline{\text{C/BE}}$[1]
135	VSS	177	VSS_PLL	219	PAR
136	VDD18 (Note 2)	178	N/C (Note 4)	220	$\overline{\text{SERR}}$
137	A[2]	179	VDD_PLL (Note 2)	221	$\overline{\text{PERR}}$
138	A[3]	180	CLK	222	VCC33 (Note 1)
139	A[4]	181	VCC33 (Note 1)	223	$\overline{\text{PCI\_LOCK}}$
140	VCC33 (Note 1)	182	$\overline{\text{AREQ}}$[3]	224	$\overline{\text{STOP}}$
141	A[5]	183	$\overline{\text{AGNT}}$[3]	225	$\overline{\text{DEVSEL}}$
142	A[6]	184	$\overline{\text{AREQ}}$[2]	226	$\overline{\text{TRDY}}$
143	A[7]	185	VSS	227	VCC33 (Note 1)
144	A[8]	186	VDD18 (Note 2)	228	$\overline{\text{IRDY}}$
145	A[9]	187	$\overline{\text{AGNT}}$[2]	229	$\overline{\text{FRAME}}$
146	A[10]	188	$\overline{\text{AREQ}}$[1]	230	VSS
147	VCC33 (Note 1)	189	VCC33 (Note 1)	231	$\overline{\text{C/BE}}$[2]
148	A[11]	190	$\overline{\text{AGNT}}$[1]	232	A/D[16]
149	A[12]	191	$\overline{\text{AREQ}}$[0]	233	VCC33 (Note 1)
150	A[13]	192	$\overline{\text{AGNT}}$[0]	234	A/D[17]
151	A[14]	193	A/D[0]	235	A/D[18]
152	A[15]	194	VCC33 (Note 1)	236	A/D[19]
153	A[16]	195	A/D[1]	237	$\overline{\text{SYSEN}}$
154	VCC33 (Note 1)	196	A/D[2]	238	A/D[20]
155	A[17]	197	A/D[3]	239	VCC33 (Note 1)
156	A[18]	198	A/D[4]	240	A/D[21]
157	A[19]	199	VSS	241	A/D[22]
158	A[20]	200	VDD18 (Note 2)	242	A/D[23]
159	A[21]	201	VCC33 (Note 1)	243	IDSEL
160	A[22]	202	A/D[5]	244	$\overline{\text{C/BE}}$[3]
161	VSS	203	A/D[6]	245	VCC33 (Note 1)
162	VCC33 (Note 1)	204	A/D[7]	246	A/D[24]
247	A/D[25]	252	VCC33 (Note 1)	-	-

Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name
248	A/D[26]	253	A/D[28]	-	-
249	VSS	254	A/D[29]	-	-
250	VDD18 (Note 2)	255	A/D[30]	-	-
251	A/D[27]	256	A/D[31]	-	-

NOTES:
1. V_{CC2} supply voltage, 3.3V.
2. V_{CC1} supply voltage, 1.8V.
3. *Reserved* pins shall not be driven to any voltage.
4. N/C = Not Connected.

1.9.2 Pin Out for Variant 02 (LGA-349)

Column Numbers	Rows						
	A	B	C	D	E	F	G
1	-	-	VDD18 (Note 1)	VSS18	PIO[6]	PIO[1]	$\overline{\text{RAMS}}$[1]
2	-	VSS18	VDD18 (Note 1)	PIO[0]	N/C (Note 2)	PIO[4]	$\overline{\text{RAMS}}$[2]
3	VDD18 (Note1)	VDD18 (Note 1)	VSS18	VCC33 (Note 3)	PIO[2]	N/C (Note 2)	$\overline{\text{RAMOE}}$[3]
4	VSS18	VDD18 (Note 1)	PIO[9]	N/C (Note 2)	PIO[5]	PIO[3]	$\overline{\text{RAMS}}$[4]
5	N/C (Note 2)	N/C (Note 2)	PIO[11]	N/C (Note 2)	N/C (Note 2)	VSS33	$\overline{\text{RAMOE}}$[1]
6	PIO[13]	PIO[10]	VCC33 (Note 3)	*Reserved* (Note 4)	CB[0]	N/C (Note 2)	VSS33
7	CB[1]	VSS33	N/C (Note 2)	PIO[15]	VSS33	PIO[12]	PIO[7]
8	CB[6]	CB[4]	D[2]	VCC33 (Note 3)	CB[7]	CB[2]	PIO[8]
9	D[3]	N/C (Note 2)	D[1]	VSS33	D[6]	VCC33 (Note 3)	CB[3]
10	D[8]	D[5]	VCC33 (Note 3)	VSS33	*Reserved* (Note 4)	D[10]	D[4]
11	D[12]	VSS33	VCC33 (Note 3)	D[13]	D[7]	D[15]	N/C (Note 2)
12	D[17]	D[18]	D[11]	VSS33	D[14]	D[16]	D[19]
13	D[21]	D[23]	VCC33 (Note 3)	VCC33 (Note 3)	VSS33	VSS33	A[1]
14	D[25]	N/C (Note 2)	D[22]	D[27]	N/C (Note 2)	VSS33	A[3]
15	D[30]	N/C (Note 2)	D[26]	D[29]	N/C (Note 2)	N/C (Note 2)	A[12]
16	VSS18	VSS18	D[28]	VCC33 (Note 3)	N/C (Note 2)	N/C (Note 2)	A[6]
17	VDD18 (Note 1)	VDD18 (Note 1)	VSS18	D[31]	N/C (Note 2)	A[7]	VSS33
18	-	VSS18	VDD18 (Note 1)	VCC33 (Note 3)	A[0]	A[4]	A[8]
19	-	-	VDD18 (Note 1)	VSS18	A[2]	VSS33	A[9]

		Rows (Continued)						
		H	J	K	L	M	N	P
Column Numbers	1	$\overline{\text{RAMOE}}$[0]	VSS33	READ	DSUACT	$\overline{\text{BEXC}}$	VCC33 (Note 3)	$\overline{\text{SDWE}}$
	2	$\overline{\text{RAMOE}}$[2]	$\overline{\text{ROMS}}$[1]	TCK	DSURX	SDCLK	VSS33	PCI_CLK
	3	VCC33 (Note 3)	$\overline{\text{ROMS}}$[0]	TDI	DSUTX	DSUBRE	SDDQM[1]	VSS33
	4	$\overline{\text{RAMOE}}$[4]	$\overline{\text{RWE}}$[0]	TDO	DSUEN	SDDQM[2]	N/C (Note 2)	$\overline{\text{SDCS}}$[0]
	5	$\overline{\text{RWE}}$[1]	$\overline{\text{WRITE}}$	VSS33	TMS	N/C (Note 2)	SDDQM[3]	$\overline{\text{SDCAS}}$
	6	$\overline{\text{RWE}}$[3]	$\overline{\text{RWE}}$[2]	$\overline{\text{IOS}}$	VSS33	VSS33	$\overline{\text{GNT}}$	A/D[24]
	7	$\overline{\text{RAMS}}$[0]	N/C (Note 2)	$\overline{\text{TRST}}$	SDDQM[0]	VSS33	VCC33 (Note 3)	A/D[30]
	8	$\overline{\text{RAMS}}$[3]	VCC33 (Note 3)	$\overline{\text{OE}}$	$\overline{\text{BRDY}}$	VCC33 (Note 3)	A/D[21]	A/D[18]
	9	CB[5]	PIO[14]	VSS33	$\overline{\text{SDRAS}}$	A/D[22]	A/D[16]	A/D[17]
	10	D[9]	D[0]	N/C (Note 2)	A/D[14]	VSS33	$\overline{\text{PERR}}$	$\overline{\text{IRDY}}$
	11	D[20]	A[5]	A[16]	N/C (Note 2)	A/D[12]	A/D[9]	A/D[15]
	12	D[24]	A[14]	A[26]	VDD_PLL (Note 1)	$\overline{\text{AGNT}}$[3]	A/D[1]	A/D[8]
	13	N/C (Note 2)	VCC33 (Note 3)	A[21]	N/C (Note 2)	N/C (Note 2)	VSS33	A/D[5]
	14	A[10]	VCC33 (Note 3)	A[27]	LOCK	SKEW[1]	A/D[0]	$\overline{\text{AGNT}}$[1]
	15	N/C (Note 2)	VSS33	VCC33 (Note 3)	A[24]	*Reserved* (Note 4)	BYPASS	CLK
	16	A[11]	VSS33	A[23]	$\overline{\text{RESET}}$	N/C (Note 2)	$\overline{\text{AREQ}}$[2]	VSS33
	17	A[19]	A[17]	VSS33	VCC33 (Note 3)	$\overline{\text{WDOG}}$	N/C (Note 2)	VSS33
	18	A[13]	A[18]	A[22]	VSS33	VSS_PLL	$\overline{\text{AREQ}}$[3]	N/C (Note 2)
	19	A[15]	A[20]	A[25]	$\overline{\text{ERROR}}$	SKEW[0]	VCC33 (Note 3)	$\overline{\text{AREQ}}$[1]

		Rows (Continued)				
		R	T	U	V	W
Column Numbers	1	$\overline{\text{REQ}}$	VSS18	VDD18 (Note 1)	-	-
	2	N/C (Note 2)	$\overline{\text{SDCS}}$[1]	VDD18 (Note 1)	VSS18	-
	3	$\overline{\text{PCI\_RST}}$	A/D[31]	VSS18	VDD18 (Note 1)	VDD18 (Note 1)
	4	N/C (Note 2)	A/D[29]	VCC33 (Note 3)	VSS18	VSS18
	5	N/C (Note 2)	N/C (Note 2)	A/D[26]	N/C (Note 2)	A/D[28]
	6	N/C (Note 2)	A/D[27]	IDSEL	VSS33	A/D[25]
	7	$\overline{\text{SYSEN}}$	VSS33	VCC33 (Note 3)	$\overline{\text{C/BE}}$[3]	A/D[23]
	8	VSS33	VSS33	$\overline{\text{FRAME}}$	A/D[20]	A/D[19]
	9	$\overline{\text{TRDY}}$	VCC33 (Note 3)	N/C (Note 2)	$\overline{\text{C/BE}}$[2]	VSS33
	10	$\overline{\text{PCI\_LOCK}}$	$\overline{\text{DEVSEL}}$	$\overline{\text{STOP}}$	VCC33 (Note 3)	VCC33 (Note 3)
	11	VSS33	VCC33 (Note 3)	VSS33	$\overline{\text{C/BE}}$[1]	$\overline{\text{SERR}}$
	12	N/C (Note 2)	A/D[11]	PAR	VSS33	A/D[13]
	13	VCC33 (Note 3)	A/D[7]	A/D[10]	VSS33	VSS33
	14	VCC33 (Note 3)	VSS33	$\overline{\text{C/BE}}$[0]	A/D[4]	A/D[6]
	15	N/C (Note 2)	A/D[2]	VCC33 (Note 3)	N/C (Note 2)	A/D[3]
	16	N/C (Note 2)	VCC33 (Note 3)	N/C (Note 2)	VDD18 (Note 1)	VSS18
	17	VCC33 (Note 3)	$\overline{\text{AGNT}}$[0]	VSS18	VDD18 (Note 1)	VDD18 (Note 1)
	18	N/C (Note 2)	$\overline{\text{AGNT}}$[2]	VDD18 (Note 1)	VSS18	-
	19	$\overline{\text{AREQ}}$[0]	VSS18	VDD18 (Note 1)	-	-

NOTES:
1. V_{CC1} supply voltage, 1.8V.
2. N/C = Not Connected.
3. V_{CC2} supply voltage, 3.3V.
4. *Reserved* pins shall not be driven to any voltage.

1.9.3 Pin Descriptions

Pins	Signal Type	Active	Description			
			Reset	Type	Definition	Comment
A[27:0]	O			CMOS	Address bus	
A/D[31:0]	I/O			PCI	PCI Address Data	
$\overline{\text{AGNT}}$[3:0]	O	Low		PCI	PCI bus grant	
$\overline{\text{AREQ}}$[3:0]	I	Low		CMOS	PCI bus request	
$\overline{\text{BEXC}}$	I	Low		CMOS	Bus exception	
$\overline{\text{BRDY}}$	I	Low		CMOS	Bus ready	
BYPASS	I	High		CMOS	PLL bypass	Internal pull-down
$\overline{\text{C/BE}}$[3:0]	I/O	Low	Z	PCI	PCI Bus Command and Byte Enables	
CB[7:0]	I/O		Z	CMOS	Check bits	
CLK	I			CMOS	Reference clock	
$\overline{\text{DEVSEL}}$	I/O	Low	Z	PCI	Device Select	
DSUACT	O	High	X / 1 (Note 3)	CMOS	DSU active	
DSUBRE	I	Rise		CMOS	DSU break enable	
DSUEN	I	High		CMOS	DSU enable	
DSURX	I			CMOS	DSU receiver	
DSUTX	O		X / 1 (Note 3)	CMOS	DSU transmitter	
D[31:0]	I/O		Z	CMOS	Data bus	
$\overline{\text{ERROR}}$	Note 1	Low	X / H (Note 3)	CMOS	Processor error	Internal pull-up
$\overline{\text{FRAME}}$	I/O	Low	Z	PCI	Cycle Frame	
$\overline{\text{GNT}}$	I	Low		CMOS	PCI bus grant	
IDSEL	I	High		CMOS	Initialisation Device Select	
$\overline{\text{IOS}}$	O	Low	1	CMOS	I/O select	
$\overline{\text{IRDY}}$	I/O	Low	Z	PCI	Initiator Ready	
LOCK	O	High	X (Note 4)	CMOS	PLL lock	
$\overline{\text{OE}}$	O	Low	1	CMOS	Output enable	
PAR	I/O		Z	PCI	PCI Parity	
PCI_CLK	I			CMOS	PCI Clock	
$\overline{\text{PCI\_LOCK}}$	I/O	Low	Z	PCI	PCI Lock	
$\overline{\text{PCI\_RST}}$	I	Low		CMOS	PCI Reset	
$\overline{\text{PERR}}$	I/O	Low	Z	PCI	Parity Error	
PIO[15:0]	I/O		Z	CMOS	Parallel I/O port	
$\overline{\text{RAMOE}}$[4:0]	O	Low	1	CMOS	SRAM output enable	
$\overline{\text{RAMS}}$[4:0]	O	Low	1	CMOS	SRAM chip select	
READ	O	High	X / 1 (Note 3)	CMOS	Read enable	
$\overline{\text{REQ}}$	O	Low	Z	PCI	PCI bus request	
$\overline{\text{RESET}}$	I	Low		CMOS	Processor reset	
$\overline{\text{ROMS}}$[1:0]	O	Low	1	CMOS	PROM chip select	
$\overline{\text{RWE}}$[3:0]	O	Low	X / 1 (Note 3)	CMOS	PROM & SRAM byte write enable	
$\overline{\text{SDCAS}}$	O	Low	X / 1 (Note 3)	CMOS	SDRAM column address strobe	
SDCLK	O			CMOS	SDRAM clock	
$\overline{\text{SDCS}}$[1:0]	O	Low	1	CMOS	SDRAM chip select	
SDDQM[3:0]	O	High		CMOS	SDRAM data mask	
$\overline{\text{SDRAS}}$	O	Low	X / 1 (Note 3)	CMOS	SDRAM row address strobe	
$\overline{\text{SDWE}}$	O	Low	X / 1 (Note 3)	CMOS	SDRAM write strobe	
$\overline{\text{SERR}}$	I/O	Low	Z	PCI	System Error	

Pins	Signal Type	Active	Description			
			Reset	Type	Definition	Comment
SKEW[1:0]	I			CMOS	Clock tree skew	Internal pull-down
$\overline{\text{STOP}}$	I/O	Low	Z	PCI	Stop	
$\overline{\text{SYSEN}}$	I	Low		CMOS	System Enable	
TCK	I			CMOS	Test Clock	Internal pull-down
TDI	I			CMOS	Test data input	Internal pull-up
TDO	Note 2			CMOS	Test data output	
TMS	I			CMOS	Test Mode select	Internal pull-up
$\overline{\text{TRDY}}$	I/O	Low	Z	PCI	Target Ready	
$\overline{\text{TRST}}$	I	Low		CMOS	Test Reset	Internal pull-up
$\overline{\text{WDOG}}$	Note 1	Low	X / H (Note 3)	CMOS	Watchdog timeout	Internal pull-up
$\overline{\text{WRITE}}$	O	Low	X / 1 (Note 3)	CMOS	Write enable	

NOTES:
1. Open Drain Output.
2. Tri-state Output.
3. First value effective during reset without a running clock while second value effective during reset after the first rising edge of the clock.
4. Value is a strong high or low level, but cannot be predicted during reset without a running clock, then value is a strong low level during reset after the first rising edge of the clock until it becomes a strong high level as soon as the PLL locks (not applicable in PLL bypass mode, i.e. when BYPASS = 1).

1.10 INSTRUCTION SET AND TIMING DIAGRAMS

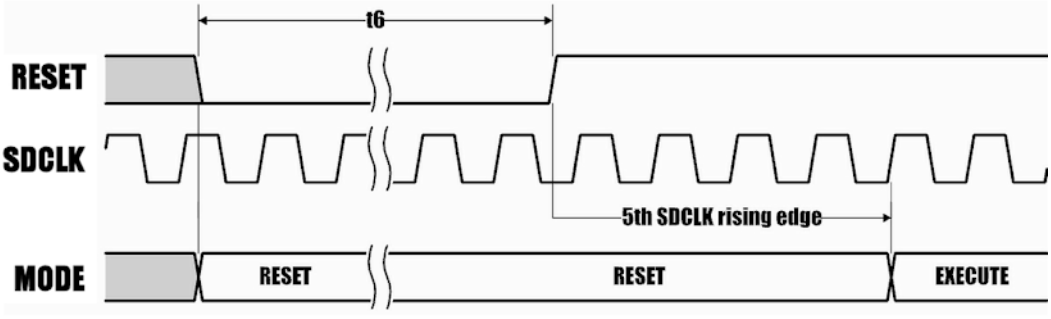
AT697F SPARC instructions fall into six functional categories: load/store, arithmetic/logical/shift, control transfer, read/write control register, floating-point and miscellaneous. Please refer to the SPARC V8 Architecture Manual.

The AT697F fully supports the SPARC V8 multiply instructions (UMUL, SMUL, UMULcc and SMULcc).

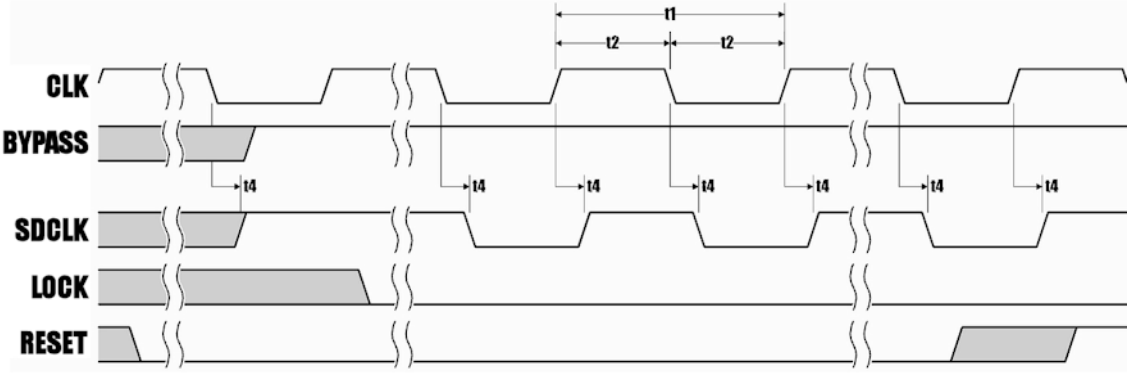
The AT697F fully supports the SPARC V8 divide instructions (UDIV, SDIV, UDIVcc and SDIVcc).

The AT697F floating-point unit is based on the MEIKO core and implements the SPARC floating-point instruction-set defined in the SPARC Architecture Manual version 8.

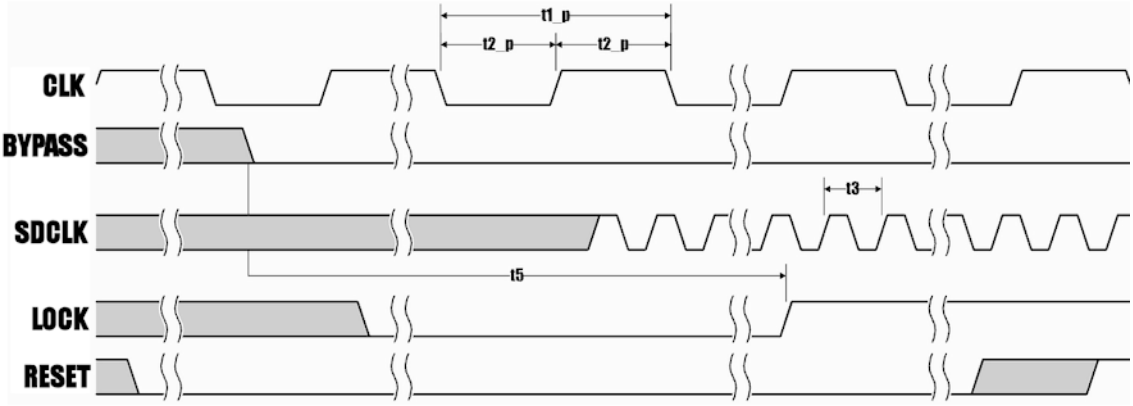
RESET SEQUENCE



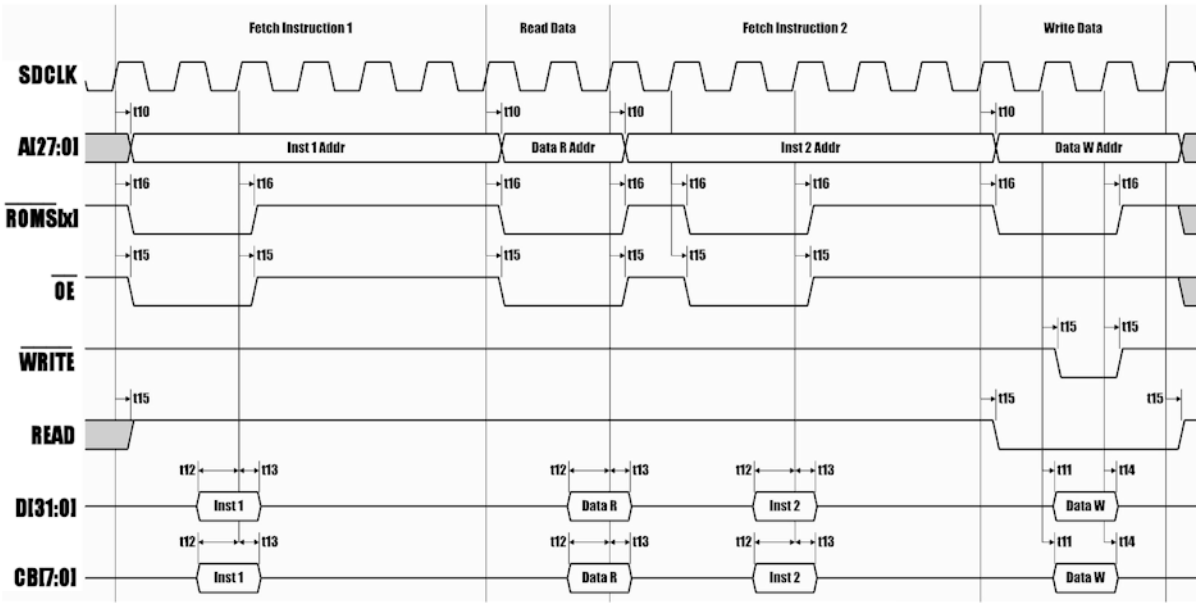
CLOCK INPUT WITHOUT PLL



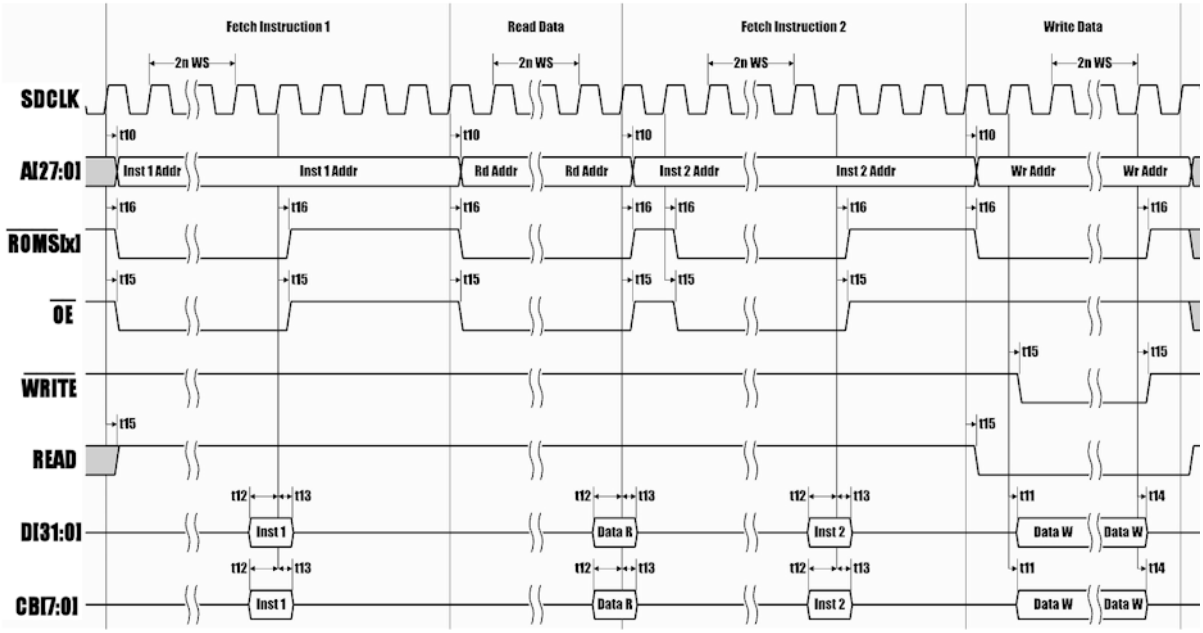
CLOCK INPUT WITH PLL



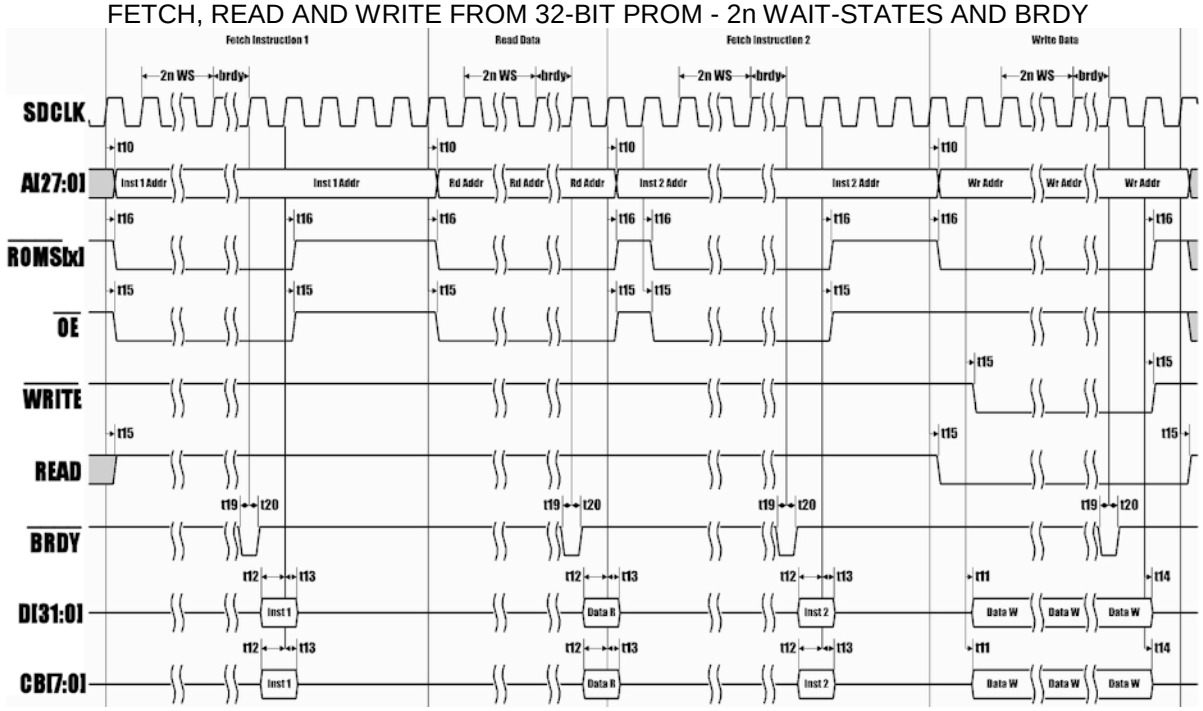
FETCH, READ AND WRITE FROM 32-BIT PROM - 0 WAIT-STATES



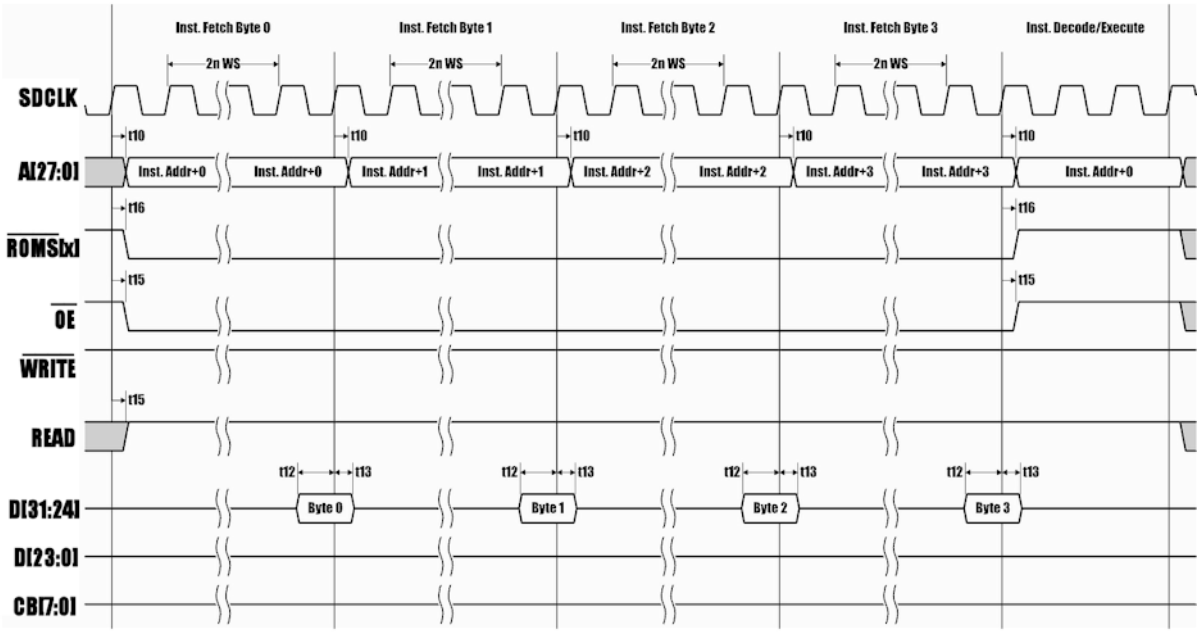
FETCH, READ AND WRITE FROM 32-BIT PROM – 2n WAIT-STATES



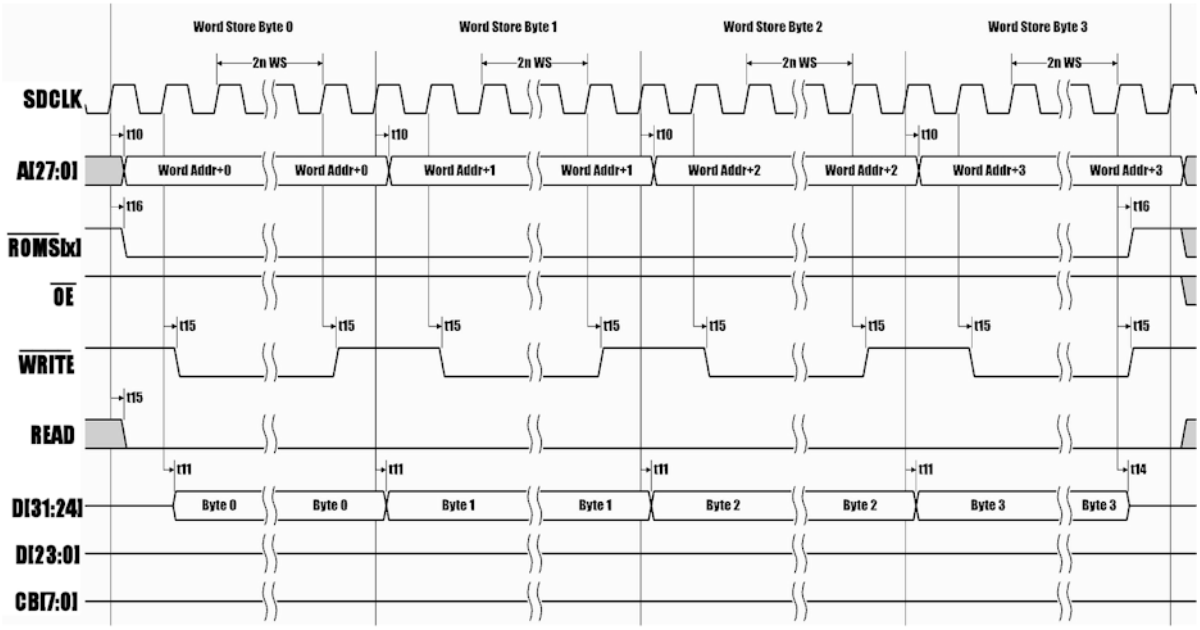
FETCH, READ AND WRITE FROM 32-BIT PROM - 2n WAIT-STATES AND $\overline{\text{BRDY}}$



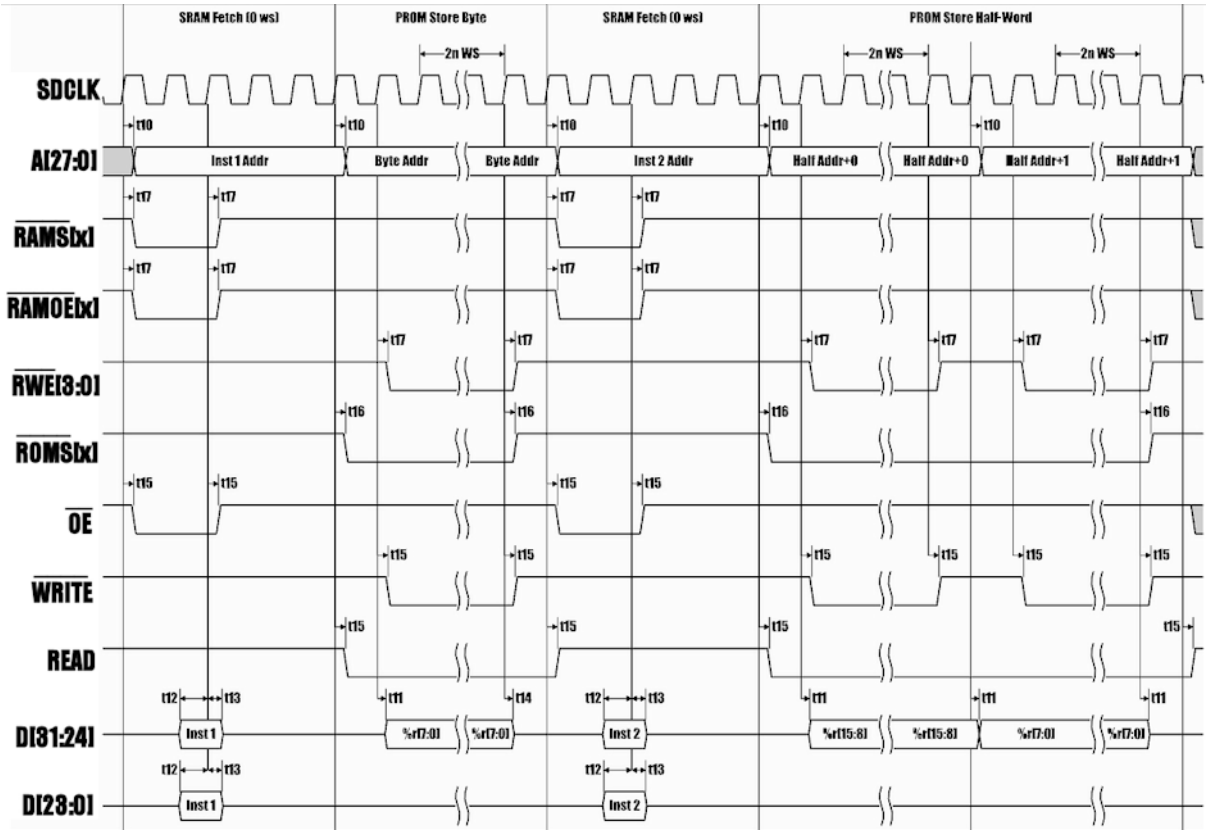
FETCH FROM 8-BIT PROM WITH EDAC DISABLED - 2n WAIT-STATES



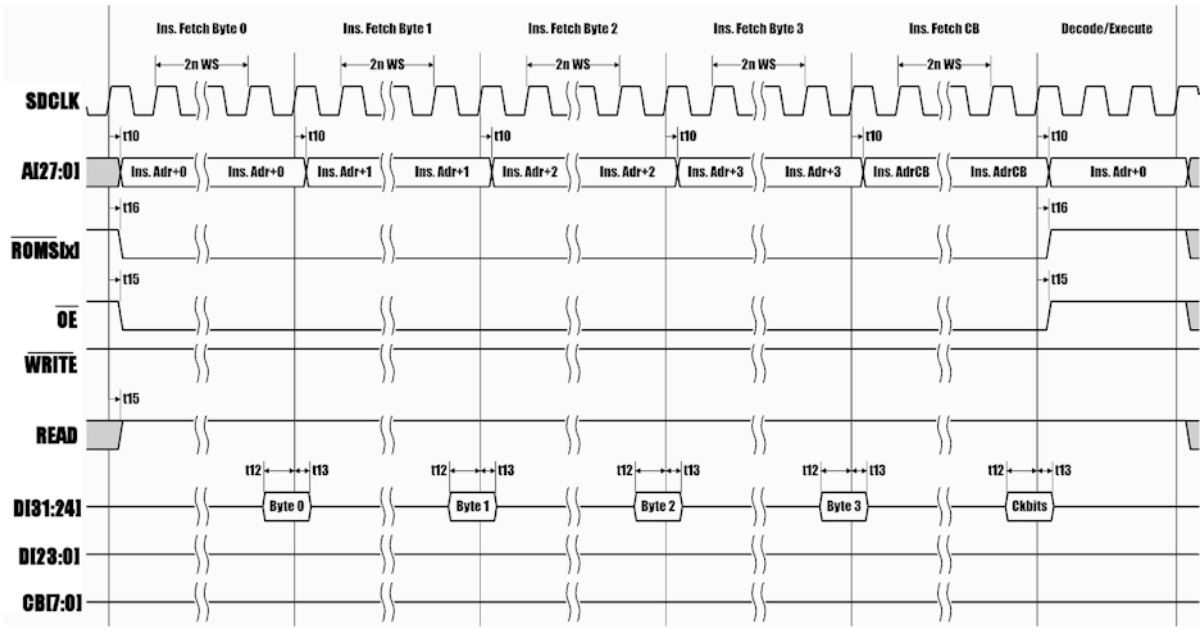
WORD WRITE TO 8-BIT PROM WITH EDAC DISABLED - 2n WAIT-STATES



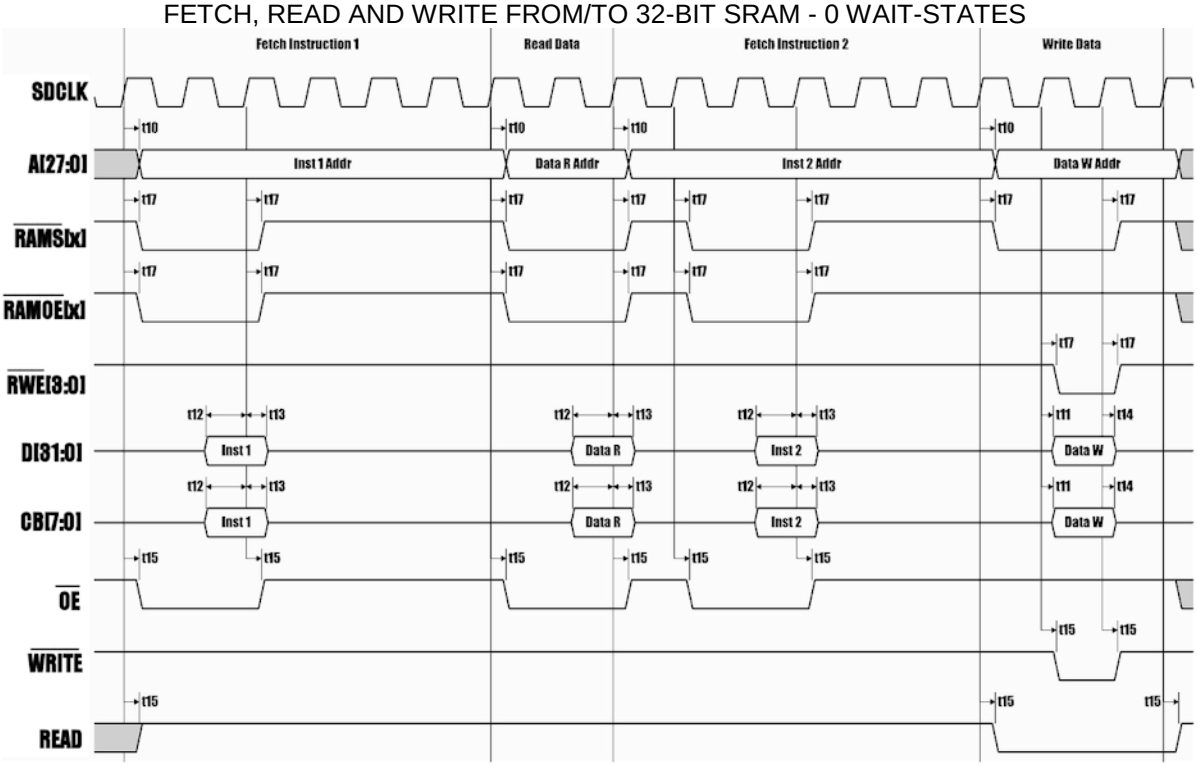
BYTE AND HALF-WORD WRITE TO 8-BIT PROM WITH EDAC DISABLED - 2n WAIT-STATES



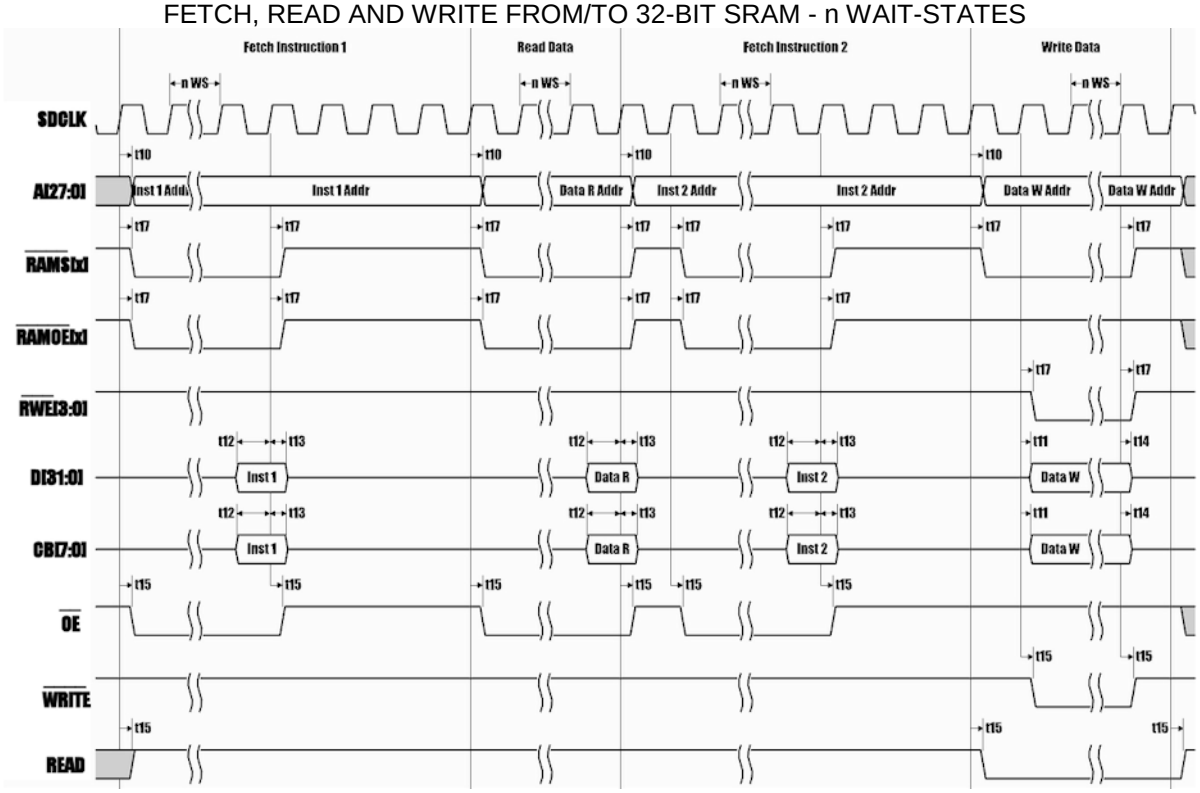
FETCH FROM 8-BIT PROM WITH EDAC ENABLED - 2n WAIT-STATES



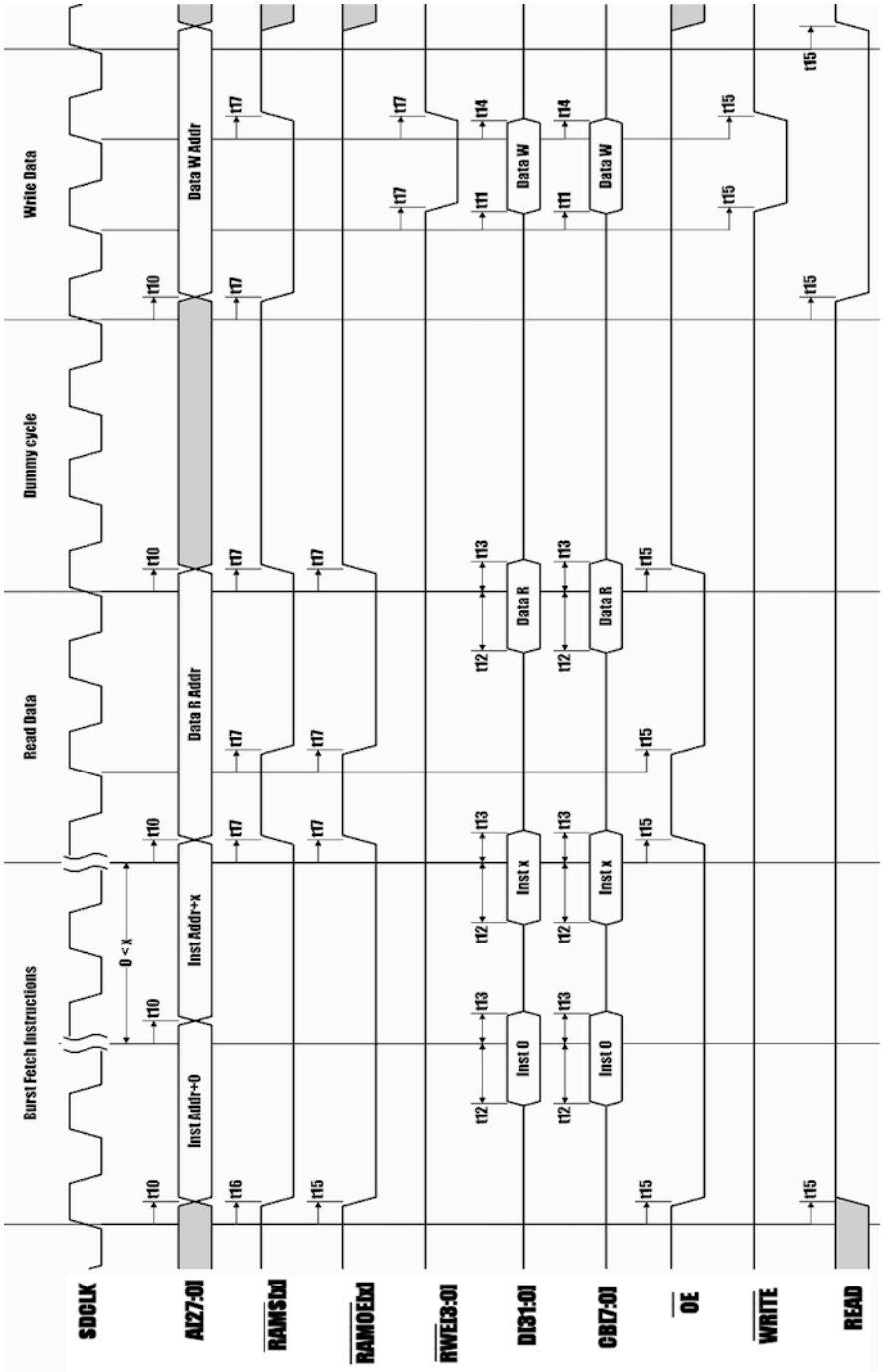
FETCH, READ AND WRITE FROM/TO 32-BIT SRAM - 0 WAIT-STATES



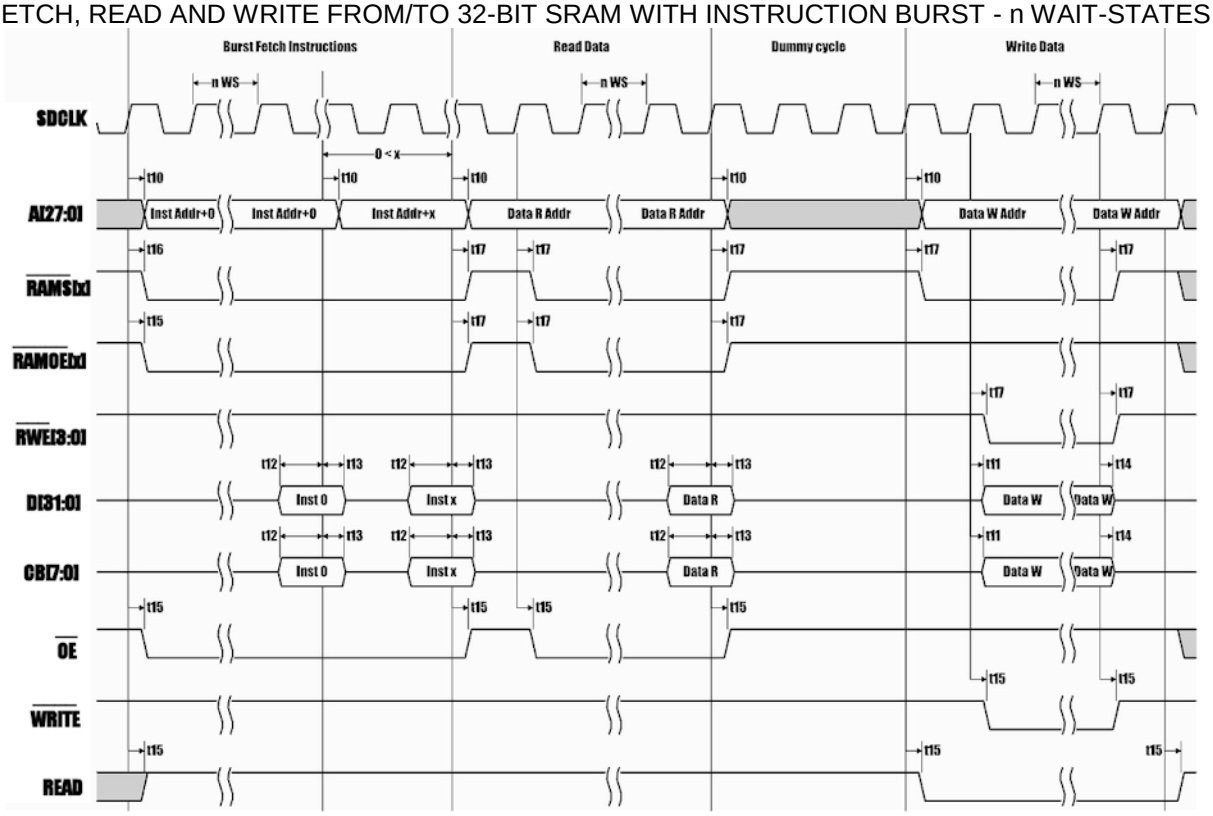
FETCH, READ AND WRITE FROM/TO 32-BIT SRAM - n WAIT-STATES



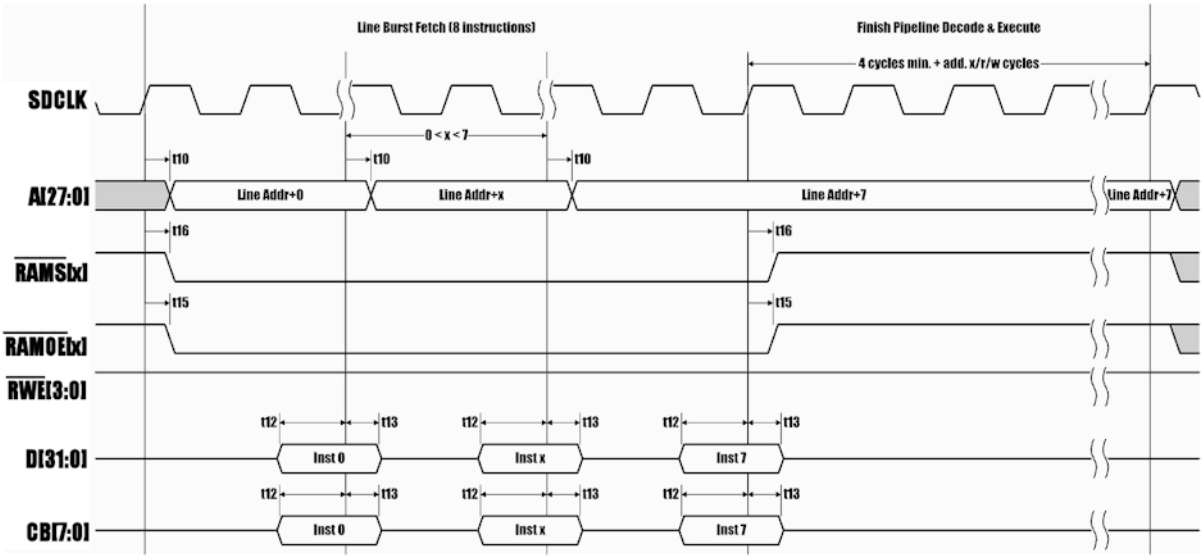
FETCH, READ AND WRITE FROM/TO 32-BIT SRAM WITH INSTRUCTION BURST - 0 WAIT-STATES



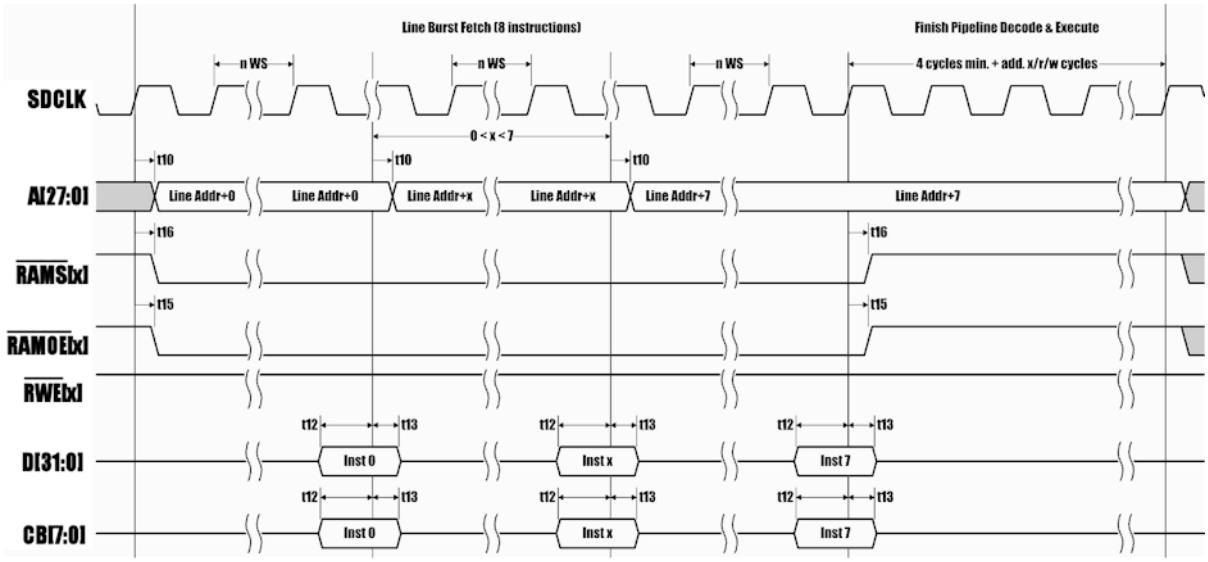
FETCH, READ AND WRITE FROM/TO 32-BIT SRAM WITH INSTRUCTION BURST - n WAIT-STATES



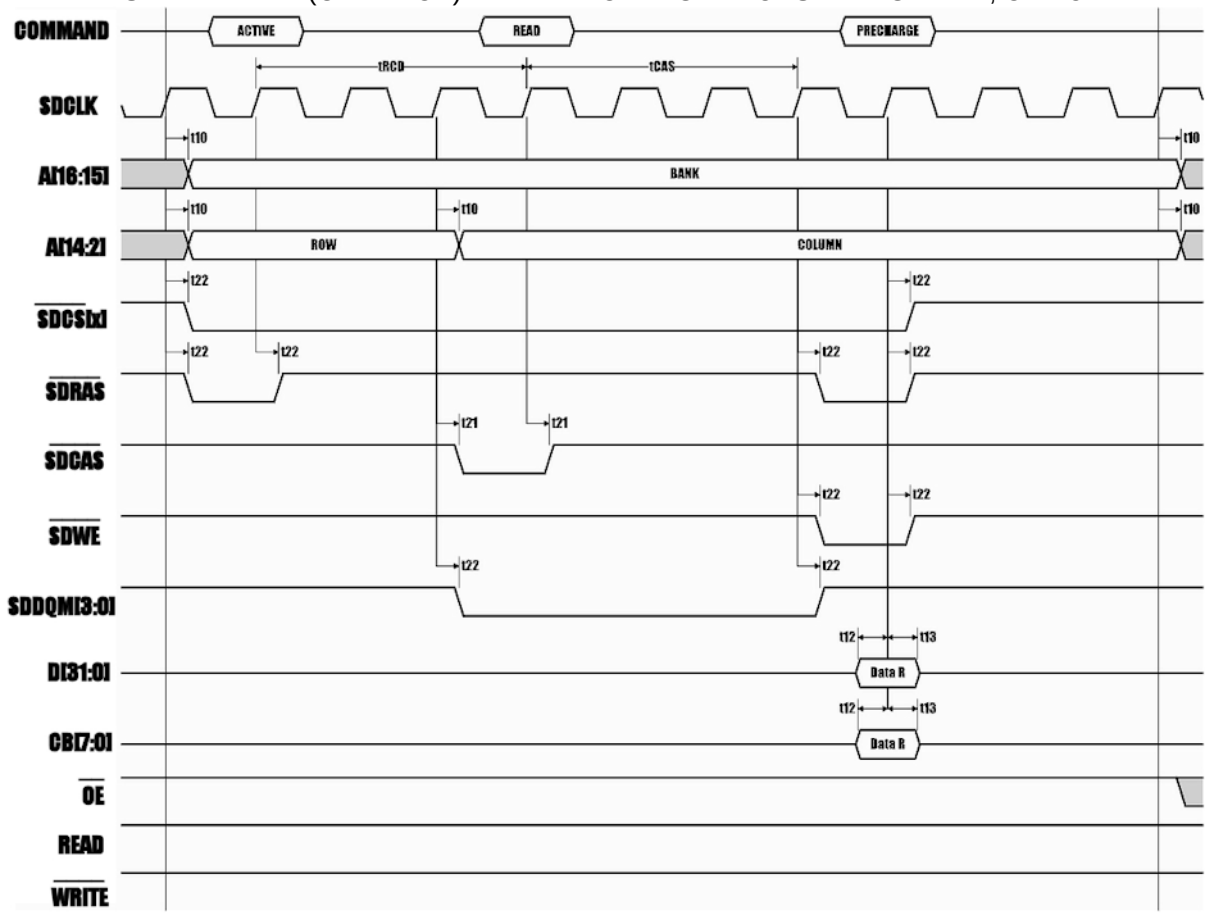
BURST OF SRAM FETCHES WITH INSTRUCTION CACHE AND BURST ENABLED - 0 WAIT-STATES



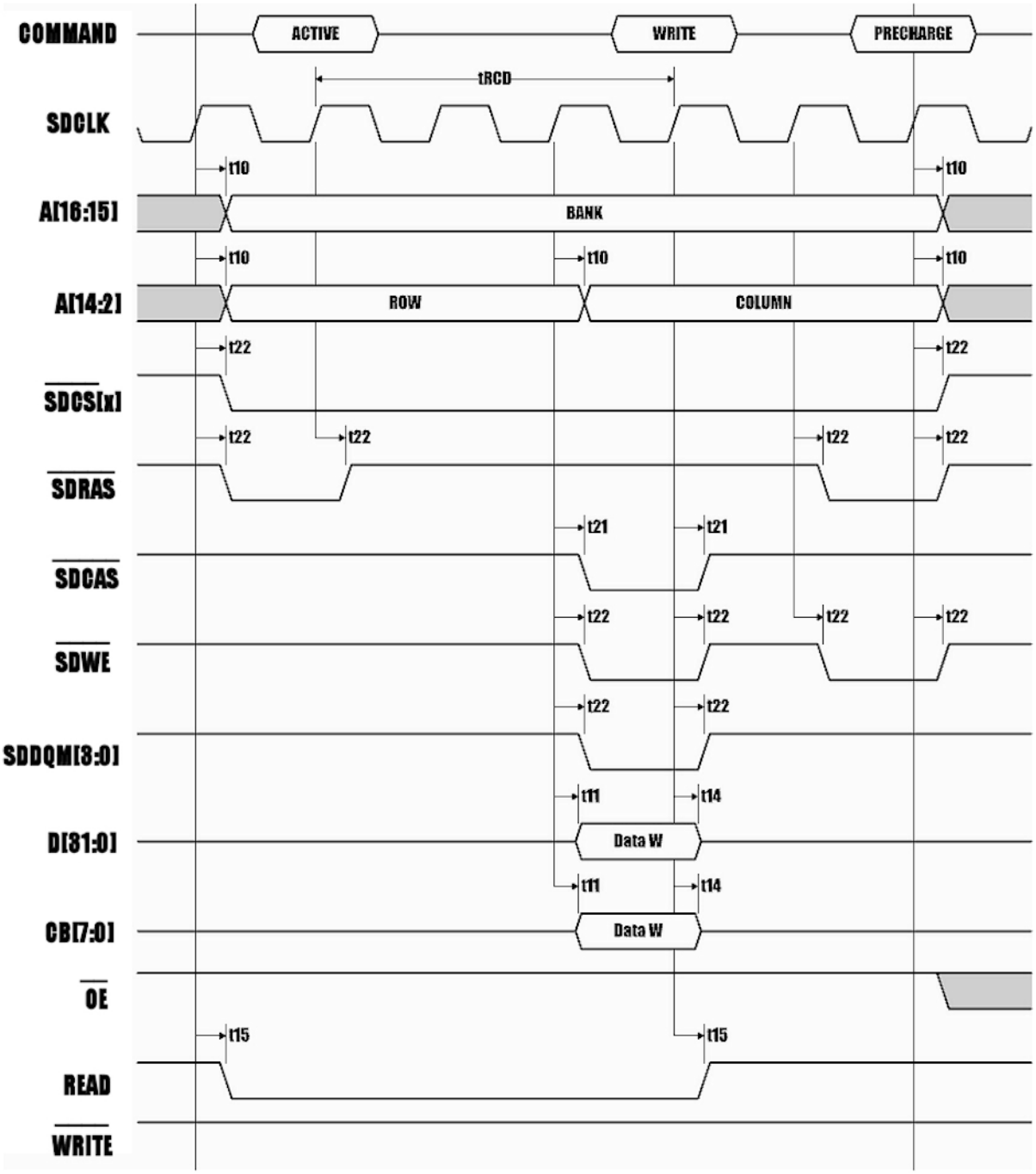
BURST OF SRAM FETCHES WITH INSTRUCTION CACHE AND BURST ENABLED - n WAIT-STATES



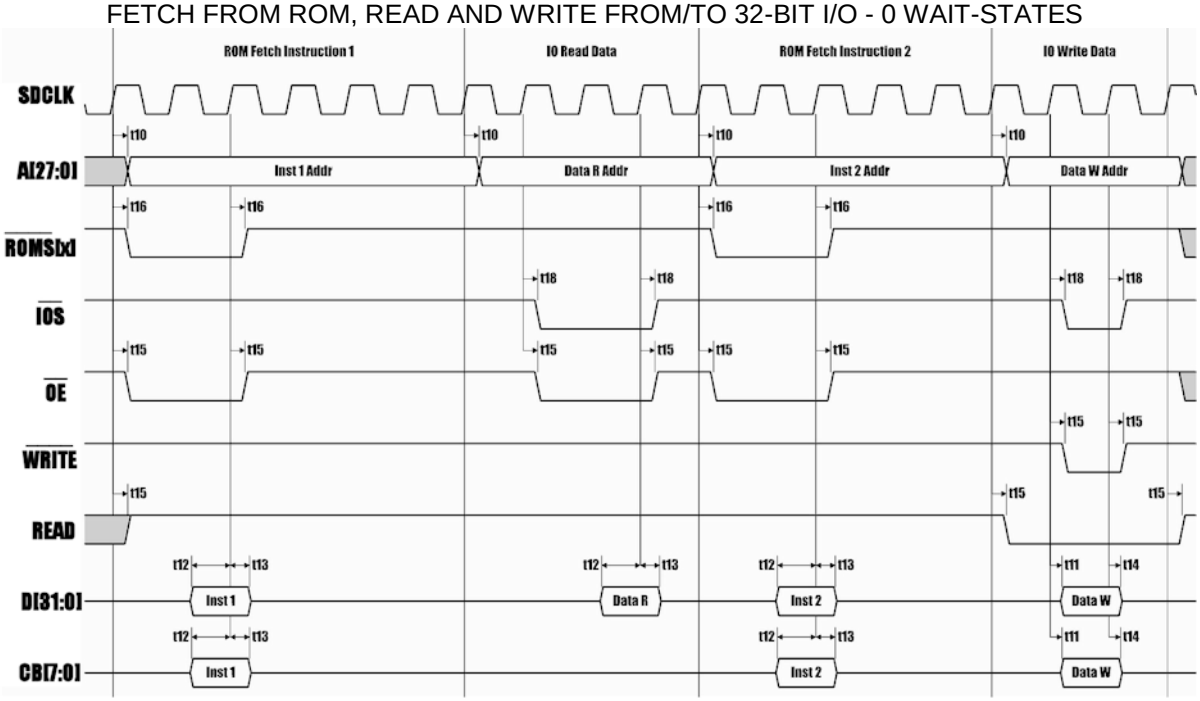
SDRAM READ (OR FETCH) WITH PRECHARGE - BURST LENGTH = 1; CL = 3



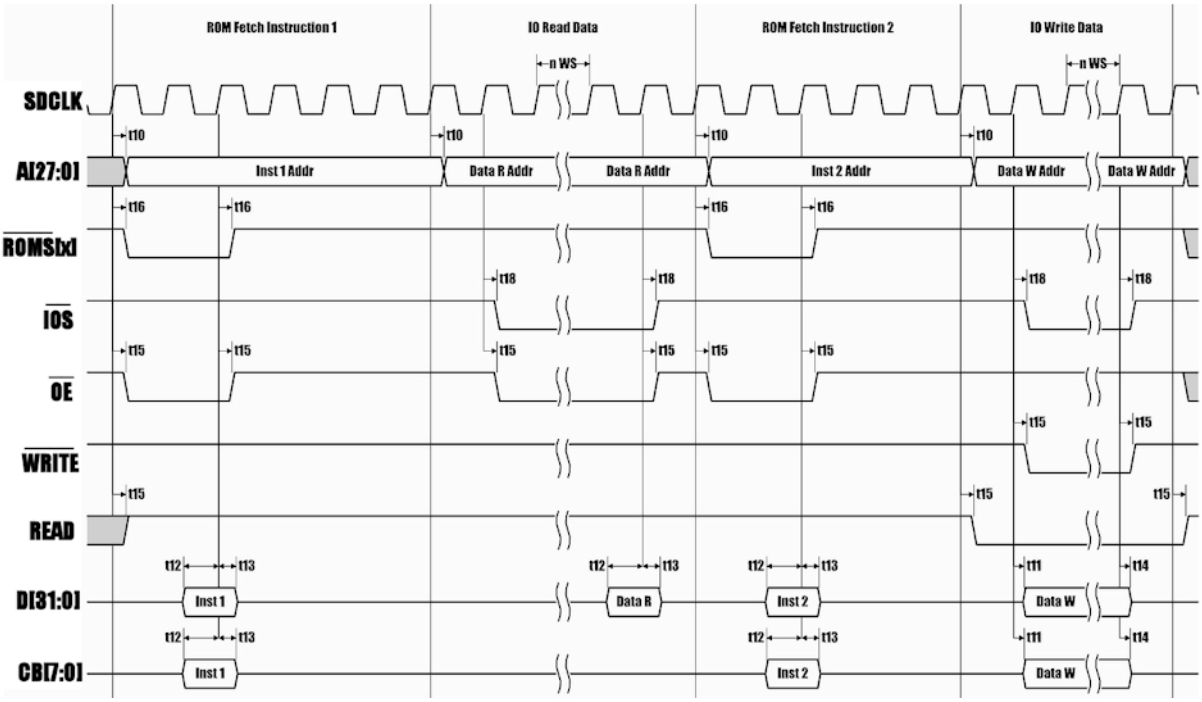
SDRAM WRITE WITH PRECHARGE - BURST LENGTH = 1; CL = 3



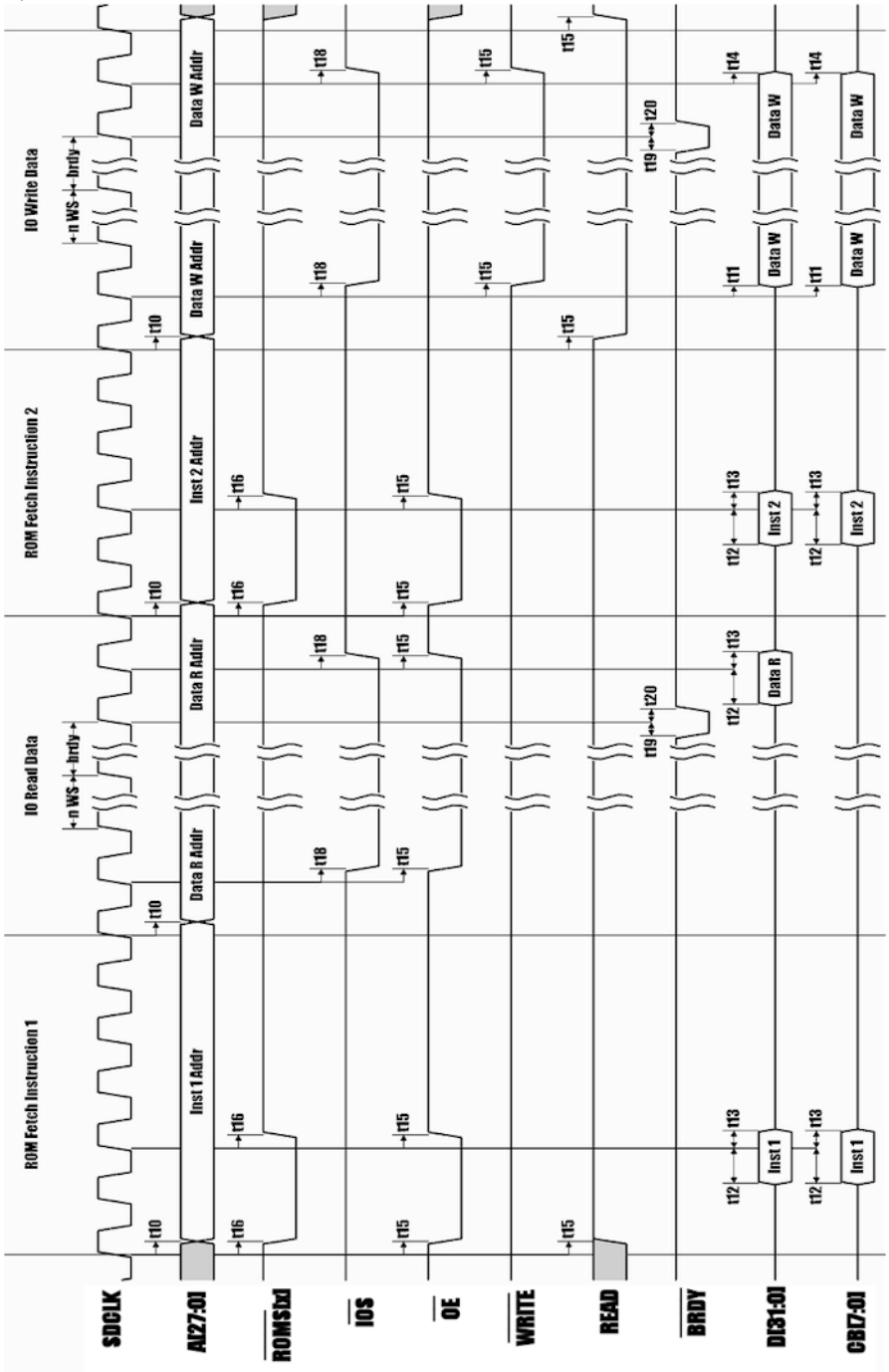
FETCH FROM ROM, READ AND WRITE FROM/TO 32-BIT I/O - 0 WAIT-STATES



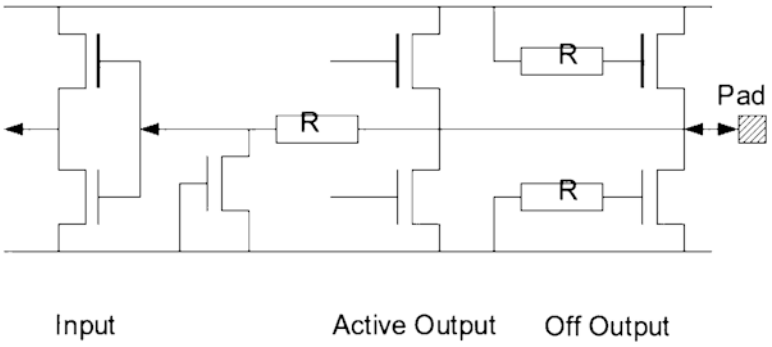
FETCH FROM ROM, READ AND WRITE FROM/TO 32-BIT I/O - n WAIT-STATES



FETCH FROM ROM, READ AND WRITE FROM/TO 32-BIT I/O - n WAIT-STATES AND SYNCHRONISED $\overline{\text{BRDY}}$



1.11 PROTECTION NETWORK



NOTES:
1. The ratio of Active Output to Off Output determines the output strength.
2. Resistors R are approximately 460Ω each.

2 REQUIREMENTS

2.1 GENERAL

The complete requirements for procurement of the components specified herein are as stated in this specification and the ESCC Generic Specification. Permitted deviations from the Generic Specification, applicable to this specification only, are listed below.

Permitted deviations from the Generic Specification and this Detail Specification, formally agreed with specific manufacturers on the basis that the alternative requirements are equivalent to the ESCC requirements and do not affect the component's reliability, are listed in the appendices attached to this specification.

2.1.1 Deviations from the Generic Specification

2.1.1.1 Deviations from Screening Tests

High temperature reverse bias burn-in shall not be performed.

2.2 MARKING

The marking shall be in accordance with the requirements of ESCC Basic Specification No. 21700 and as follows.

The information to be marked on the component shall be:

(a) Terminal identification.
(b) The ESCC qualified components symbol (for ESCC qualified component only).
(c) The ESCC Component Number.
(d) Traceability information.

2.3 ELECTRICAL MEASUREMENTS AT ROOM, HIGH AND LOW TEMPERATURES

Electrical measurements shall be performed at room, high and low temperatures. Consolidated notes are given after the tables.

2.3.1 Room Temperature Electrical Measurements

The measurements shall be performed at T_{amb} = +22±3°C.

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions (Note 1)	Limits		Units
				Min	Max	
FUNC_USPARC	-	3014	1.65V < V_{CC1} < 1.95V 3V < V_{CC2} < 3.6V f = 50MHz (Note 2)	-	-	-
FUNC_TB_FUNC32	-	3014	1.65V < V_{CC1} < 1.95V 3V < V_{CC2} < 3.6V f = 20MHz (Note 2)	-	-	-
FUNC_TB_FUNC8	-	3014	1.65V < V_{CC1} < 1.95V 3V < V_{CC2} < 3.6V f = 20MHz (Note 2)	-	-	-
FUNC_ TB_FUNC_SD	-	3014	1.65V < V_{CC1} < 1.95V 3V < V_{CC2} < 3.6V f = 20MHz (Note 2)	-	-	-
FUNC_PCI_MASTER	-	3014	1.65V < V_{CC1} < 1.95V 3V < V_{CC2} < 3.6V f = 10MHz (Note 2)	-	-	-
FUNC_PCI_SLAVE	-	3014	1.65V < V_{CC1} < 1.95V 3V < V_{CC2} < 3.6V f = 10MHz (Note 2)	-	-	-
FUNC_DSU	-	3014	1.65V < V_{CC1} < 1.95V 3V < V_{CC2} < 3.6V f = 20MHz (Note 2)	-	-	-
FUNC_SRAM	-	3014	1.65V < V_{CC1} < 1.95V 3V < V_{CC2} < 3.6V f = 20MHz (Note 2)	-	-	-
FUNC_TDF	-	3014	1.65V < V_{CC1} < 1.95V 3V < V_{CC2} < 3.6V f(preload) = 12.5MHz f(capture) = 90MHz Test coverage = 81.94% (Note 2)	-	-	-

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions (Note 1)	Limits		Units
				Min	Max	
FUNC_SCAN	-	3014	1.65V < V_{CC1} < 1.95V 3V < V_{CC2} < 3.6V f=25MHz Test coverage = 95.12% (Note 2)	-	-	-
FUNC_JTAG	-	3014	1.65V < V_{CC1} < 1.95V 3V < V_{CC2} < 3.6V f = 10MHz (Note 2)	-	-	-
FUNC_BIST	-	3014	1.65V < V_{CC1} < 1.95V 3V < V_{CC2} < 3.6V f = 10MHz (Note 2)	-	-	-
FUNC_TEST_PLL	-	3014	1.65V < V_{CC1} < 1.95V 3V < V_{CC2} < 3.6V f = 25MHz (Note 2)	-	-	-
Stand-by Current	ICCSB	3005	-	-	5	mA
Low Level Input Current	I_{IL}	3009	(Note 3)	-1	1	µA
Low Level Input Current with Pull-up	I_{ILPU}	3009	(Note 4)	-500	-100	µA
Low Level Input Current with Pull-down	I_{ILPD}	3009	(Note 5)	-5	5	µA
High Level Input Current	I_{IH}	3010	(Note 3)	-1	1	µA
High Level Input Current with Pull-up	I_{IHPU}	3010	(Note 4)	-5	5	µA
High Level Input Current with Pull-down	I_{IHPD}	3010	(Note 5)	100	600	µA
Output Leakage Current Third State, Low Level Applied	IOZL	3020	(Note 6)	-1	1	µA
Output Leakage Current Third State, Low Level Applied with Pull-up	IOZLPU	3020	(Note 7)	-500	100	µA
Output Leakage Current Third State, High Level Applied	IOZH	3021	(Notes 6, 7)	-1	1	µA
High Level Input Voltage	V_{IH}	-	V_{CC2} = 3.6V CMOS buffers PCI buffers	 2 0.5*V_{CC2}	 - -	V
Low Level Input Voltage	V_{IL}	-	V_{CC2} = 3V CMOS buffers PCI buffers	 - -	 0.8 0.3*V_{CC2}	V
Low Level Output Voltage	V_{OL}	3006	V_{CC2} = 3V (Note 8)	-	0.4	V

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions (Note 1)	Limits		Units
				Min	Max	
Low Level Output Voltage, PCI	V_{OLPCI}	3006	V_{CC2} = 3V (Note 9)	-	0.1*V_{CC2}	V
High Level Output Voltage	V_{OH}	3006	V_{CC2} = 3V (Note 10)	V_{CC2}-0.4	-	V
High Level Output Voltage, PCI	V_{OHPCI}	3006	V_{CC2} = 3V (Note 10)	0.9*V_{CC2}	-	V
CLK Period with PLL Disabled	t1	3003	1.65V < V_{CC1} < 1.95V 3V < V_{CC2} < 3.6V (Notes 11, 12) Maximum Skew Natural Skew	 12 10	 - -	ns
CLK Period with PLL Enabled	t1_p	3003	1.65V < V_{CC1} < 1.95V 3V < V_{CC2} < 3.6V (Notes 11, 13) Maximum Skew Natural Skew	 48 40	 50 50	ns
CLK Low and High Pulse Width – PLL Disabled	t2	3003	1.65V < V_{CC1} < 1.95V 3V < V_{CC2} < 3.6V (Notes 11, 12) Maximum Skew Natural Skew	 5.4 4.5	 - -	ns
CLK Low and High Pulse width – PLL Enabled	t2_p	3003	1.65V < V_{CC1} < 1.95V 3V < V_{CC2} < 3.6V (Notes 11, 13) Maximum Skew Natural Skew	 21 18	 - -	ns
SDCLK Period	t3	3003	1.65V < V_{CC1} < 1.95V 3V < V_{CC2} < 3.6V (Notes 11, 12) Maximum Skew Natural Skew	 12 10	 - -	ns
SDCLK Output Delay - PLL Disabled	t4	3003	1.65V < V_{CC1} < 1.95V 3V < V_{CC2} < 3.6V (Notes 11, 14)	3	7	ns
PLL Setup Time	t5	3003	1.65V < V_{CC1} < 1.95V 3V < V_{CC2} < 3.6V (Notes 11, 12)	-	10	ms
Reset Pulse Width	t6	3003	1.65V < V_{CC1} < 1.95V 3V < V_{CC2} < 3.6V (Notes 11, 12)	Note 20	-	ns
A[27:0] Output Delay	t10	3003	1.65V < V_{CC1} < 1.95V 3V < V_{CC2} < 3.6V (Notes 11, 15) Maximum Skew Natural Skew	 1.5 1.5	 8 7	ns
D[31:0] and CB[7:0] Output Delay	t11	3003	1.65V < V_{CC1} < 1.95V 3V < V_{CC2} < 3.6V (Notes 11, 15) Maximum Skew Natural Skew	 2 2	 9 8	ns

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions (Note 1)	Limits		Units
				Min	Max	
D[31:0] and CB[7:0] Setup Time	t12	3003	1.65V < V_{CC1} < 1.95V 3V < V_{CC2} < 3.6V (Notes 11, 15)	4	-	ns
D[31:0] and CB[7:0] Hold Time	t13	3003	1.65V < V_{CC1} < 1.95V 3V < V_{CC2} < 3.6V (Notes 11, 15, 16)	0	-	ns
D[31:0] and CB[7:0] Hold Time During Write	t14	3003	1.65V < V_{CC1} < 1.95V 3V < V_{CC2} < 3.6V (Notes 11, 13, 15, 18) Maximum Skew Natural Skew	 1 0	 11 9	ns
$\overline{OE}$, READ and $\overline{WRITE}$ Output Delay	t15	3003	1.65V < V_{CC1} < 1.95V 3V < V_{CC2} < 3.6V (Notes 11, 15) Maximum Skew Natural Skew	 2 2	 7.5 7	ns
$\overline{ROMS}$[1:0] Output Delay	t16	3003	1.65V < V_{CC1} < 1.95V 3V < V_{CC2} < 3.6V (Notes 11, 15) Maximum Skew Natural Skew	 2 2	 8 5.5	ns
$\overline{RAMS}$[4:0], $\overline{RAMOE}$[4:0] and RWE[3:0] Output Delay	t17	3003	1.65V < V_{CC1} < 1.95V 3V < V_{CC2} < 3.6V (Notes 11, 15) Maximum Skew Natural Skew	 2 2	 7 6	ns
$\overline{IOS}$ Output Delay	t18	3003	1.65V < V_{CC1} < 1.95V 3V < V_{CC2} < 3.6V (Notes 11, 15, 16) Maximum Skew Natural Skew	 2 2	 7 5.5	ns
$\overline{BRDY}$ Setup Time	t19	3003	1.65V < V_{CC1} < 1.95V 3V < V_{CC2} < 3.6V (Notes 11, 13, 15)	5	-	ns
$\overline{BRDY}$ Hold Time	t20	3003	1.65V < V_{CC1} < 1.95V 3V < V_{CC2} < 3.6V (Notes 11, 13, 15)	0	-	ns
$\overline{SDCAS}$ Output Delay	t21	3003	1.65V < V_{CC1} < 1.95V 3V < V_{CC2} < 3.6V (Notes 11, 15) Maximum Skew Natural Skew	 3 3	 10 8	ns
$\overline{SDCS}$[1:0], $\overline{SDRAS}$, $\overline{SDWE}$ and $\overline{SDDQM}$[3:0] Output Delay	t22	3003	1.65V < V_{CC1} < 1.95V 3V < V_{CC2} < 3.6V (Notes 11, 15) Maximum Skew Natural Skew	 2 2	 9.5 8.5	ns
$\overline{BEXC}$ Setup Time	t23	3003	1.65V < V_{CC1} < 1.95V 3V < V_{CC2} < 3.6V (Notes 11, 13, 15)	4	-	ns

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions (Note 1)	Limits		Units
				Min	Max	
$\overline{\text{BEXC}}$ Hold Time	t24	3003	1.65V < V_{CC1} < 1.95V 3V < V_{CC2} < 3.6V (Notes 11, 13, 15)	0	-	ns
PIO[15:0] Output Delay	t25	3003	1.65V < V_{CC1} < 1.95V 3V < V_{CC2} < 3.6V (Notes 11, 15, 16) Maximum Skew Natural Skew	 2.5 2.5	 11 9	ns
PIO[15:0] Setup Time	t26	3003	1.65V < V_{CC1} < 1.95V 3V < V_{CC2} < 3.6V (Notes 11, 13, 15)	4.5	-	ns
PIO[15:0] Hold Time During Write	t28	3003	1.65V < V_{CC1} < 1.95V 3V < V_{CC2} < 3.6V (Notes 11, 13, 15)	2.5	-	ns
PCI_CLK Period	t101	3003	1.65V < V_{CC1} < 1.95V 3V < V_{CC2} < 3.6V (Notes 11, 16)	33	-	ns
PCI_CLK Low and High Pulse Width	t102	3003	1.65V < V_{CC1} < 1.95V 3V < V_{CC2} < 3.6V (Notes 11, 19)	14.5	-	ns
A/D[31:0] and C/BE[3:0] Output Delay	t110	3003	1.65V < V_{CC1} < 1.95V 3V < V_{CC2} < 3.6V (Notes 11, 17, 19) Maximum Skew Natural Skew	 4 4	 13 12	ns
A/D[31:0] and C/BE[3:0] Setup Time	t111	3003	1.65V < V_{CC1} < 1.95V 3V < V_{CC2} < 3.6V (Notes 11, 17, 19)	6		ns
A/D[31:0] and C/BE[3:0] Hold Time	t112	3003	1.65V < V_{CC1} < 1.95V 3V < V_{CC2} < 3.6V (Notes 11, 16, 17)	0		ns
$\overline{\text{FRAME}}$, PAR, $\overline{\text{PERR}}$, $\overline{\text{SERR}}$, $\overline{\text{STOP}}$ and DEVSEL Output Delay	t113	3003	1.65V < V_{CC1} < 1.95V 3V < V_{CC2} < 3.6V (Notes 11, 17, 19) Maximum Skew Natural Skew	 4 4	 12 11	ns
$\overline{\text{IRDY}}$ and $\overline{\text{TRDY}}$ Output Delay	t114	3003	1.65V < V_{CC1} < 1.95V 3V < V_{CC2} < 3.6V (Notes 11, 17, 19) Maximum Skew Natural Skew	 4 4	 12.5 11	ns
$\overline{\text{REQ}}$ Output Delay	t115	3003	1.65V < V_{CC1} < 1.95V 3V < V_{CC2} < 3.6V (Notes 11, 16, 17) Maximum Skew Natural Skew	 4 4	 13 12	ns
$\overline{\text{FRAME}}$, $\overline{\text{LOCK}}$, PAR, $\overline{\text{PERR}}$, $\overline{\text{SERR}}$, IDSEL, $\overline{\text{STOP}}$ and DEVSEL Setup Time	t116	3003	1.65V < V_{CC1} < 1.95V 3V < V_{CC2} < 3.6V (Notes 11, 16, 17) Maximum Skew Natural Skew	 7.5 7	 - -	ns

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions (Note 1)	Limits		Units
				Min	Max	
$\overline{IRDY}$ and $\overline{TRDY}$ Setup Time	t117	3003	$1.65V < V_{CC1} < 1.95V$ $3V < V_{CC2} < 3.6V$ (Notes 11, 16, 17) Maximum Skew Natural Skew	 7.5 7	 - -	ns
$\overline{GNT}$ Setup Time	t118	3003	$1.65V < V_{CC1} < 1.95V$ $3V < V_{CC2} < 3.6V$ (Notes 11, 16, 17) Maximum Skew Natural Skew	 9.5 9	 - -	ns
$\overline{FRAME}$, $\overline{LOCK}$, PAR, $\overline{PERR}$, $\overline{SERR}$, $\overline{IDSEL}$, $\overline{STOP}$ and $\overline{DEVSEL}$ Hold Time	t119	3003	$1.65V < V_{CC1} < 1.95V$ $3V < V_{CC2} < 3.6V$ (Notes 11, 16, 17) Maximum Skew Natural Skew	 0.5 0	 - -	ns
$\overline{IRDY}$ and $\overline{TRDY}$ Hold Time	t120	3003	$1.65V < V_{CC1} < 1.95V$ $3V < V_{CC2} < 3.6V$ (Notes 11, 16, 17) Maximum Skew Natural Skew	 0.5 0	 - -	ns
$\overline{GNT}$ Hold Time	t121	3003	$1.65V < V_{CC1} < 1.95V$ $3V < V_{CC2} < 3.6V$ (Notes 11, 16, 17) Maximum Skew Natural Skew	 0.5 0	 - -	ns

2.3.2 High and Low Temperatures Electrical Measurements

The measurements shall be performed at T_{amb} = +125(+0 -5)°C and T_{amb} = -55(+5 -0)°C.

The characteristics, test methods, conditions and limits shall be the same as specified for Room Temperature Electrical Measurements.

2.3.3 Notes to Electrical Measurements Tables

1. Unless otherwise specified all inputs and outputs shall be tested for each characteristic. Inputs not under test shall be VIN = VSS or VCC and outputs not under test shall be open. VSS = 0V.
2. Functional test. Shall be performed at Natural Skew, Medium Skew and Maximum Skew.
3. Applies to DSUBRE, DSURX, DSUEN, $\overline{BEXC}$, $\overline{BRDY}$, $\overline{PCI\_RST}$, PCI_CLK, $\overline{GNT}$, IDSEL, $\overline{SYSEN}$, $\overline{AREQ}$[3:0], CLK, $\overline{RESET}$.
4. Applies to TDI, TMS, $\overline{TRST}$.
5. Applies to TCK, BYPASS, SKEW[1:0].
6. Applies to CB[7:0], D[31:0], PIO[15:0] , A/D[31:0], TDO, $\overline{REQ}$, $\overline{C/BE}$[3:0], $\overline{FRAME}$, $\overline{IRDY}$, $\overline{TRDY}$, $\overline{DEVSEL}$, $\overline{STOP}$, $\overline{SERR}$, $\overline{PCI\_LOCK}$, $\overline{PERR}$, PAR.
7. Applies to $\overline{WDOG}$, $\overline{ERROR}$.
8. Applies to SDCLK, DSUACT, A[27:0], $\overline{SDCS}$[1:0], $\overline{SDRAS}$, $\overline{SDWE}$, $\overline{OE}$, $\overline{ROMS}$[1:0], $\overline{SDCAS}$, $\overline{RAMOE}$[4:0], $\overline{RAMS}$[4:0], READ, CB[7:0], D[31:0], $\overline{RWE}$[3:0], $\overline{WRITE}$, IOS, $\overline{WDOG}$, PIO[15:0], $\overline{SDDQM}$[3:0], LOCK, $\overline{ERROR}$, DSUTX, TDO.
9. Applies to $\overline{AGNT}$[3:0], $\overline{REQ}$, A/D[31:0], PAR, $\overline{FRAME}$, $\overline{C/BE}$[3:0], $\overline{IRDY}$, $\overline{PERR}$, $\overline{DEVSEL}$, $\overline{TRDY}$, $\overline{STOP}$, $\overline{SERR}$, $\overline{PCI\_LOCK}$, PAR.
10. Applies to SDCLK, DSUACT, A[27:0], $\overline{SDCS}$[1:0], $\overline{SDRAS}$, $\overline{SDWE}$, $\overline{OE}$, $\overline{ROMS}$[1:0], $\overline{SDCAS}$, $\overline{RAMOE}$[4:0], $\overline{RAMS}$[4:0], READ, CB[6:0], D[31:0], $\overline{RWE}$[3:0], $\overline{WRITE}$, IOS, $\overline{WDOG}$, PIO[15:0], $\overline{SDDQM}$[3:0], $\overline{ERROR}$, DSUTX, TDO.
11. Test shall be performed at Natural Skew and Maximum Skew. The output load = 50pF.

12. Not recorded, only tested GO-NO-GO as part of functional tests.
13. Guaranteed but not tested.
14. The specified delay is with reference to CLK.
15. The specified delay is with reference to the rising edge of SDCLK.
16. Parameter tested GO-NO-GO at each supply voltage during AC testing.
17. The specified delay is with reference to the rising edge of PCI_CLK.
18. When the buffer stops driving the buses.
19. Recorded in PCI Master and Slave conditions.
20. The applicable minimum limit shall be the corresponding measured value of t3 (SDCLK Period).

2.4 PARAMETER DRIFT VALUES

Unless otherwise specified, the measurements shall be performed at T_{amb} = +22±3°C.

The test methods and test conditions shall be as per the corresponding test defined in Room Temperature Electrical Measurements.

The drift values (Δ) shall not be exceeded for each characteristic specified. The corresponding absolute limit values for each characteristic shall not be exceeded.

Characteristics	Symbols	Limits			Units
		Drift Value Δ	Absolute		
			Min	Max	
Stand-by Current	ICCSB	±0.5	-	5	mA
Low Level Input Current	I_{IL}	±0.1	-	-1	µA
High Level Input Current	I_{IH}	±0.1	-	1	µA
Output Leakage Current Third State, Low Level Applied	I_{OZL}	±0.1	-	-1	µA
Output Leakage Current Third State, High Level Applied	I_{OZH}	±0.1	-	1	µA
Low Level Output Voltage	V_{OL}	±100	-	400	mV
High Level Output Voltage	V_{OH}	±0.1	2.6	-	V

2.5 INTERMEDIATE AND END-POINT ELECTRICAL MEASUREMENTS

Unless otherwise specified, the measurements shall be performed at T_{amb} = +22±3°C.

The characteristics, test methods, conditions and limits shall be the same as specified for Room Temperature Electrical Measurements.

2.6 POWER BURN-IN CONDITIONS

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	T_{amb}	+125(+0 -3)	°C
Inputs RESET, D[31:0]	V_{IN}	V_{CC2}(+0, -0.6)	V
Input CLK	V_{IN}	V_{GEN}	V
Inputs DSUBRE, DSUEN, PCI_RST, SKEW[1:0], TCK, TRST	V_{IN}	V_{SS}	V
Remaining Inputs	V_{IN}	V_{CC1}	V
All Outputs	V_{OUT}	V_{CC1}/2	V
Pulse Voltage	V_{GEN}	0V to V_{CC2}(+0, -0.6)	V
Pulse Frequency Square Wave	f_{GEN}	2.5 50±15% Duty Cycle	MHz
Positive Core Supply Voltage	V_{CC1}	1.8 (+0.15, -0)	V
Positive Interface Supply Voltage	V_{CC2}	3.3 (+0.3, -0)	V
Negative Supply Voltage	V_{SS}	0	V

NOTES:
1. All Inputs and Outputs shall be connected through a suitable serial protection resistor/load.

2.7 OPERATING LIFE CONDITIONS

The conditions shall be as specified for Power Burn-in.

2.8 TOTAL DOSE IRRADIATION TESTING

2.8.1 Bias Conditions and Total Dose Level for Total Dose Radiation Testing

Continuous bias shall be applied during irradiation testing as specified below.

The total dose level applied shall be as specified in the component type variant information herein or in the Purchase Order.

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	T_{amb}	+22±3	°C
Inputs PCI_CLK, CLK (Note 2)	V_{IN}	V_{GEN}	V
Remaining Inputs	V_{IN}	$V_{CC2}/2$	V
All Outputs	V_{OUT}	$V_{CC2}/2$	V
Pulse Voltage (Note 2)	V_{GEN}	0V to V_{CC2}(+0, -6)	V
Pulse Frequency Square Wave (Note 2)	f_{GEN}	100 50±15% Duty Cycle t = 10µs	kHz
Positive Core Supply Voltage	V_{CC1}	1.8 (+0.15, -0)	V
Positive Interface Supply Voltage	V_{CC2}	3.3 (+0.3, -0)	V
Negative Supply Voltage	V_{SS}	0	V

NOTES:

1. All Inputs and Outputs shall be connected through a suitable serial protection resistor/load.
2. f_{GEN} is only required for the period specified in order to initialise the component. After initialisation, Inputs PCI_CLK and CLK shall be $V_{CC}/2$.

2.8.2 Electrical Measurements for Total Dose Radiation Testing

Prior to, during and on completion of irradiation testing the devices shall have successfully met Room Temperature Electrical Measurements specified herein.

Unless otherwise stated the measurements shall be performed at T_{amb} = +22±3°C.

The characteristics, test methods, conditions and limits shall be as per the corresponding test defined in Room Temperature Electrical Measurements.