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Pages 1 to 40

**INTEGRATED CIRCUITS, SILICON MONOLITHIC,
32-BIT SPARC EMBEDDED PROCESSOR,
BASED ON TYPE TSC695F**

ESCC Detail Specification No. 9512/003

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DOCUMENTATION CHANGE NOTICE

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DCR No.	CHANGE DESCRIPTION
TBD1 TBD2	Specification up issued to incorporate editorial and Technical changes per DCR

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1. GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics, test and inspection data for the component type variants and/or the range of components specified below. It supplements the requirements of, and shall be read in conjunction with, the ESCC Generic Specification listed under Applicable Documents.

1.2 APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:

- (a) ESCC Generic Specification No. 9000.
- (b) MIL-STD-883, Test Methods and Procedures for Microelectronics.

1.3 TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESCC Basic specification No. 21300 shall apply.

1.4 THE ESCC COMPONENT NUMBER AND COMPONENT TYPE VARIANTS

1.4.1 The ESCC Component Number

The ESCC Component Number shall be constituted as follows:

Example: 951200301R

- Detail Specification Reference: 9512003
- Component Type Variant Number: 01 (as required)
- Total Dose Radiation Level Letter: R (as required)

1.4.2 Component Type Variants

The component type variants applicable to this specification are as follows:

Variant Number	Based on Type	Case	Terminal Material and/or Finish	Weight Max g	Total Dose Radiation Level Letter
01	TSC695F	MQFP-F256	G2	15	R [100kRAD(Si)]

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The terminal material and/or finish shall be in accordance with the requirements of ESCC Basic Specification No. 23500.

The total dose radiation level letter shall be as defined in ESCC Basic Specification No. 22900. If an alternative radiation test level is specified in the Purchase Order the letter shall be changed accordingly.

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1.5 MAXIMUM RATINGS

The maximum ratings shall not be exceeded at any time during use or storage. Functional performance for extended periods at the maximum ratings may adversely affect device reliability.

Maximum ratings shall only be exceeded during testing to the extent specified in this specification and when stipulated in Test Methods and Procedures of the ESCC Generic Specification.

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Characteristics	Symbols	Maximum Ratings	Units	Remarks
Supply Voltage	V_{DD}	-0.5 to +7	V	1
Input Voltage Range	V_{IN}	-0.5 to $V_{DD} + 0.5$	V	2
Input Current per Signal pin per Power pin	I_{IN}	-10 to +10 -50 to +50	mAdc	
Output Current	I_{OUT}	-90 to +110	mAdc	3
Device Power Dissipation	P_D	1.5	W	
Operating Temperature	T_{op}	-55 to +125	°C	T_{amb}
Storage Temperature	T_{stg}	-65 to +150	°C	
Junction Temperature	T_{Jmax}	165	°C	
Thermal Resistance	$R_{th(J-C)}$	3	°C/W	
Soldering Temperature	T_{sol}	265	°C	4

NOTES

1. Device is functional for $4.5 \leq V_{DD} \leq 5.5V$ with reference to $V_{SS} = 0V$.
2. $V_{DD} + 0.5V$ shall not exceed +7V.
3. The maximum output current of any single output for a maximum duration of 1 second.
4. Duration 10 seconds maximum at a distance of not less than 1.6mm from the device body and the same terminal shall not be resoldered until 3 minutes have elapsed.

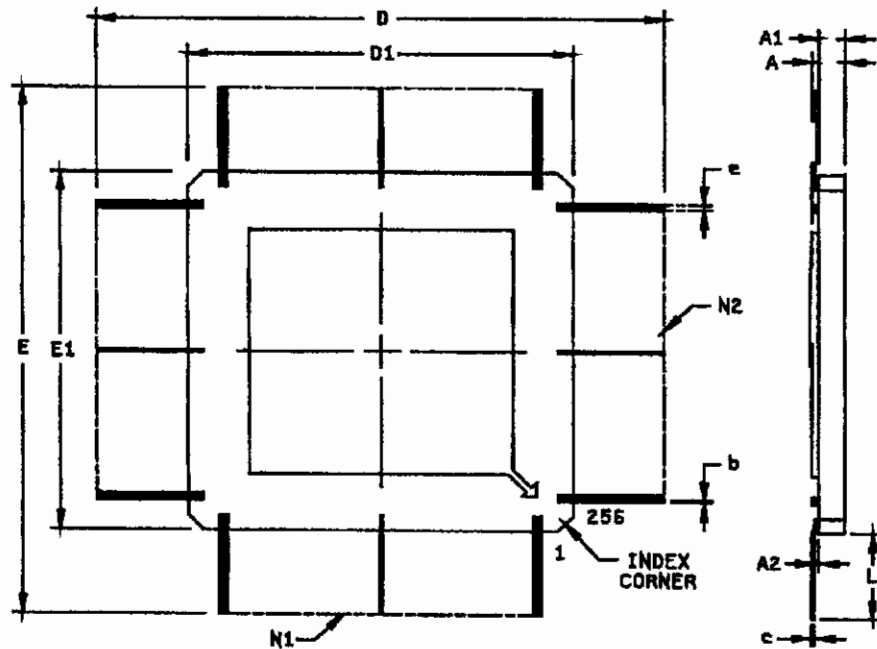
1.6 HANDLING PRECAUTIONS

These devices are susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacture, testing, packaging, shipment and any handling.

These components are categorised as Class 1 per ESCC Basic Specification No. 23800 with a Minimum Critical Path Failure Voltage of 1000 volts.

1.7 PHYSICAL DIMENSIONS AND TERMINAL IDENTIFICATION

1.7.1 ~~256 Flat Leads~~ Multilayer Quad Flat Package - (MQFP-F256) - 256 Flat leads



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Symbols Dimension	Dimension mm		Shade in Notes
	Min	Max	
A	2.41	3.18	
A1	2.06	2.56	
A2	0.05	0.36	
b	0.15	0.25	1
c	0.1	0.2	1
D, E	53.23	55.74	
D1, E1	36.83	37.34	
e	0.508 BSC		1
L	8.2	9.2	1
N1, N2	64		

NOTES

1. All leads
2. Terminal identification is specified by reference to the index corner as shown.

1.9 PIN ASSIGNMENT AND DESCRIPTION

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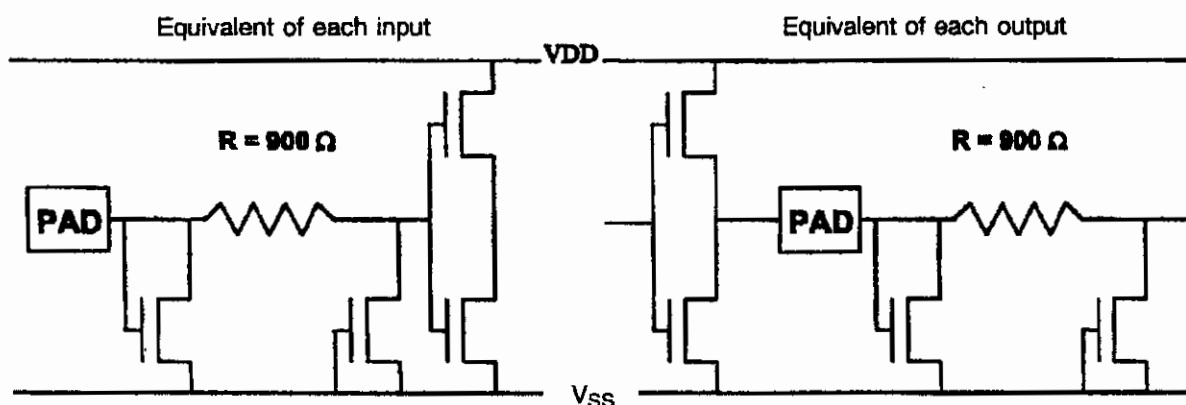
Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	GPIINT	33	D[20]	65	D[0]	97	RA[18]
2	GPI[7]	34	D[19]	66	RSIZE[1]	98	V _{DDO}
3	V _{DDO}	35	D[18]	67	RSIZE[0]	99	V _{SSO}
4	V _{SSO}	36	V _{DDO}	68	RASI[3]	100	RA[17]
5	GPI[6]	37	V _{SSO}	69	V _{DDO}	101	RA[16]
6	GPI[5]	38	D[17]	70	V _{SSO}	102	RA[15]
7	GPI[4]	39	D[16]	71	RASI[2]	103	V _{DDO}
8	GPI[3]	40	V _{DDI}	72	RASI[1]	104	V _{SSO}
9	V _{DDO}	41	V _{SSI}	73	RASI[0]	105	RA[14]
10	V _{SSO}	42	D[15]	74	RA[31]	106	V _{DDI}
11	GPI[2]	43	D[14]	75	RA[30]	107	V _{SSI}
12	GPI[1]	44	V _{DDO}	76	V _{DDO}	108	RA[13]
13	GPI[0]	45	V _{SSO}	77	V _{SSO}	109	RA[12]
14	D[31]	46	D[13]	78	RA[29]	110	V _{DDO}
15	D[30]	47	D[12]	79	RA[28]	111	V _{SSO}
16	V _{DDO}	48	D[11]	80	RA[27]	112	RA[11]
17	V _{SSO}	49	D[10]	81	V _{DDO}	113	RA[10]
18	D[29]	50	V _{DDO}	82	V _{SSO}	114	RA[9]
19	D[28]	51	V _{SSO}	83	RA[26]	115	V _{DDO}
20	V _{DDI}	52	D[9]	84	RA[25]	116	V _{SSO}
21	V _{SSI}	53	D[8]	85	RA[24]	117	RA[8]
22	D[27]	54	D[7]	86	V _{DDI}	118	RA[7]
23	D[26]	55	D[6]	87	V _{SSI}	119	RA[6]
24	V _{DDO}	56	V _{DDO}	88	V _{DDO}	120	V _{DDO}
25	V _{SSO}	57	V _{SSO}	89	V _{SSO}	121	V _{SSO}
26	D[25]	58	D[5]	90	RA[23]	122	RA[5]
27	D[24]	59	D[4]	91	RA[22]	123	RA[4]
28	D[23]	60	D[3]	92	RA[21]	124	RA[3]
29	D[22]	61	D[2]	93	V _{DDO}	125	V _{DDO}
30	V _{DDO}	62	V _{DDO}	94	V _{SSO}	126	V _{SSO}
31	V _{SSO}	63	V _{SSO}	95	RA[20]	127	RA[2]
32	D[21]	64	D[1]	96	RA[19]	128	RA[1]

Pin	Function	Pin	Function	Pin	Function	Pin	Function
129	RA[0]	161	SYSERR	193	DXFER	225	MEMCS[3]
130	VDDO	162	SYSAB	194	MEXC	226	VDDO
131	VSSO	163	EXTINT[4]	195	VDDO	227	VSSO
132	RAPAR	164	EXTINT[3]	196	VSSO	228	MEMCS[2]
133	RASPAR	165	EXTINT[2]	197	RESET	229	MEMCS[1]
134	DPAR	166	EXTINT[1]	198	SYSRESET	230	MEMCS[0]
135	VDDO	167	EXTINT[0]	199	BA[1]	231	VDDI
136	VSSO	168	VDDI	200	BA[0]	232	VSSI
137	SYSCLK	169	VSSI	201	CB[6]	233	OE
138	TDO	170	EXTINTACK	202	CB[5]	234	VDDO
139	TRST	171	TUERR	203	VDDO	235	VSSO
140	TMS	172	VDDO	204	VSSO	236	MEMWR
141	TDI	173	VSSO	205	CB[4]	237	BUFFEN
142	TCK	174	CPAR	206	CB[3]	238	DDIR
143	CLK2	175	TXA	207	CB[2]	239	VDDO
144	DRDY	176	RXA	208	CB[1]	240	VSSO
145	DMAAS	177	RXB	209	VDDO	241	DDIR
146	VDDO	178	TXB	210	VSSO	242	MHOLD
147	VSSO	179	TOWR	211	CB[0]	243	MDS
148	DMAGNT	180	IOSEL[3]	212	ALE	244	WDCLK
149	EXMCS	181	VDDO	213	VDDI	245	IWDE
150	VDDI	182	VSSO	214	VSSI	246	EWDINT
151	VSSI	183	IOSEL[2]	215	PROMB	247	TMODE[1]
152	DMAREQ	184	IOSEL[1]	216	ROMCS	248	TMODE[0]
153	BUSERR	185	IOSEL[0]	217	MEMCS[9]	249	DEBUG
154	BUSRDY	186	WRT	218	VDDO	250	INULL
155	ROMWRT	187	WE	219	VSSO	251	DIA
156	NOPAR	188	VDDO	220	MEMCS[8]	252	VDDO
157	SYSHALT	189	VSSO	221	MEMCS[7]	253	VSSO
158	CPUHALT	190	RD	222	MEMCS[6]	254	FLUSH
159	VDDO	191	RLDSTO	223	MEMCS[5]	255	INST
160	VSSO	192	LOCK	224	MEMCS[4]	256	RTC

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Signal	Type	Active	Description	
RA[31-0]	I/O		32-bit registered address bus	Output buffer: 400pF
RAPAR	I/O	High	Registered address bus parity	-
RASI[3-0]	I/O		4-bit registered address space identifier	-
RSIZE[1-0]	I/O		2-bit registered bus transaction size	-
RASPAR	I/O	High	Registered ASI and SIZE parity	-
CPAR	I/O	High	Control bus parity	-
D[31-0]	I/O		32-bit data bus	-
CB[6-0]	I/O		7-bit check-bit bus	-
DPAR	I/O	High	Data bus parity	-
RLDSTO	I/O	High	Registered atomic load-store	-

1.11 PROTECTION NETWORKS



2. REQUIREMENTS

2.1 GENERAL

The complete requirements for procurement of the components specified herein are as stated in this specification and the applicable ESCC Generic Specification. Permitted deviations from the ~~applicable~~ Generic Specification, applicable to this specification only, are listed below.

Permitted deviations from the ~~applicable~~ Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESCC requirement and do not affect the component's reliability, are listed in the appendices attached to this specification.

2.1.1 Deviations from the Generic Specification

2.1.1.1 Deviations from Screening Tests

High Temperature Reverse Bias Burn-in shall not be performed.

2.2 MARKING

The marking shall be in accordance with the requirements of ESCC Basic Specification No. 21700 and as follows.

The information to be marked on the component shall be:

- Terminal identification.
- The ESCC qualified components symbol (for ESCC qualified components only).
- The ESCC Component Number
- Traceability information.

2.3 ELECTRICAL MEASUREMENTS AT ROOM, HIGH AND LOW TEMPERATURES

Electrical measurements shall be performed at room, high and low temperatures. ~~Consolidated~~
Notes are given after the tables.

2.3.1 Room Temperature Electrical Measurements

The measurements shall be performed at $T_{amb} = +22 \pm 3^\circ\text{C}$.

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions (Note 1)	Limits		Units
				Min	Max	
Functional Test 1	-	3014	$V_{IL} = 0.8\text{V}$, $V_{IH1} = 2.2\text{V}$, $V_{IH2} = 3\text{V}$ $V_{DD} = 4.5\text{V}$, $V_{SS} = 0\text{V}$ Note 2	-	-	-
Functional Test 2	-	3014	$V_{IL} = 0.8\text{V}$, $V_{IH1} = 2.2\text{V}$, $V_{IH2} = 3\text{V}$ $V_{DD} = 5\text{V}$, $V_{SS} = 0\text{V}$ Note 2	-	-	-
Functional Test 3	-	3014	$V_{IL} = 0.8\text{V}$, $V_{IH} = 2.2\text{V}$, $V_{IH2} = 3\text{V}$ $V_{DD} = 5.5\text{V}$, $V_{SS} = 0\text{V}$ Note 2	-	-	-
Low Level Input Current 1	I_{IL1}	3009	$V_{IN} = 0\text{V}$, $V_{DD} = 5.5\text{V}$ $V_{SS} = 0\text{V}$ Note 3	10 -	1 -10	μA
Low Level Input Current 2	I_{IL2}	3009	$V_{IN} = 0\text{V}$, $V_{DD} = 5.5\text{V}$ $V_{SS} = 0\text{V}$ Note 3	250 -	4 -350	μA
High Level Input Current	I_{IH}	3010	$V_{IN} = 5.5\text{V}$, $V_{DD} = 5.5\text{V}$ $V_{SS} = 0\text{V}$	-	10	μA
Low Level Output Voltage 1	V_{OL1}	3007	$V_{DD} = 4.5\text{V}$, $V_{SS} = 0\text{V}$, $I_{OL} = 4\text{mA}$ Note 4	-	400	mV
Low Level Output Voltage 2	V_{OL2}	3007	$V_{DD} = 4.5\text{V}$, $V_{SS} = 0\text{V}$, $I_{OL} = 12\text{mA}$ Note 4	-	400	mV
High Level Output Voltage 1	V_{OH1}	3006	$V_{DD} = 4.5\text{V}$, $V_{SS} = 0\text{V}$, $I_{OH} = -6\text{mA}$ Note 4	2.4	-	V
High Level Output Voltage 2	V_{OH2}	3006	$V_{DD} = 4.5\text{V}$, $V_{SS} = 0\text{V}$, $I_{OH} = -16\text{mA}$ Note 4	2.4	-	V
Output Leakage Current Third State Low Level Applied	I_{OZL}	3020	Outputs disabled $V_{OUT} = 0\text{V}$, $V_{DD} = 5.5\text{V}$ $V_{SS} = 0\text{V}$	10 -	1 -10	μA

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Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions (Note 1)	Limits		Units
				Min	Max	
Output Leakage Current Third State, High Level Applied	I_{OZH}	3021	Outputs disabled $V_{OUT} = V_{DD} = 5.5V$ $V_{SS} = 0V$	-	10	μA
Supply Current, Power Down	I_{DDPD}	3005	$V_{DD} = 5.5V, V_{SS} = 0V,$ $f = 25MHz$ V_{DDI} Pins Power Down mode	-	41	mA
Supply Current, Operating	I_{DDOP}	3005	$V_{DD} = 5.5V, V_{SS} = 0V,$ $f = 25MHz$ V_{DDI} Pins	-	230	mA
Input Capacitance	C_{IN} C_{IN}	3012	$V_{DD} = 0V, V_{SS} = 0V$ Note 5	-	10	pF
CLK2 period	T_1	3003	$V_{DD} = 4.5$ and $5.5V,$ $V_{SS} = 0V$ Note 6	20	-	ns
SYSCLK Period	T_2	3003	$V_{DD} = 4.5$ and $5.5V,$ $V_{SS} = 0V$ Note 6	40	-	ns
CLK2 High and Low Pulse Width	T_3	3003	$V_{DD} = 4.5$ and $5.5V,$ $V_{SS} = 0V$ Note 6	9.75	-	ns
RA[31-0], RAPAR, RSIZE, RLDSTO and LOCK Output Delay from SYSCLK + Edge	T_4	3003	$V_{DD} = 4.5$ and $5.5V,$ $V_{SS} = 0V$ Note 7	-	6.5	ns
MEMCS[9-0], ROMCS, EXMCS Output Delay from SYSCLK + Edge	T_5	3003	$V_{DD} = 4.5$ and $5.5V,$ $V_{SS} = 0V$ Note 6	-	12.5	ns
DDIR, DDIR Output Delay from SYSCLK + Edge	T_6	3003	$V_{DD} = 4.5$ and $5.5V,$ $V_{SS} = 0V$ Note 6	-	15	ns
MEMWR and IOWR Output Delay from SYSCLK + and SYSCLK-Edge	T_7	3003	$V_{DD} = 4.5$ and $5.5V,$ $V_{SS} = 0V$ Note 7	-	23.5	ns
OE High to Low Output Delay from SYSCLK + Edge	T_8	3003	$V_{DD} = 4.5$ and $5.5V,$ $V_{SS} = 0V$ Note 7	-	20.5	ns
Data Setup Time during Load from SYSCLK + Edge	T_{9-1}	3003	$V_{DD} = 4.5$ and $5.5V,$ $V_{SS} = 0V$ Note 6	11.5	-	ns
Data Setup Time during Load from SYSCLK + Edge	T_{9-2}	3003	$V_{DD} = 4.5$ and $5.5V,$ $V_{SS} = 0V$ Note 7, 8	9	-	ns
Data Hold Time during Load from SYSCLK + Edge	T_{10}	3003	$V_{DD} = 4.5$ and $5.5V,$ $V_{SS} = 0V$ Note 6	5	-	ns

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions (Note 1)	Limits		Units
				Min	Max	
SYSERR, SYSAV Output Delay from SYSCLK + Edge	T ₄₉	3003	V _{DD} = 4.5 and 5.5V, V _{SS} = 0V Note 6	-	20	ns
IUERR Output Delay from SYSCLK + Edge	T ₅₀	3003	V _{DD} = 4.5 and 5.5V, V _{SS} = 0V Note 6	-	20	ns
EXTINT[4-0] Setup Time from SYSCLK- Edge	T ₅₂	3003	V _{DD} = 4.5 and 5.5V, V _{SS} = 0V Note 6	12	-	ns
EXTINT[4-0] Hold Time from SYSCLK-Edge	T ₅₃	3003	V _{DD} = 4.5 and 5.5V, V _{SS} = 0V Note 6	0	-	ns
EXTINTACK Output Delay from SYSCLK + Edge	T ₅₄		V _{DD} = 4.5 and 5.5V, V _{SS} = 0V Note 6	-	15	ns
OE Low to High Output Delay from SYSCLK + Edge (no DMA Mode)	T ₅₆	3003	V _{DD} = 4.5 and 5.5V, V _{SS} = 0V Note 6	-	8.5	ns
BUFFEN Low to High Output Delay from SYSCLK + Edge	T ₅₇	3003	V _{DD} = 4.5 and 5.5V, V _{SS} = 0V Note 6	-	9	ns
INST Output Delay from SYSCLK + Edge	T ₆₀	3003	V _{DD} = 4.5 and 5.5V, V _{SS} = 0V Note 6	-	22	ns
Data Output Delay to Low-Z from SYSCLK + Edge	T ₆₁	3003	V _{DD} = 4.5 and 5.5V, V _{SS} = 0V Note 6	20	-	ns

2.3.2 High and Low Temperatures Electrical Measurements

The measurements shall be performed at T_{amb} = +125 (+0 -5)°C and T_{amb} = -55 (+5 -0)°C.

The characteristics, test methods, conditions and limits shall be the same as specified for Room Temperature Electrical Measurements.

NOTES:

~~2.3.2 Notes to Electrical Measurement Tables~~

- Unless otherwise specified all inputs and outputs shall be tested for each characteristic.
- Functional tests shall be performed at each supply voltage with V_{SYSCLK} = 25MHz, t_r = t_f ≤ 5ns, V_{IL} = 0.8V, V_{IH1} = 2.2V, V_{IH2} = 3V, V_{OL} ≤ 1.45V, V_{OH} ≥ 1.55V. Functionality per the timing diagram specified herein shall be verified. *space*
V_{IH2} applies to inputs RxA/RxB, GPI[7-0], EXTINT[4-0], EWDINT, SYSRESET. V_{IH1} applies to all other inputs.
- I_{IL2} applies to inputs TRST, TMS, TDI. I_{IL1} applies to all other inputs.
- V_{OL2} and V_{OH2} apply to outputs RA[31-0], MEMCS[9-0], MEMWR, OE. V_{OL1} and V_{OH1} apply to all other outputs.
- Guaranteed but not tested.

6. Parameter tested go-no-go at each supply voltage during AC testing with $f_{\text{SYSCLK}} = 25\text{MHz}$, $C_L = 50\text{pF}$, $V_{\text{ref}} = 2.5\text{V}$.
7. Parameter recorded at each supply voltage during AC testing with $f_{\text{SYSCLK}} = 25\text{MHz}$, $C_L = 50\text{pF}$, $V_{\text{ref}} = 2.5\text{V}$.
8. Parameter tested with following conditions: NOPAR = 0, rpa = rec = 0 or 1
(NOPAR: No Parity Input signal; rpa, rec: bit 13 and 14 of Memory Configuration Register)

2.4 PARAMETER DRIFT VALUES

Unless otherwise specified, the measurements shall be performed at $T_{\text{amb}} = +22 \pm 3^\circ\text{C}$.

The test methods and test conditions shall be as per the corresponding test defined in Room Temperature Electrical Measurements.

The drift values (Δ) shall not be exceeded for each characteristic specified. The corresponding absolute limit values for each characteristic shall not be exceeded.

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Characteristics	Symbols	Limits			Units
		Drift Value Δ	Absolute		
			Min	Max	
Low Level Input Current 1	I_{IL1}	± 0.1	+0	-10	μA
High Level Input Current	I_{IH}	± 0.1	-	10	μA
Low Level Output Voltage 1	V_{OL1}	± 100	-	400	mV
Low Level Output Voltage 2	V_{OL2}	± 100	-	400	mV
High Level Output Voltage 1	V_{OH1}	± 0.1	2.4	-	V
High Level Output Voltage 2	V_{OH2}	± 0.1	2.4	-	V
Output Leakage Current Third State, (Low Level Applied)	I_{OZL}	± 0.1	+10 -	-10 -	μA
Output Leakage Current Third State, (High Level Applied)	I_{OZH}	± 0.1	-	10	μA

NOTES:

1. Unless otherwise specified all inputs and outputs shall be tested for each characteristic.

2.5 INTERMEDIATE AND END-POINT ELECTRICAL MEASUREMENTS

Unless otherwise specified, the measurements shall be performed at $T_{\text{amb}} = +22 \pm 3^\circ\text{C}$.

The characteristics, test methods, conditions and limits shall be the same as specified for Room Temperature Electrical Measurements.

2.6 POWER BURN-IN CONDITIONS

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Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	T_{amb}	+ 125 (+ 0, -3)	°C
Input CLK2	V_{IN}	V_{GEN1} (Note 1)	V
Input SYSRESET	V_{IN}	V_{GEN2} (Note 1)	V
All other Inputs and Outputs	V_{IN}, V_{OUT}	V_{DD}, V_{SS} (Note 1)	V
Pulse Voltage	V_{GEN1}, V_{GEN2}	0V to V_{DD}	V
Pulse Frequency Square Wave	f_{GEN1}, f_{GEN2}	1.65M 50.3 (Note 2) 50 ± 15% Duty Cycle $t_r = t_f \leq 5ns$	Hz
Positive Supply Voltage V_{DDO}, V_{DDI}	V_{DD}	5 (+ 0.5, -0)	V
Negative Supply Voltage V_{SSO}, V_{SSI}	V_{SS}	0	V

NOTES:

1. All Inputs and Outputs shall be connected through a serial protection resistor/load as follows:

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Pin	Signal	Wired to:	Serial Resistor	Pin	Signal	Wired to:	Serial Resistor
1	GPI[INT]	V_{DD}	5.6k Ω	24	V_{DDO}	V_{DD}	N/A
2	GPI[7]	V_{DD}	1k Ω	25	V_{SSO}	V_{SS}	N/A
3	V_{DDO}	V_{DD}	N/A	26	D[25]	V_{SS}	1k Ω
4	V_{SSO}	V_{SS}	N/A	27	D[24]	V_{SS}	1k Ω
5	GPI[6]	V_{DD}	1k Ω	28	D[23]	V_{DD}	1k Ω
6	GPI[5]	V_{DD}	1k Ω	29	D[22]	V_{SS}	1k Ω
7	GPI[4]	V_{DD}	1k Ω	30	V_{DDO}	V_{DD}	N/A
8	GPI[3]	V_{DD}	1k Ω	31	V_{SSO}	V_{SS}	N/A
9	V_{DDO}	V_{DD}	N/A	32	D[21]	V_{SS}	1k Ω
10	V_{SSO}	V_{SS}	N/A	33	D[20]	V_{DD}	1k Ω
11	GPI[2]	V_{DD}	1k Ω	34	D[19]	V_{DD}	1k Ω
12	GPI[1]	V_{DD}	1k Ω	35	D[18]	V_{SS}	1k Ω
13	GPI[0]	V_{DD}	1k Ω	36	V_{DDO}	V_{DD}	N/A
14	D[31]	V_{DD}	1k Ω	37	V_{SSO}	V_{SS}	N/A
15	D[30]	V_{DD}	1k Ω	38	D[17]	V_{SS}	1k Ω
16	V_{DDO}	V_{DD}	N/A	39	D[16]	V_{SS}	1k Ω
17	V_{SSO}	V_{SS}	N/A	40	V_{DDI}	V_{DD}	N/A
18	D[29]	V_{SS}	1k Ω	41	V_{SSI}	V_{SS}	N/A
19	D[28]	V_{SS}	1k Ω	42	D[15]	V_{SS}	1k Ω
20	V_{DDI}	V_{DD}	N/A	43	D[14]	V_{SS}	1k Ω
21	V_{SSI}	V_{SS}	N/A	44	V_{DDO}	V_{DD}	N/A
22	D[27]	V_{SS}	1k Ω	45	V_{SSO}	V_{SS}	N/A
23	D[26]	V_{DD}	1k Ω	46	D[13]	V_{SS}	1k Ω

Pin	Signal	Wired to:	Serial Resistor	Pin	Signal	Wired to:	Serial Resistor
227	VSS0	VSS	N/A	242	MHOLD	VDD	5.6kΩ
228	MEMCS[2]	VDD	5.6kΩ	243	MDS	VDD	5.6kΩ
229	MEMCS[1]	VDD	5.6kΩ	244	WDCLK	VSS	1kΩ
230	MEMCS[0]	VDD	5.6kΩ	245	IWDE	VSS	1kΩ
231	VDDI	VDD	N/A	246	EWDINT	VSS	1kΩ
232	VSSI	VSS	N/A	247	TMODE[1]	VSS	1kΩ
233	OE	VDD	5.6kΩ	248	TMODE[0]	VSS	1kΩ
234	VDDO	VDD	N/A	249	DEBUG	VSS	1kΩ
235	VSSO	VSS	N/A	250	INULL	VDD	5.6kΩ
236	MEMWR	VDD	5.6kΩ	251	DIA	VDD	5.6kΩ
237	BUFFEN	VDD	5.6kΩ	252	VDDO	VDD	N/A
238	DDIR	VDD	5.6kΩ	253	VSSO	VSS	N/A
239	VDDO	VDD	N/A	254	FLUSH	VDD	5.6kΩ
240	VSSO	VSS	N/A	255	INST	VDD	5.6kΩ
241	DDIR	VDD	5.6kΩ	256	RTC	VDD	5.6kΩ

2. $f_{GEN2} = f_{GEN1} / 2^{15}$.

2.7 OPERATING LIFE CONDITIONS

The conditions shall be as specified for **power burn-in**.

2.8 TOTAL DOSE IRRADIATION TESTING

2.8.1 Bias Conditions and Total Dose Level for Total Dose Radiation Testing

Continuous bias shall be applied during irradiation testing as specified below.

The total dose level applied shall be as specified in the component type variant information herein or in the **Purchase Order**.

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Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	T_{amb}	22 ± 3	°C
Input CLK2	V_{IN}	V_{GEN1} (Note 1)	V
All other Inputs and Outputs	V_{IN}, V_{OUT}	V_{DD}, V_{SS} (Note 1)	V
Pulse Voltage	V_{GEN1}	0V to V_{DD}	V
Pulse Frequency Square Wave	f_{GEN1}	≤ 100 $50 \pm 15\%$ Duty Cycle $t_r = t_f \leq 500ns$	Hz
Positive Supply Voltage V_{DDO}, V_{DDI}	V_{DD}	5 (+0.5, -0)	V
Negative Supply Voltage V_{SSO}, V_{SSI}	V_{SS}	0	V

NOTES:

- All Inputs and Outputs shall be connected through a serial protection resistor/load as defined for burn-in with the exception that Pin 198 SYSRESET shall be connected to V_{SS} through 1kΩ serial resistor.