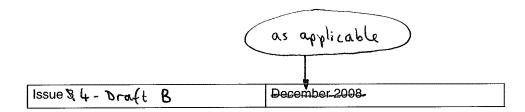


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# TRANSISTORS, LOW POWER, PNP

### **BASED ON TYPE 2N4033**

**ESCC Detail Specification No. 5202/008** 







as applicable

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## **DOCUMENTATION CHANGE NOTICE**

(Refer to https://escies.org for ESCC DCR content)

| 423, 447 Specification up issued to incorporate editorial and technical changes per DCR. |  |
|--|--|

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#### 1.5 **MAXIMUM RATINGS**

The maximum ratings shall not be exceeded at any time during use or storage.

Maximum ratings shall only be exceeded during testing to the extent specified in this specification and when stipulated in Test Methods and Procedures of the ESCC Generic Specification.

| Characteristics                               | Symbols           | Maximum Ratings  | Unit | Remarks                                      |
|---|-------------------|------------------|------|--|
| Collector-Base Voltage                        | V <sub>CBO</sub>  | -80              | ٧    | Over entire                                  |
| Collector-Emitter Voltage                     | V <sub>CEO</sub>  | -80              | ٧    | operating<br>temperature                     |
| Emitter-Base Voltage                          | V <sub>EBO</sub>  | -5               | ٧    | range  |
| Collector Current                             | I <sub>C</sub>    | 1                | Α    | Continuous                                   |
| Power Dissipation<br>For TO-39<br>For CCP     | P <sub>tot1</sub> | 800<br>500       | mW   | At T <sub>amb</sub> ≤ +25°C<br>Note <b>n</b> |
| FOR CENTRAL PROPERTY                          | JPtot2            | J 760 (Note 2) J | DW.  | in   |
| For TO-39                                     | P <sub>tot3</sub> | 800              | mW   | At T <sub>case</sub> ≤ +25°0  Voten          |
| Operating Temperature Range                   | T <sub>op</sub>   | -65 to +200      | °C   | Note 🖫 2                                     |
| Storage Temperature Range                     | T <sub>stg</sub>  | -65 to +200      | °C   | Note & 2_                                    |
| Soldering Temperature<br>For TO-39<br>For CCP | T <sub>sol</sub>  | +260<br>+245     | °C   | Note 4 3<br>Note 5 4                         |

ses attached

**NOTES:** 

Eor T<sub>amb</sub>-or T<sub>case</sub> > +25°C, derate linearly-to-0W at +200°C.

-When-mounted-on-a-15-x-15-x-0-6mm-ceramic-substrate.

For Variants with tin-lead plating or hot solder dip lead finish all testing performed at T<sub>amb</sub> > +125°C shall be carried out in a 100% inert atmosphere.

Duration 10 seconds maximum at a distance of not less than 1.5mm from the device body and the same lead shall not be resoldered until 3 minutes have elapsed.

Duration 5 seconds maximum and the same terminal shall not be resoldered until 3 minutes have

1. Thermal Resistance, Junction-to-Case only applies to 70-39 packaged Variants.

| Thermal Resistance, |               |              |      |                      |
|---------------------|---------------|--------------|------|----------------------|
| Junction-to-Ambient | $R_{th(j-a)}$ | 218.8<br>350 | °C/W | For TO-39<br>For CCP |
| Thermal Resistance, |               |              |      |                      |
| Junction-to-Case    | $R_{th(j-c)}$ | 218.8        | °C/W | Note 1               |



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| Characteristics                      | Symbols              | Lin | Units |    |
|--------------------------------------|----------------------|-----|-------|----|
|                                      |                      | Min | Max   |    |
| Collector-Base Cut-off Current       | I <sub>CBO</sub>     | -   | -50   | nA |
| Collector-Emitter Saturation Voltage | V <sub>CE(sat)</sub> | -   | -150  | mV |
| Forward-Current Transfer Ratio 2     | h <sub>FE2</sub>     | 100 | 300   | -  |

#### 2.7 <u>HIGH TEMPERATURE REVERSE BIAS BURN-IN CONDITIONS</u>

| Characteristics        | Symbols          | Test Conditions | Units |
|------------------------|------------------|-----------------|-------|
| Ambient Temperature    | T <sub>amb</sub> | +150(+0 -5)     | °C    |
| Emitter-Base Voltage   | V <sub>EB</sub>  | 4               | V     |
| Collector-Base Voltage | V <sub>CB</sub>  | 40              | V     |
| Duration               | t                | 48 minimum      | hours |

#### 2.8 POWER BURN-IN CONDITIONS

| Characteristics        | Symbols          | Test Conditions  | Units |
|------------------------|------------------|--|-------|
| Ambient Temperature    | T <sub>amb</sub> | +20 to +50   | °C    |
| Power Dissipation      | P <sub>tot</sub> | As per Maximum Ratings.  Ptot1 disrated at the chosen  Tamb Ms ing the | W     |
| Collector-Base Voltage | V <sub>CB</sub>  | -40  | V     |

2.9

**OPERATING LIFE CONDITIONS** 

The conditions shall be as specified for Power Burn-in.

specified Rth(j-a).

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#### **APPENDIX 'A'**



#### AGREED DEVIATIONS FOR STMICROELECTRONICS (F

| ITEMS AFFECTED   | DESCRIPTION OF DEVIATIONS   |
|--|---|
| Deviations from<br>Production Control-<br>Chart F2                         | Special In-process Control Internal Visual Inspection. For CCP packages the criteria specified for voids in the fillet and minimum die mounting material around the visible die perimeter for die mounting defects may be omitted providing that a radiographic inspection to verify the die-attach process is performed on a sample basis in accordance with STMicroelectronics procedure 0076637. |
| Deviations from Room<br>Temperature Electrical<br>Measurements             | All AC characteristics (Room Temperature Electrical Measurement Note 2) may be considered guaranteed but not tested if successful pilot lot testing has been performed on the wafer lot which includes AC characteristic measurements per the Detail Specification.  A summary of the pilot lot testing shall be provided if required by the Purchase Order.  |
| Deviations from High<br>and Low Temperatures<br>Electrical<br>Measurements | All characteristics specified may be considered guaranteed but not tested if successful pilot lot testing has been performed on the wafer lot which includes characteristic measurements at high and low temperatures per the Detail Specification. A summary of the pilot lot testing shall be provided if required by the Purchase Order.   |
| Deviations from<br>Screening Tests -<br>Chart F3                           | Solderability is not applicable unless specifically stipulated in the Purchase Order.   |