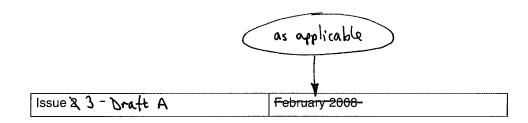


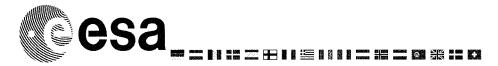
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# TRANSISTORS, MATCHED DUAL, PNP

# **BASED ON TYPE 2N3350**

# **ESCC Detail Specification No. 5207/003**







as applicable

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## **DOCUMENTATION CHANGE NOTICE**

(Refer to https://escies.org for ESCC DCR content)

DCR No.	CHANGE DESCRIPTION
\$857339	Specification up issued to incorporate editorial and technical changes per DCRs.

447, thad



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when stipulated in Test Methods and Procedures of the ESCC Generic Specification.

Characteristics	Symbols	Maximum Ratings	Unit	Remarks
Collector-Base Voltage	V <sub>CBO</sub>	-60	V	Over entire
Collector-Emitter Voltage	V <sub>CEO</sub>	-45	V	operating temperature
Emitter-Base Voltage	V <sub>EBO</sub>	-6	V	range
Collector Current	I <sub>C</sub>	30	mA	Continuous
Power Dissipation (One Section)				At T <sub>amb</sub> ≤ +25°0
For TO-77 and CCP	P <sub>totO1</sub>	0.3	W	
For COPY .	150 PM	J Q.6 (Nbte.2)	JW	MUNI
For TO-77	Ptoto 3 2	0.6	W	At T <sub>case</sub> ≤ +25°0 NoteNs
Power Dissipation (Both Sections)				At T <sub>amb</sub> ≤ +25°0
For TO-77 and CCP	P <sub>totB1</sub>	0.6	w	
FOR DEPLY STATES	NEW BY	J J. 2 Wode & J	JW	m
For TO-77	PtotBy 2	1.2	W	At T <sub>case</sub> ≤ +25°C
Operating Temperature Range	T <sub>op</sub>	-55 to +200	°C	Note 및 2_
Storage Temperature Range	T <sub>stg</sub>	-65 to +200	°С	Note § 2
Soldering Temperature For TO-77 For CCP	T <sub>sol</sub>	+260 +245	°C	Note 🐒 3 Note 🗞 4

see

#### **NOTES:**

FOR Tamb OF Tease >+25°C, derate linearly to OW at +2000s. Thermal Resistance, Junction-to-case

-When mounted on a 15 x 15 x 0.6mm ceramic substrate.

2. Tor Variants with tin-lead plating or hot solder dip lead finish all testing performed at Tamb > +125°C shall be carried out in a 100% inert atmosphere.

Duration 10 seconds maximum at a distance of not less than 1.5mm from the device body and the same lead shall not be resoldered until 3 minutes have elapsed.

Duration 5 seconds maximum and the same terminal shall not be resoldered until 3 minutes have elapsed.

only applies to TO-77 packaged Variants.

Thermal Resistance,				
Junction-to-Ambient	$R_{th(j-a)}$	583.3	°C/W	For one section
		291.7		For both sections
Thermal Resistance,				
Junction-to-Case	R <sub>th(j-c)</sub>	291.7	°c/w	For one section
		145.8		For both sections
				Note 1

Characteristics	Symbols	MIL-STD-750	Test Conditions	Lin	nits	Units
		Test Method		Min	Max	
Small-Signal Input Impedance	h <sub>ie</sub>	3201	I <sub>C</sub> =-1mA V <sub>CE</sub> =-5V f=1kHz Note 2	3.7	20	kΩ
Small-Signal Output Impedance	h <sub>oe</sub>	3216	I <sub>C</sub> =-1mA V <sub>CE</sub> =-5V f=1kHz Note 2	-	100	μmho
Noise Figure	NF	3246	$I_C$ =-10μA $V_{CE}$ =-5V $R_S$ =10k $\Omega$ BW=15.7kHz Note 2	-	4	dB

#### **NOTES:**

- 1. Pulse measurement: Pulse Width  $\leq 300\mu s$ , Duty Cycle  $\leq 2\%$ .
- 2. For AC characteristics read and record measurements shall be performed on a sample of 32 components with 0 failures allowed. Alternatively a 100% inspection may be performed.

#### 2.4.2 <u>High and Low Temperatures Electrical Measurements</u>

Characteristics	Symbols MIL-STD-7 Test Metho		Test Conditions	Limits		Units	
			Note 1	Min Max			
Collector-Base Cut-off Current	Ісво	3036	T <sub>amb</sub> =+150(+0-5)°0 V <sub>CB</sub> =-45V, Blas Condition D	-	-10	μА	
Forward-Current Transfer Ratio 2	h <sub>FE2</sub>	3076	T <sub>amb</sub> =-55(+5-0)°C I <sub>C</sub> =-1mA V <sub>CE</sub> =-5V	70	-	-	5
Forward-Current Transfer Ratio Comparison	h <sub>FE1-1</sub> / h <sub>FE1-2</sub>	3076	$T_{amb}$ =-55 to +125°C $I_{C}$ =-10 $\mu$ A ; $V_{CE}$ =-5V	0.9	1.1	-	
Base-Emitter Voltage Differential Change	IΔ(V <sub>BE1</sub> - V <sub>BE2</sub> )ΔT <sub>amb</sub> l 1	3066	T <sub>amb</sub> =-55(+5-0)° to +25±3°C I <sub>C</sub> =-10μA V <sub>CE</sub> =-5V	-	800	μV	J
	IΔ(V <sub>BE1</sub> - V <sub>BE2</sub> )ΔT <sub>amb</sub> l 2	3066	$T_{amb}$ =+25±3°C to +125(+5-0)°C $I_{C}$ =-10 $\mu$ A $V_{CE}$ =-5V	-	1000		

## **NOTES:**

1. Read and record measurements shall be performed on a sample of 5 components with 0 failures allowed. Alternatively a 100% inspection may be performed.

#### 2.5 PARAMETER DRIFT VALUES

Unless otherwise specified, the measurements shall be performed at  $T_{amb}$ =+22  $\pm 3^{\circ}$ C.



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## 2.7 <u>HIGH TEMPERATURE REVERSE BIAS BURN-IN CONDITIONS</u>

Characteristics	Symbols	Test Conditions	Units
Case Temperature	T <sub>case</sub>	+150 (+0 -5)	°C
Collector-Base Voltage	V <sub>CB</sub>	-60	٧
Emitter-Base Voltage	V <sub>EB</sub>	-6	٧
Duration	t	72 minimum	hrs

### 2.8 <u>POWER BURN-IN CONDITIONS</u>

Characteristics	Symbols	Test Conditions	Units*
Ambient Temperature	T <sub>amb</sub>	+25#3 to +50	°C
Power Dissipation (Both Sections)	P <sub>totB</sub>	As per Maximum Ratings P <sub>totB1</sub>	W
Collector-Base Voltage	V <sub>CB</sub>	-30	V

2.9 OPERATING LIFE CONDITIONS

The conditions shall be as specified for Power Burn-in.

using the specified Rth (j-a).

.Derate



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P

APPENDIX 'A'

<u>5</u>-

# AGREED DEVIATIONS FOR STMICROELECTRONICS (F)

	ITEMS AFFECTED	DESCRIPTION OF DEVIATIONS
Р	Deviations from Production Control- Chart F2	Special In process Control Internal Visual Inspection. For CCP packages the criteria specified for voids in the fillet and minimum die mounting material around the visible die perimeter for die mounting defects may be omitted providing that a radiographic inspection to verify the die-attach process is performed on a sample basis in accordance with STMicroelectronics procedure 0076637.
Т	Deviations from Room Temperature Electrical Measurements	All AC characteristics (Room Temperature Electrical Measurement Note 2) may be considered guaranteed but not tested if successful pilot lot testing has been performed on the wafer lot which includes AC characteristic measurements per the Detail Specification.  A summary of the pilot lot testing shall be provided if required by the Purchase Order.
a E	eviations from High nd Low Temperatures lectrical leasurements	All characteristics specified may be considered guaranteed but not tested if successful pilot lot testing has been performed on the wafer lot which includes characteristic measurements at high and low temperatures per the Detail Specification.  A summary of the pilot lot testing shall be provided if required by the Purchase Order.
D	eviations from	Solderability is not applicable unless specifically
5	eviations from creening Tests - chart F3	Solderability is not applicable unless specifically stipulated in the Purchase Order.
(	hart F3	

(Approved DCR 447 refers)