TRANSISTORS, POWER, MOSFET, N-CHANNEL, RAD-HARD

BASED ON TYPE STRH8N10

ESCC Detail Specification No. 5205/023

TABLE OF CONTENTS

1.	**GENERAL**	
1.1	Scope	4
1.2	Applicable Documents	4
1.3	Terms, Definitions, Abbreviations, Symbols and Units	4
1.4	The ESCC Component Number and Component Type Variants	4
1.4.1	The ESCC Component Number	4
1.4.2	Component Type Variants	4
1.5	Maximum Ratings	5
1.6	Handling Precautions	7
1.7	Physical Dimensions and Terminal Identification	7
1.8	Functional Diagram	8
1.9	Materials and Finishes	8
2.	**REQUIREMENTS**	
2.1	General	8
2.1.1	Deviations from the Generic Specification	9
2.1.1.1	Deviations from Screnning Tests – Chart F3	9
2.1.1.2	Deviations from Qualification and Periodic Tests - Chart F4	9
2.2	Wafer Lot Acceptance	
2.3	Marking	9
2.4	Terminal Strength	9
2.5	Electrical Measurements at Room, High and Low Temperatures	9
2.5.1	Room Temperature Electrical Measurements	10
2.5.2	High and Low Temperatures Electrical Measurements	11
2.5.3	Notes to Room,High and Low Electrical Measurement Tables	11
2.6	Parameter Drift Values	12
2.7	Intermediate and End-Point Electrical Measurements	12
2.8	High Temperature Reverse Bias Burn-in Conditions	13
2.9	High Temperature Forward Bias Burn-in conditions	13
2.10	Operating Life Conditions	13
2.11	Total Dose Radiation Testing	14
2.11.1	Bias Conditions and Total Dose Level for Total Dose Radiation Testing	14
2.11.2	Electrical Measurements for Total Dose Radiation Testing	14

APPENDIX ‘A’

1. GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics and test and inspection data for the component type variants and/or the range of components specified below. It supplements the requirements of, and shall be read in conjunction with, the ESCC Generic Specification listed under Applicable Documents.

1.2 APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:

(a) ESCC Generic Specification No. 5000

(b) MIL-STD-750, Test Methods and Procedures for Semiconductor Devices

1.3 TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESCC Basic Specification No. 21300 shall apply.

1.4 THE ESCC COMPONENT NUMBER AND COMPONENT TYPE VARIANTS

1.4.1 The ESCC Component Number

The ESCC Component Number shall be constituted as follows:

Example: 520502301F

- Detail Specification Reference: 5205023
- Component Type Variant Number: 01 (as required)
- Total Dose Radiation Level Letter:F (as required)

1.4.2 Component Type Variants

The component type variants applicable to this specification are as follows:

Variant Number	Based on Type	Case	Lead/Terminal Material and Finish	Weight max g	Total Dose Radiation Level Letter
01	STRH8N10	SMD.5	Q14	2	F[70kRAD/Si]

The lead/terminal material and finish shall be in accordance with the requirements of ESCC Basic Specification No. 23500.

Total dose radiation level letters are defined in ESCC Basic Specification No. 22900. If an alternative radiation test level is specified in the Purchase Order the letter shall be changed accordingly.

1.5 MAXIMUM RATINGS

The maximum ratings shall not be exceeded at any time during use or storage.
Maximum ratings shall only be exceeded during testing to the extent specified in this specification and when stipulated in Test Methods and Procedures of the applicable ESCC Generic Specification.

Characteristics	Symbols	Maximum Ratings	Unit	Remarks
Drain-Source Voltage	V_{DS}	100	V	Over Top V_{GS}=0V Note 2
Gate-Source Voltage	V_{GS}	±20	V	Over Top
Drain Current	I_{DS}	6	A	Continuous At T_{case} ≤ +25°C Note 1
		4.1	A	Continuous At T_{case} >+100°C Note 1
Drain Current (pulsed)	I_{DM}	24	A	Note 2
Power Dissipation	P_{TOT}	25	W	AtT_{case} ≤ +25°C Note 1
Avalanche Energy (Single Pulse)	E_{AS}	 457 134	mJ	V_{DS}=50V I_{AS}=4A T_j=+25±3°C T_j=+110 (+0 -5°C)
Avalanche Energy (Repetitive Pulse)	E_{AR}	 4.3 1.4	mJ	V_{DS}=50V I_{AR}=4A f=100kHz Duty Cycle= 10% T_j=+25±3°C T_j=+110 (+0 -5°C)
Operating Temperature Range	Top	-55 to +150	°C	Note 3
Junction Temperature	Tj	+150	°C	
Storage Temperature Range	Tstg	-55 to +150	°C	Note 3
Soldering Temperature	Tsol	+260	°C	Note 4
ThermalResistance, Junction-to-Heat Sink	$R_{th(J-S)}$	 ~~5~~ 2	°C/W	Note 5
ThermalResistance, Junction-to-Ambient	$Rth_{(J-A)}$	 ~~175~~ 52	°C/W	

NOTES:

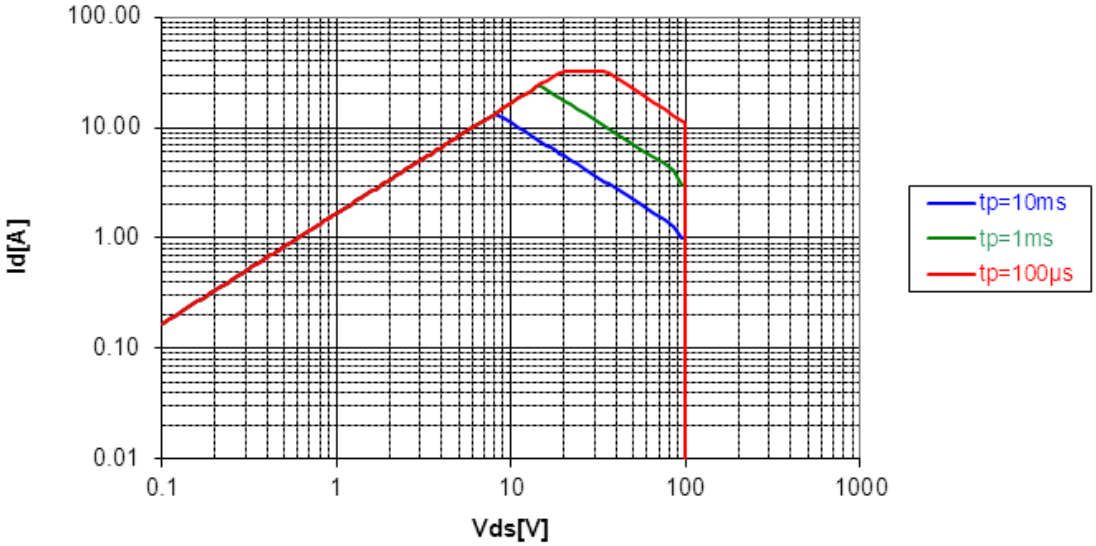
1. I_{DS} and P_{tot} ratings are in accordance with $R_{th(j-s)}$. The maximum theoretical I_D limit at T_{case} > +25°C can be obtained by using the following formula (I_D is limited by the package and device construction):

$$I_D = \sqrt{\frac{T_{j(max)} - T_{Case}}{R_{th(j-s)} \; x \; R_{DS}(on) \; at \; T_{j(max)}}}$$

Where ($r_{DS(on)}$ at Tj(max) = 720mΩ
For T_{case} > +25°C, the power Dissipation derates linearly to 0W at T_{case} = +150°C

2. Safe Operating Area applies as follows:

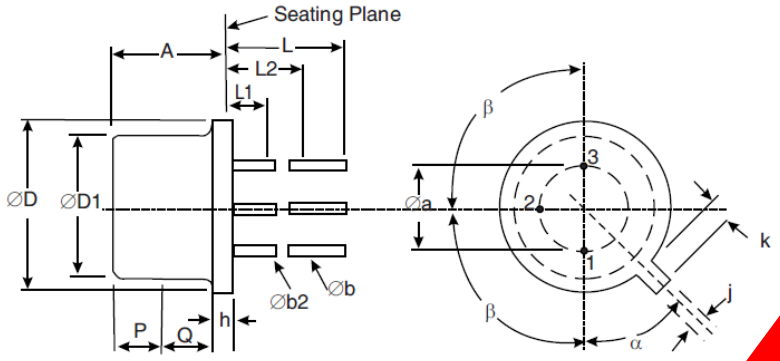
Maximun Safe Operating Area



3. For Variants with hot solder dip lead finish all testing performed at Tamb>+125°C shall be carried out in a 100% inert atmosphere.
4. Duration 10 seconds maximum at a distance of not less than 1.5mm from the device body and the same lead shall not be resoldered until 3 minutes have elapsed.
5. Package mounted on infinite heatsink..

1.6 PHYSICAL DIMENSIONS AND TERMINAL IDENTIFICATION

~~Metal can Package (TO39) - 3 Lead~~

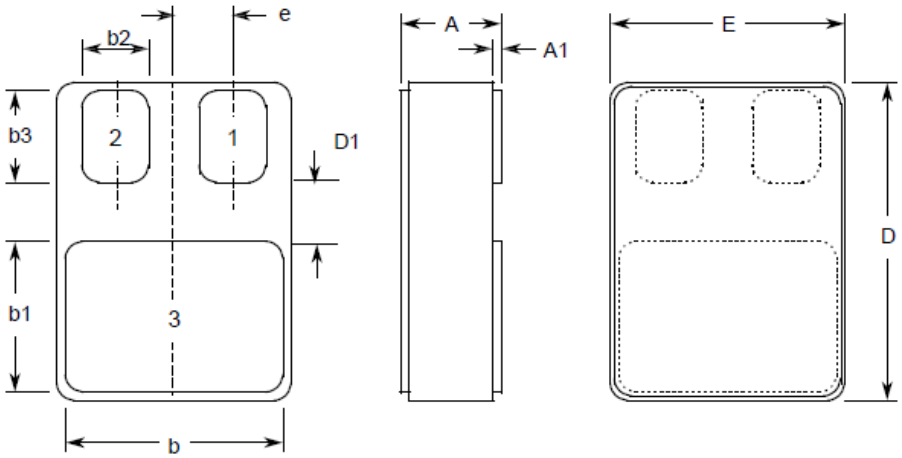


Symbols	Dimensions mm		Notes
	Min	Max	
Øa	4.83	5.35	
A	6	6.6	
Øb	0.4	0.533	
Øb2	0.4	0.483	, 3
ØD	8.31	9.4	
ØD1	7.75	8.51	
h	0.229	3.18	
j	0.71	0.864	
k	0.737	1.1	4
L	12.7		2
L1	-		2, 3
L2	6.35	-	2, 3
P	2.54	-	5
Q	-	-	6
α		SC	1, 7
β		BSC	1

NOTES:

1. Terminal identification specified by reference to the tab position where Lead 1 = emitter, Lead 2 = base and Le = collector.
2. Applies to all lead
3. Øb2 applies be en L1 and L2. Øb applies between L1 and 12.7mm from the seating plane. Diameter ncontrolled within L1 and beyond 12.7mm from the seating plane.
4. Measured fr the maximum diameter of the actual device.
5. This zone controlled for automatic handling. The variation in actual diameter within this zone shall not exce .254mm.
6. The ails of outline in this zone are optional.
7. M ured from the tab centreline.

Surface Mount Package (SMD.5) - 3 Terminal

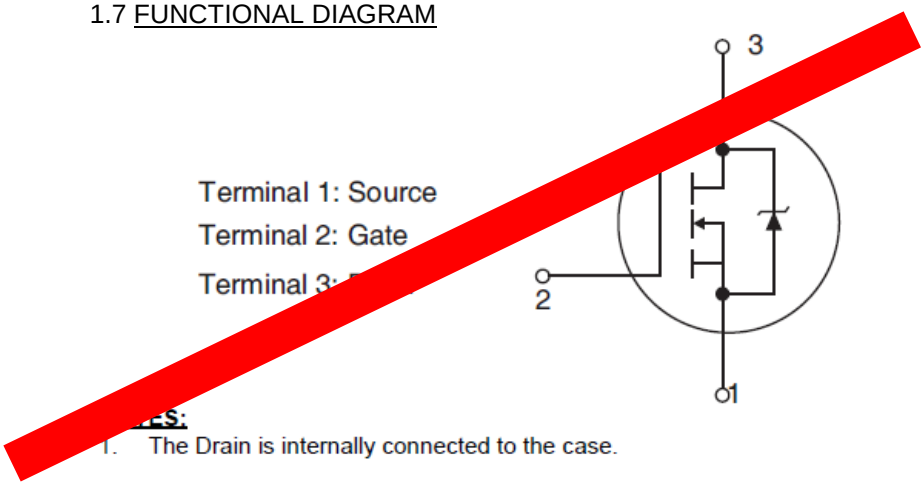


Symbols	Dimensions mm		Notes
	Min	Max	
A	2.84	3.15	
A1	0.25	0.51	
b	7.13	7.39	
b1	5.58	5.84	
b2	2.28	2.54	2
b3	2.92	3.18	2
D	10.03	10.28	
D1	0.76	-	2
E	7.39	7.64	
e	1.91 BSC		2

NOTES:

1. The terminal identification is specified by the component's geometry. See Functional Diagram for the terminal connections.
2. 2 places.

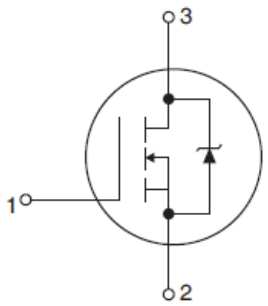
1.7 FUNCTIONAL DIAGRAM



ES:

1. The Drain is internally connected to the case.

Terminal 1: Gate
Terminal 2: Source
Terminal 3: Drain



NOTES:
1. The lid is not connected to any terminal.

1.8 MATERIALS AND FINISHES

Materials and finishes shall be as follows:

a) Case

~~For the metal can package, the case shall be hermetically sealed and have a metal body with hard glass seals.~~

For the surface mount package the case shall be hermetically sealed and have a ceramic body with a Kovar lid.

b) Leads/Terminals

As specified in Component Type Variants.

2. REQUIREMENTS

2.1 GENERAL

The complete requirements for procurement of the components specified herein are as stated in this specification and the ESCC Generic Specification. Permitted deviations from the Generic Specification, applicable to this specification only, are listed below.

Permitted deviations from the Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESCC requirement and do not affect the component's reliability, are listed in the appendices attached to this specification.

2.1.1 Deviations from the Generic Specification

2.1.1.1 Deviations from Screening Tests - Chart F3

- Verification of Safe Operating Area

The Safe Operating Area shall be verified by performing the VSD test specified in Room Temperature Electrical Measurements (Thermal Resistance, Junction-to-Heat Sink).

- A High Temperature Forward Bias test shall be performed instead of Power Burn-in.

2.1.1.2 Deviations from Qualification and Periodic Tests - Chart F4

(a) Constant Acceleration is omitted.

(b) For SMD.5 Terminal Strength is not applicable

2.2 WAFER LOT ACCEPTANCE

A SEM inspection shall be performed as defined in Chart F2 and Para 5.2.2 of the ESCC Generic Specification.

2.3 MARKING

The marking shall be in accordance with the requirements of ESCC Basic Specification No. 21700 and as follows.

The information to be marked on the component shall be:

(a) The ESCC Qualified components symbol (for ESCC qualified components only).

(b) The ESCC Component Number.

(c) Traceability information (Date Code).

2.4 TERMINAL STRENGTH

~~The test conditions for terminal strength, tested as specified in the ESCC Generic Specification, shall be as follows:~~

~~For T039, Test Condition: E, lead fatigue.~~
Terminal strength is not applicable for the SMD.5

2.5 ELECTRICAL MEASUREMENTS AT ROOM, HIGH AND LOW TEMPERATURES
Electrical measurements shall be performed at room, high and low temperatures. Consolidated notes are given after the tables.

2.5.1 Room Temperature Electrical Measurements
The measurements shall be performed at Tamb=+22 ±3°C.

Characteristics	Symbols	MIL-STD-750 Test Method	Test Conditions	Limits		Units
				Min	Max	
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	3407	V_{GS}=0V I_D=1mA Bias Condition C	100	-	V
Gate-to-Source Leakage Current	I_{GSSF1}	3411	V_{GS}=+20V Bias Condition C, V_{DS}=0V	-	+100	nA
	I_{GSSR1}	3411	V_{GS}=-20V Bias Condition C, V_{DS}=0V	-100	-	nA
Drain Current	I_{DSS}	3413	V_{DS}=80% of rated B_{VDSS} Bias Condition C, V_{GS}=0V	-	10	µA
Gate-Source-Voltage (threshold)	$V_{GS(th)}$	3403	V_{GS}=V_{DS} I_D= 1mA	2	4.5	V
Static Drain-to-Source on resistance	$r_{DS(ON)}$	3421	I_D=4A V_{GS}=12V Note 1	-	0.3	Ω
Forward Voltage	V_{SD}	4011	I_{SD}=8A V_{GS}=0V Note 1	-	1.5	V
Thermal Resistance Junction-to-Heat Sink	Rth(j-s)	3161	Note 2	-	5	°C/W
Input capacitance	Ciss	3431	V_{GS}=+0V V_{DS}=25V f=1MHz	527	791	pF
Output capacitance	Coss	3453		76	114	pF
Reverse transfert capacitance	Crss	3433		31	47	pF
Total Gate Charge	Q_g	3471	V_{DD}=50V I_D=4A V_{GS}=12V	15	22	nC
Gate to Source charge	Q_{gs}			~~3~~ 2.5	~~5~~ 4.5	nC nC
Gate to Drain charge	Q_{gd}			~~4~~ 3.5	~~7~~ 6	nC nC
Turn-on delay time	$t_{d(on)}$	3472	V_{DD}=50V I_D=4A R_G=4.7Ω V_{GS}=12V	~~6~~ 5	~~15~~ 10	ns ns
Rise time	t_r			~~4~~ 2	~~17~~ 9	ns ns
Turn-off delay time	$t_{d(off)}$			13	30	ns
Fall time	tf			~~3~~ 2.5	~~8~~ 7.5	ns ns
Reverse Recovery Time	t_{rr}	3473	V_{DS}=50V I_{SD}=8A di/dt=100A/µs Tj=+25 ±3°C	196	294	ns

2.5.2 High and Low Temperatures Electrical Measurements

Characteristics	Symbols	MIL-STD-750 Test Method	Test Conditions Note 3	Limits		Units
				Min	Max	
Gate-to-Source Leakage Current	I_{GSSF1}	3411	V_{GS}=+20V Bias Condition C, V_{DS}=0V Tcase= +125 (+0-5)°C	-	+200	nA
	I_{GSSR1}	3411	V_{GS}=-20V Bias Condition C, V_{DS}=0V Tcase= +125 (+0-5)°C	-200	-	nA
Drain Current	I_{DSS}	3413	V_{DS}=80% of rated B_{VDSS} Bias Condition C, V_{GS}=0V Tcase= +125 (+0-5)°C	-	100	µA
Gate-Source Voltage (threshold)	$V_{GS(th)}$	3403	V_{GS}=V_{DS} I_D= 1mA Tcase= +125 (+0-5)°C	1.5	3.7	V
			V_{GS}=V_{DS} I_D= 1mA Tcase= -55 (+5-0)°C	2.1	5.5	V
Static Drain-to-Source on resistance	$r_{DS(ON)}$	3421	I_D=4A V_{GS}=12V Note 1 Tcase= +125 (+0-5)°C		0.72	Ω
Forward Voltage	V_{SD}	4011	I_D=8A V_{GS}=0V Note 1 Tcase= +125 (+0-5)°C		1.275	V

2.5.3 Notes to Electrical Measurement Tables

1) Pulse Width≤300µs, Duty Cycle≤2%.
2) The Rth(j-s) limit is guaranteed by performing a ΔV_{SD} (go-no-go) test. The following test conditions and limits shall apply:

~~a. V_{DS} = 6V~~
~~b. I_D = 4~~
~~c. I~~ ~~5mA~~
~~d. ~~ulse = 20ms~~
~~e. tcal = 50µs~~
f. ~~V_{SD} = 100mV minimum, 190mV maximum~~.

a. V_{DS} = 6V
b. I_D = 4.26A
c. Ical = 5mA
d. tpulse = 20ms
e. tcal = 50µs
f. V_{SD} = 140mV minimum, 250mV maximum.

3) Read and record measurements shall be performed on a sample of 5 components with 0 failures allowed. Alternatively a 100% inspection may be performed.

2.6 PARAMETER DRIFT VALUES

Unless otherwise specified, the measurements shall be performed at Tamb=+22 ±3°C.
The test methods and test conditions shall be as per the corresponding test defined in Room Temperature Electrical Measurements.
The drift values (Δ) shall not be exceeded for each characteristic specified. The corresponding absolute limit values for each characteristic shall not be exceeded.

Characteristics	Symbols	Limits			Units
		Drift Value	Absolute		
		Δ	Min	Max	
Gate-to-Source Leakage Current	I_{GSSF1}	± 50 or (1) ± 100%	-	+100	nA
	I_{GSSR1}	± 50 or (1) ± 100%	-100	-	nA
Drain Current	I_{DSS}	±4 or (1) ±100%	-	10	µA
Gate-Source Voltage (threshold)	$V_{GS(th)}$	± 5%	2	4.5	V
StaticDrain-Source on resistance	$R_{DS(ON)}$	± 10%	-	0.3	Ω

NOTES:
1. Whichever is the greater referred to the initial value.

2.7 INTERMEDIATE AND END-POINT ELECTRICAL MEASUREMENTS

Unless otherwise specified, the measurements shall be performed at Tamb=+22 ±3°C.
The test methods and test conditions shall be as per the corresponding test defined in Room Temperature Electrical Measurements.
The limit values for each characteristic shall not be exceeded.

Characteristics	Symbols	MIL-STD-750 Test Method	Test Conditions	Limits		Units
				Min	Max	
Drain Current	I_{DSS}	3413	V_{DS}=80% of rated B_{VDSS} Bias Condition C, V_{GS}=0V	-	10	µA
Gate-Source Voltage (threshold)	$V_{GS(th)}$	3403	V_{GS}=V_{DS} I_D= 1mA	2	4.5	V
StaticDrain-Source on resistance	$r_{DS(ON)}$	3421	I_D=4A V_{GS}=12V Note 1		0.3	Ω

2.8 HIGH TEMPERATURE REVERSE BIAS CONDITIONS

HTRB Burn-in shall be performed in accordance with MIL-STD-750, Test Metho 1042, Test Condition A with the following conditions:

Characteristics	Symbols	Test Conditions MIL-STD-750 Test Method 1042 Cond A	Units
Ambient Temperature	Tamb	+150	°C
Drain to Source	V_{DS}	+80	V
Duration	-	240	hrs

2.9 HIGH TEMPERATURE FORWARD BIAS CONDITIONS.

HTFB Burn-in shall be performed in accordance with MIL-STD-750, Test Metho 1042, Test Condition B with the following conditions:

Characteristics	Symbols	Test Conditions MIL-STD-750 Test Method 1042 Cond B	Units
Ambient Temperature	Tamb	+150	°C
Gate to Source	V_{GS}	+16	V
Duration	-	48	hrs

2.10 OPERATING LIFE CONDITIONS

Operating Life shall be performed in accordance with MIL-STD-750, Test Metho 1042, Test Condition A (HTRB) and B (HTFB) with the following conditions:

HIGH TEMPERATURE REVERSE BIAS CONDITIONS (HTRB)

Characteristics	Symbols	Test Conditions MIL-STD-750 Test Method 1042 Cond A	Units
Ambient Temperature	Tamb	+150	°C
Drain to Source	V_{DS}	+80	V
Duration	-	1000	hrs

HIGH TEMPERATURE FORWARD BIAS CONDITIONS (HTFB or HTGB)

Characteristics	Symbols	Test Conditions MIL-STD-750 Test Method 1042 Cond B	Units
Ambient Temperature	Tamb	+150	°C
Gate to Source	V_{GS}	+16	V
Duration	-	1000	hrs

2.11 TOTAL DOSE RADIATION TESTING

All lots shall be irradiated in accordance with ESCC Basic Specification No.22900, standard dose rate (window 1: 3.6kRAD to 36kRAD per hour).

2.11.1 Bias Conditions and Total Dose Level for Total Dose Radiation Testing

The following bias condition (worst-case) shall be used for Total Dose Radiation Testing at T_{amb}=22±3°C:

With V_{GS} bias = +15V and V_{DS}=0V during irradiation.

The total dose level applied shall be as specified in the component type variant information herein or in the Purchase order.

2.11.2 Electrical Measurements for Total Dose Radiation Testing

Prior to irradiation testing the devices shall have successfully met Room Temperature Electrical Measurements specified herein.

Unless otherwise stated the measurements shall be performed at T_{amb}=22 ± 3°C.

Unless otherwise specified the test methods and test conditions shall be as per the corresponding test defined in Room Temperature Electrical Measurements.

The parameters to be measured during and on completion of irradiation testing, after 24 hours anneal at Room Temperature and after 168 hours anneal at +100±3°C are shown below.

Characteristics	**Symbols**	**Limits**
		Drift Values (Δ)
Drain-to-source Voltage (Note 1)	V_{DSS}	-25 %
Gate-to-Source Leakage Current 1	I_{GSS1}	+/- 1.5 nA
Gate-to-Source Leakage Current 2	I_{GSS2}	+/- 1.5 nA
Drain Current	I_{DSS}	+ 1µA
Gate-to-Source Threshold Voltage	$V_{GS(th)}$	-60 % / + 30 %
Static Drain-to-Source On Resistance (TO-3)	$r_{DS(on)}$	+/- 10%
Source-to-Drain Diode Forward Voltage	V_{SD}	+/- 2 %
Total Gate Charge [(a)]	Q_g	-5% / +40%
Gate-to-Source Charge [(a)]	Q_{gs}	+/- 35%
Gate-to-Drain Charge [(a)]	Q_{gd}	-5% / +130%

(a) Parameter not measured after irradiation but guaranteed by the results obtained during the evaluation phase that proves this parameter is directly correlated to the V_{GSth} shift.

APPENDIX 'A'

AGREED DEVIATIONS FOR STMICROELECTRONICS (F)

ITEMS AFFECTED	DESCRIPTION OF DEVIATIONS
Deviations from Room Temperature Electrical Measurements	The AC characteristics Ciss, Coss, Crss, Qg, Qgs, Qgd, td(on), tr, td(off), tf and trr may be considered guaranteed but not tested if successful pilot lot testing has been performed on the wafer lot in accordance with STMicroelectronics procedure 8212069, which includes AC (Ciss, Coss, Crss, Qg, Qgs, Qgd, td(on), tr, td(off), tf and trr) characteristic measurements per the Detail Specification. A summary of the pilot lot testing shall be provided if required by the Purchase Order.
Deviations from Electrical Measurements for Total Dose Radiation Testing	The AC characteristics Qg, Qgs and Qgd need not be measured because they are guaranteed by the results obtained by STMicroelectronics during the evaluation phase which proved these characteristics are directly correlated to the VGS(th) shift.
Deviations from Screening Tests –Chart F3	Solderability is not applicable unless specifically stipulated in the Purchase Order.

ADDITIONAL DATA – STMICROELECTRONICS (F)

Heavy ions characterization has been done on STRH100N10 part. But STRH8N10 is based on the same technology and same epitaxy. The results obtained on STRH100N10 are transposable to the STRH8N10.

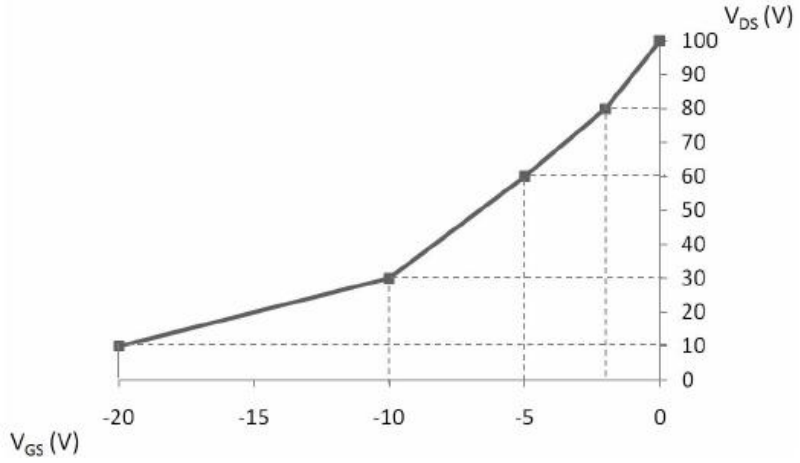
(a) Derating for Space Application

These components are susceptible to Single Event Gate Rupture if operated in a space environment unless the following derating is applied. The derating for space applications was originally obtained on STRH100N10 devices under the following test conditions. The testing was performed in a vacuum at UCL (Louvain-la-Neuve, Belgium):

Ion used = Kr
LET = 32 (MeV / (mg/cm2))
Energy = 768 MeV
Range = 94 μm

$V_{DS} \leq 100V$	When	$V_{GS} = 0V$
$V_{DS} \leq 80V$	When	$V_{GS} = -2V$
$V_{DS} \leq 60V$	When	$V_{GS} = -5V$
$V_{DS} \leq 30V$	When	$V_{GS} = -10V$
$V_{DS} \leq 10V$	When	$V_{GS} = -20V$

Single Event Effect Safe Operating Area (for STRH100N10)



Justification:
Delete the TO-39, this package does not meet of customer expectations (no space market demand). ST has not manufactured and sold any products in this version (TO-39).

A Contrary the SMD.5 is requested, the ESCC qualification has been done according this package and also from new silicon for which the thickness of the gate oxide is 470Å instead of 350Å on the previous one➔ meaning a review of the limits (mainly AC test parameters).