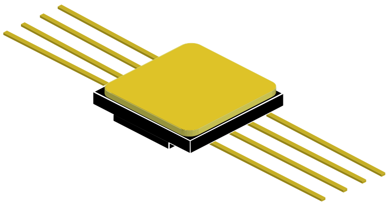
ST1843, ST1845

Rad-tolerant current mode PWM controller

Datasheet - production data



Flat-8

Features

- Oscillator frequency guaranteed at 250 kHz
- Trimmed oscillator for precise frequency control
- Current mode operation to 500 kHz automatic feed forward compensation
- Latching PWM for cycle-by-cycle current limiting
- Internally trimmed reference with undervoltage lockout
- High current totem pole output
- Undervoltage lockout with hysteresis
- Low start-up and operating current
- Hermetic package
- 50 and 100 krad (Si)
- SEL free @ 120 MeV/cm2/mg at 125 °C
- ESCC qualified

Description

The ST1843 and ST1845 ICs are rad-tolerant current mode PWM controllers providing an industry standard solution for the implementation of off-line or DC to DC fixed frequency current mode control schemes with a minimal external part count.

Its radiation hardness, hermetic packaging and its ESCC qualification make it an ideal choice for aerospace and other harsh environments.

Table 1: Device summary

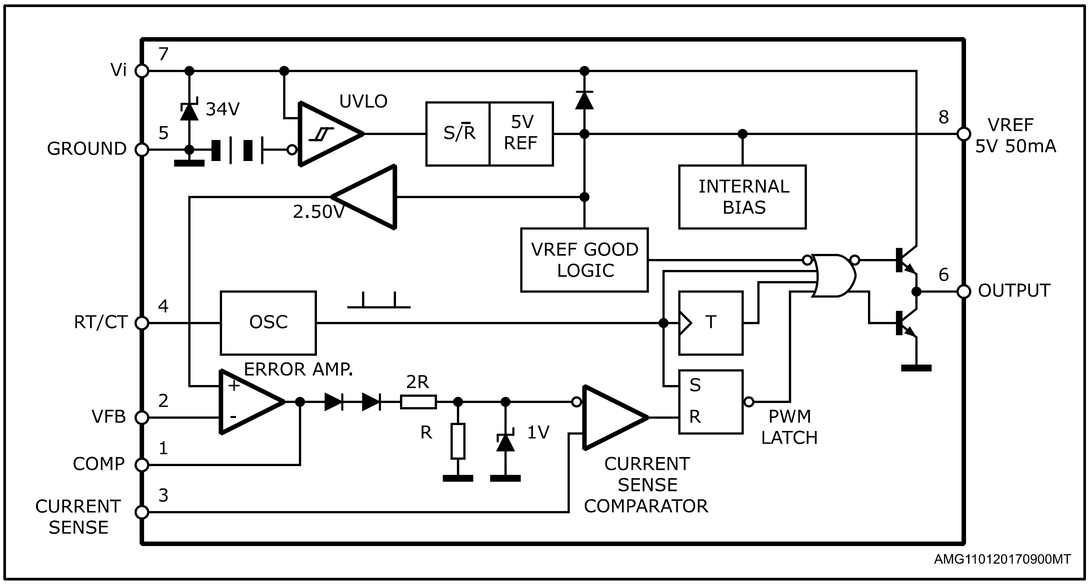
Order code	Detailed specification	Quality level	Radiation level	EPPL	Duty cycle max.	Lead finish	Package	Mass (g)
ST1843K1	-	Engineering model	-	-	100 %	Gold	Flat-8	0.45
ST1843FKG	9108/020/01F	ESCC	100 krad(si)	Target				
ST1843FKT	9108/020/02F					Solder dip		
ST1845K1	-	Engineering model	-	-	50 %	Gold		
ST1845RKG	9108/021/01R	ESCC	50 krad(si)	Target				
ST1845RKT	9108/021/02R					Solder dip		

Contact STMicroelectronics sales office for information about die specific conditions and other quality levels.

Contents

1 Block diagram

Figure 1: Block diagram (toggle flip flop used only in ST1845)



2 Maximum ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_i	Supply voltage (low impedance source)	30	V
	Supply voltage (Ii < 30 mA)	Self limiting	
I_O	Output current	±1	A
E_O	Output energy (capacitive load)	5	µJ
	Analog inputs (pins 2, 3)	-0.3 to 5.5	V
	Error amplifier output sink current	10	mA
P_{tot}	Power dissipation at $T_A \leq 25$ °C	800	mW
T_{stg}	Storage temperature range	-55 to 150	°C
T_J	Junction operating temperature	-55 to 150	°C

All voltages are with respect to pin 5, all currents are positive into the specified terminal.

3 Thermal data

Table 3: Thermal data

Symbol	Description	Flat-8	Unit
R_{thJA}	Thermal resistance junction-ambient max.	100	°C/W

4 Pin connection

Figure 2: Pin connection

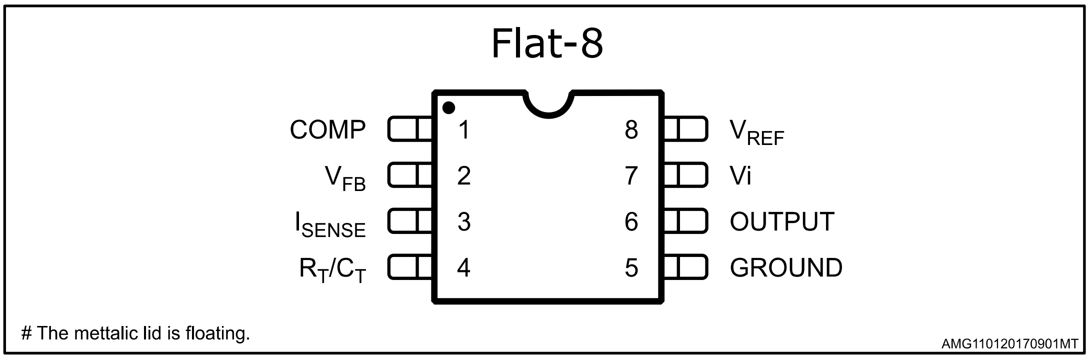


Table 4: Pin functions

No	Function	Description
1	COMP	This pin is the error amplifier output and is made available for loop compensation.
2	V_{FB}	This is the inverting input of the error amplifier. It is normally connected to the switching power supply output through a resistor divider.
3	I_{SENSE}	A voltage proportional to inductor current is connected to this input. The PWM uses this information to terminate the output switch conduction.
4	R_T/C_T	The oscillator frequency and maximum output duty cycle are programmed by connecting resistor RT to Vref and capacitor CT to ground. Operation to 500 kHz is possible.
5	GROUND	This pin is the combined control circuitry and power ground.
6	OUTPUT	This output directly drives the gate of a power MOSFET. Peak currents up to 1 A are sourced and sunk by this pin.
7	V_{CC}	This pin is the positive supply of the control IC.
8	V_{ref}	This is the reference output. It provides charging current for capacitor CT through resistor RT.

5 Electrical characteristics

Maximum package power dissipation limits must be respected; low duty cycle pulse techniques are used during test maintain T_J as close to T_A as possible.

Unless otherwise stated, these specifications apply for -T_A = 22 ±3 °C, V_i = 15 V, Adjust V_i above the start threshold before setting at 15 V; R_T = 10 kΩ; C_T = 3.3 nF.

Table 5: Electrical characteristics

Symbol	MIL-STD-883 test method	Parameter	Test conditions	Values		Unit
				Min.	Max.	
Reference section						
V_{REF}		Output voltage	V_I = 15 V; R_T = 10 kΩ; C_T = 3.3 nF; I_O = 1 mA	4.95	5.05	V
ΔV_{REF_LINE}		Line regulation	12 V ≤ V_I ≤ 25 V; R_T = 10 kΩ; C_T = 3.3 nF		0.02	V
ΔV_{REF_LOAD}		Load regulation for ST1843	V_I = 15 V; R_T = 10 kΩ; C_T = 3.3 nF; 1 ≤ I_O ≤ 20 mA		19	mV
		Load regulation for ST1845			25	
I_{SC}	3011	Output short circuit		-0.18	-0.03	A
Oscillator section						
f_{OSC}		Frequency for ST1843	V_I = 15 V; R_T = 10 kΩ; C_T = 3.3 nF; 1 ≤ I_O ≤ 20 mA	49	55	kHz
		Frequency for ST1845		24.5	27.5	
$\Delta f_{OSC}/\Delta_V$		Frequency change with voltage	12 V ≤ V_I ≤ 25 V; R_T = 10 kΩ; C_T = 3.3 nF	-	1	%
I_{dischg}		Discharge current for ST1843	V_I = 15 V; R_T = 10 kΩ; C_T = 3.3 nF; 1 ≤ I_O ≤ 20 mA; V_{OSC} = 2 V	8.1	8.8	mA
		Discharge current for ST1845		8.3		
Error amp section						
V_{FB}		Input voltage	V_I = 15 V; R_T = 10 kΩ; C_T = 3.3 nF; V_{PIN1} = 2.5 V	2.45	2.55	V
I_b	4001	Input bias current	V_I = 15 V; R_T = 10 kΩ; C_T = 3.3 nF; V_{FB} = 5 V	-1		µA

Symbol	MIL-STD-883 test method	Parameter	Test conditions	Values		Unit
				Min.	Max.	
A_{VOL}		A_{VOL}	V_I = 15 V; R_T = 10 kΩ; C_T = 3.3 nF; 2 V ≤ V_O ≤ 4 V	65		dB
PSRR	4003	Power supply rejec. ratio for ST1843	12 V ≤ V_i ≤ 25 V; R_T = 10 kΩ; C_T = 3.3 nF	67		dB
		Power supply rejec. ratio for ST1845		68		
I_{o_sink}		Output sink current	V_I = 15 V; R_T = 10 kΩ; C_T = 3.3 nF; V_{PIN2} = 2.7 V; V_{PIN1} = 1.1 V	6		mA
I_{o_source}		Output source current	V_I = 15 V; R_T = 10 kΩ; C_T = 3.3 nF; V_{PIN2} = 2.2 V; V_{PIN1} = 5 V		-1	mA
V_{OH}		V_{OUT} high for ST1843	V_I = 15 V; R_T = 10 kΩ; C_T = 3.3 nF; V_{PIN2} = 2.3 V; R_L = 15 kΩ to GND	6.2		V
		V_{OUT} high for ST1845		5.4		
V_{OL}		V_{OUT} low	V_I = 15 V; R_T = 10 kΩ; C_T = 3.3 nF; V_{PIN2} = 2.3 V; R_L = 15 kΩ to GND		0.95	V
Current sense section						
G_V	4004	Gain	V_I = 15 V; R_T = 10 kΩ; C_T = 3.3 nF[(1)(2)]	2.85	3.15	V/V
V_3		Maximum input signal	V_I = 15 V; R_T = 10 kΩ; C_T = 3.3 nF; V_{PIN1} = 2.3 V[(1)]	0.9	1.05	V
SVR		Supply voltage rejection for ST1843	12 ≤ V_i ≤ 25 V; R_T = 10 kΩ; C_T = 3.3 nF;	74		dB
		Supply voltage rejection for ST1845		72		
I_b	4001	Input bias current	V_I = 15 V; R_T = 10 kΩ; C_T = 3.3 nF	-10		µA
D_O	3003	Delay to output	V_I = 15 V; R_T = 10 kΩ; C_T = 3.3 nF		300	ns

Symbol	MIL-STD-883 test method	Parameter	Test conditions	Values		Unit
				Min.	Max.	
Output section						
V_{OL1}	3007	Output low level for ST1843	V_I = 15 V; R_T = 10 kΩ; C_T = 3.3 nF; I_{SINK} = 20 mA		0.26	V
		Output low level for ST1845			0.18	
V_{OL2}		Output low level	V_I = 15 V; R_T = 10 kΩ; C_T = 3.3 nF; I_{SINK} = 200 mA		2.2	V
V_{OH1}	3006	Output high level	V_I = 15 V; R_T = 10 kΩ; C_T = 3.3 nF; I_{SOURCE} = 20 mA	13		V
V_{OH2}			V_I = 15 V; R_T = 10 kΩ; C_T = 3.3 nF; I_{SOURCE} = 200 mA	12		V
V_{OLS}		UVLO saturation	V_I = 6 V; R_T = 10 kΩ; C_T = 3.3 nF; I_{SINK} = 1 mA		1.1	V
t_r	3004	Rise time	V_I = 15 V; R_T = 10 kΩ; C_T = 3.3 nF; C_L = 1 nF		150	ns
t_f		Fall time			150	ns
Under-voltage lockout section						
V_{TH}		Start threshold	V_I = 15 V; R_T = 10 kΩ; C_T = 3.3 nF	7.8	9	V
V_{MIN}		Min operating voltage after turn-on for ST1843	V_I = 15 V; R_T = 10 kΩ; C_T = 3.3nF	7	8.2	V
		Min operating voltage after turn-on for ST1845			8	
DC_{MAX}		Max duty cycle for ST1843	V_I = 15 V; R_T = 10 kΩ; C_T = 3.3 nF	47	50	%
		Max duty cycle for ST1845		94	100	%
DC_{MIN}		Min duty cycle	V_I = 15 V; R_T = 10 kΩ; C_T = 3.3 nF		0	%

Symbol	MIL-STD-883 test method	Parameter	Test conditions	Values		Unit
				Min.	Max.	
Total standby current						
I_{st}		Start-up current	V_I = 15 V; R_T = 10 kΩ; C_T = 3.3 nF		0.5	mA
I_i	3005	Operating supply current	V_I = 15 V; R_T = 10 kΩ; C_T = 3.3 nF; V_{PIN2} = V_{PIN3} = 0 V		17	mA
V_{iz}		Zener voltage	V_I = 15 V; R_T = 10 kΩ; C_T = 3.3 nF; I_i = 25 mA	30		V

Notes:

(1)Parameter measured at trip point of latch with V_{PIN2} = 0.

(2)Gain defined as:

$$A = \frac{\Delta V_{PIN1}}{\Delta V_{PIN3}}; 0 \leq \Delta V_{PIN3} \leq 0.8V$$

6 Radiation characteristics

6.1 Total dose

The total dose results are provided in the following table:

Table 6: Total dose performance

Device	Total dose
ST1843	50 krad (Si)
ST1845	100 krad (Si)

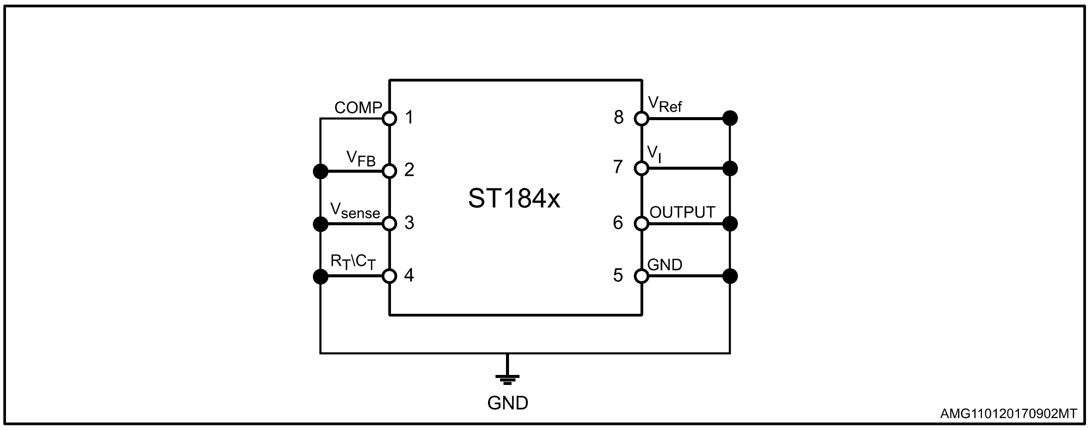
These results are obtained on the following conditions:

6.1.1 Bias conditions and total dose level for total dose radiation testing

Continuous bias shall be applied during irradiation testing as specified below.

The total dose level applied shall be as specified in the component type variant information here in or in purchaser order.

Figure 3: Unbias conditions



6.1.2 Electrical measurements for total dose radiation testing

Prior to irradiation testing the devices shall have successfully met room temperature electrical measurements specified herein.

Unless otherwise stated the measurements shall be performed at T_A = +22 ±3 °C.

The test methods and test conditions shall be as per the corresponding test defined in electrical measurements at room temperature. The parameters to be measured during and on completion of irradiation testing are shown below.

Table 7: Electrical parameter during irradiation testing

Symbol	Parameter	Test conditions	Values		Unit
			Min.	Max.	
Reference section					
V_{REF}	Output voltage for ST1843	V_I = 15 V; R_T = 10 kΩ; C_T = 3.3 nF; I_O = 1 mA	4.85	5.15	V
	Output voltage for ST1845			5.15	
ΔV_{REF_LINE}	Line regulation	12 V ≤ V_i ≤ 25 V; R_T = 10 kΩ; C_T = 3.3 nF		0.02	V
ΔV_{REF_LOAD}	Load regulation	V_I = 15 V; R_T = 10 kΩ; C_T = 3.3 nF; 1 ≤ I_o ≤ 20 mA		0.025	V
I_{SC}	Output short circuit current	V_I = 15 V; R_T = 10 kΩ; C_T = 3.3 nF	-0.18	-0.03	A
Oscillator section					
F_{OSC}(1)	Frequency	V_I = 15 V; R_T = 10 kΩ; C_T = 3.3 nF	49	65	kHz
ΔF_{OSC} / ΔV	Frequency change with voltage	12 V ≤ V_i ≤ 25 V; R_T = 10 kΩ; C_T = 3.3 nF	-1	1	%
IDISCHG	Discharge current	V_I = 15 V; R_T = 10 kΩ; C_T = 3.3 nF; V_{OSC} = 2 V	0.0078	0.0088	A

Symbol	Parameter	Test conditions	Values		Unit
			Min.	Max.	
Error amp section					
V_2	Input voltage for ST1843	V_I = 15 V; R_T = 10 kΩ; C_T = 3.3 nF; V_{PIN1} = 2.5 V	2.45	2.6	V
	Input voltage for ST1845		2.45	2.55	
I_b	Input bias current ST1843	V_I = 15 V; R_T = 10 kΩ; C_T = 3.3 nF; V_{FB} = 5 V	-2.75		µA
	Input bias currentST1845		-2.8		
AVOL	AVOL for ST1843	V_I = 15 V; R_T = 10 kΩ; C_T = 3.3 nF; 2 V ≤ V_o ≤ 4 V	60		dB
	AVOL for ST1845		62		
PSRR	Power supply rejection ratio	12 V ≤ V_i ≤ 25 V; R_T = 10 kΩ; C_T = 3.3 nF	60		dB
IO_SINK	Output sink current	V_I = 15 V; R_T = 10 kΩ; C_T = 3.3 nF; V_{PIN2} = 2.7 V; V_{PIN1} = 1.1 V	2		mA
IO_SOURCE	Output source current	V_I = 15 V; R_T = 10 kΩ; C_T = 3.3 nF; V_{PIN2} = 2.3 V; V_{PIN1} = 5 V		-0.5	mA
V_{OH}	VOUT high	V_I = 15 V; R_T = 10 kΩ; C_T = 3.3 nF; V_{PIN2} = 2.3 V; RL = 15 K to GND	5		V
V_{OL}	VOUT low	V_I = 15 V; R_T = 10 kΩ; C_T = 3.3 nF; V_{PIN2} = 2.3 V; R_L = 15 kΩ to pin		1.1	V

Symbol	Parameter	Test conditions	Values		Unit
			Min.	Max.	
Current sense section					
G_V	Gain	V_I = 15 V; R_T = 10 kΩ; C_T = 3.3 nF	2.85	3.15	V/V
V3	Maximum input signal	V_I = 15 V; R_T = 10 kΩ; C_T = 3.3 nF; V_{PIN1} = 2.3 V	0.9	1.1	V
SVR	Supply voltage rejection	12 V ≤ V_i ≤ 25 V; R_T = 10 kΩ; C_T = 3.3 nF;	60		dB
I_b	Input bias currentST1843	V_I = 15 V; R_T = 10 kΩ; C_T = 3.3 nF	-50		µA
	Input bias currentST1845		-45		
D_O	Delay to output	V_I = 15 V; R_T = 10 kΩ; C_T = 3.3 nF		300	ns
Output section					
V_{OL1}	Output low level	V_I = 15 V; R_T = 10 kΩ; C_T = 3.3 nF; I_{SINK} = 20 mA		0.4	V
V_{OL2}	Output low level	V_I = 15 V; R_T = 10 kΩ; C_T = 3.3 nF; I_{SINK} = 200 mA		2.2	V
V_{OH1}	Output high level	V_I = 15 V; R_T = 10 kΩ; C_T = 3.3 nF; I_{SOURCE} = 20 mA	13		V
V_{OH2}	Output high level	V_I = 15 V; R_T = 10 kΩ; C_T = 3.3 nF; I_{SOURCE} = 200 mA	12		V
V_{OLS}	UVLO saturation	V_I = 15 V; R_T = 10 kΩ; C_T = 3.3 nF; I_{SINK} = 1 mA		1.1	V
T_R	Rise time	V_I = 15 V; R_T = 10 kΩ; C_T = 3.3 nF; C_L = 1 nF		180	ns
T_F	Fall time	V_I = 15 V; R_T = 10 kΩ; C_T = 3.3 nF; C_L = 1 nF		180	ns

Symbol	Parameter	Test conditions	Values		Unit
			Min.	Max.	
Under-voltage lockout section					
V_{TH}	Start threshold for ST1843	V_I = 15 V; R_T = 10 kΩ; C_T = 3.3 nF	7.8	9.5	V
	Start threshold for ST1845		7.8	10.5	
V_{MIN}	Min operating voltage after turn-on for ST1843	V_I = 15 V; R_T = 10 kΩ; C_T = 3.3 nF	7	8.6	V
	Min operating voltage after turn-on forST1845		7	9	
DCMAX	Max duty cycle for ST1843	V_I = 15 V; R_T = 10 kΩ; C_T = 3.3 nF	94	100	%
	Max duty cycle for ST1845		47	50	
DCMIN	Min duty cycle	V_I = 15 V; R_T = 10 kΩ; C_T = 3.3 nF		0	%
Total stand-by current					
I_{ST}	Start-up current	V_I = 6.5 V; R_T = 10 kΩ; C_T = 3.3 nF		0.5	mA
I_i	Operating supply current	V_I = 15 V; R_T = 10 kΩ; C_T = 3.3 nF; V_{PIN2} = V_{PIN3} = 0 V		17	mA
Viz	Zener voltage	V_I = 15 V; R_T = 10 kΩ; C_T = 3.3 nF; I_i = 25 mA	30		V

Notes:

(1)For ST1845 the limits applies to the internal frequency of the device before the output divider by 2. The limits for the external frequency are divide by 2 ,i.e. 24.5 kHz min and 32.5 kHz max.

6.1.3 Heavy Ions

Both devices have been tested SEL free at 120 MeV/cm^2/mg at 125 °C.

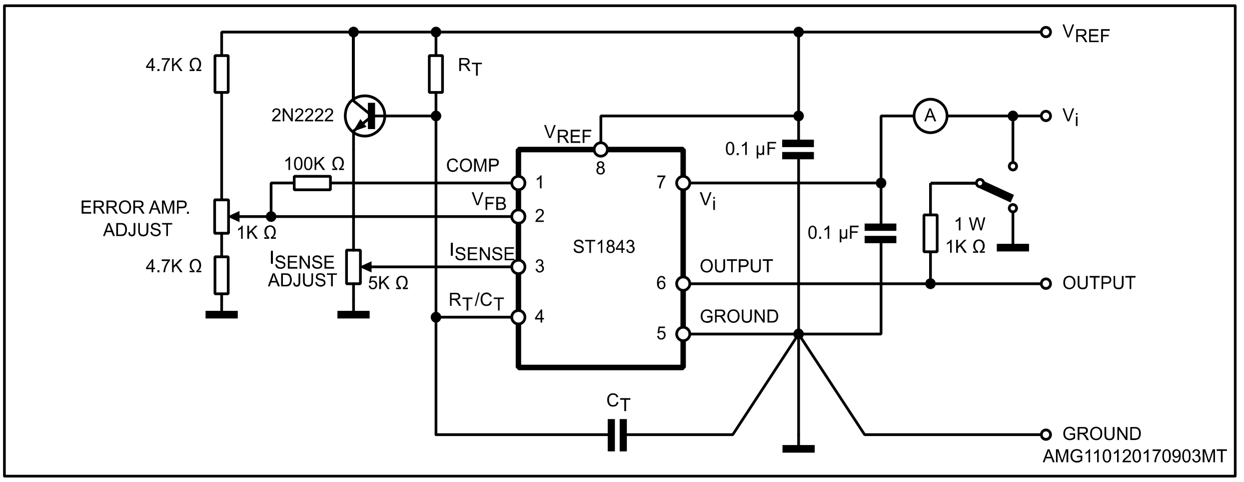
The heavy ions trials are performed on qualification lots only.

Table 8: SEE Hardness summary

Type	Characteristics	Value	Unit
SEL	Immunity at 30 V, 125 °C, 60 °C tilt	120	MeV.cm^2/mg
SET	Threshold	1.5	
	Saturated cross section	1.10$^{(-2)}$	cm^2

7 Test circuit

Figure 4: Open loop test circuit



High peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to pin 5 in a single point ground. The transistor and 5 kΩ potentiometer are used to sample the oscillator waveform and apply an adjustable ramp to pin 3.

Figure 5: Timing resistor vs oscillator frequency

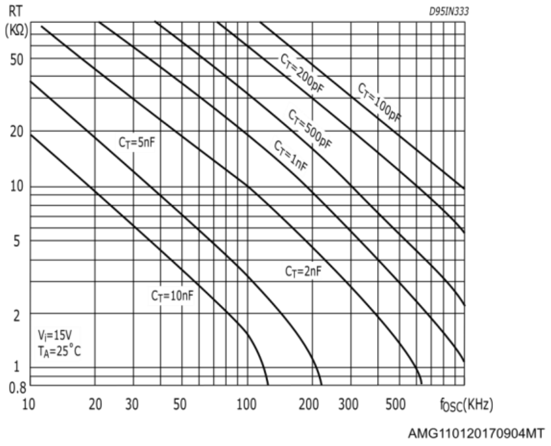


Figure 6: Output dead-time vs oscillator frequency

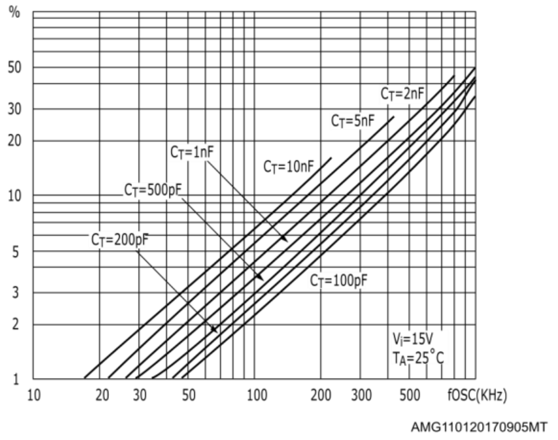


Figure 7: Oscillator discharge current vs temperature

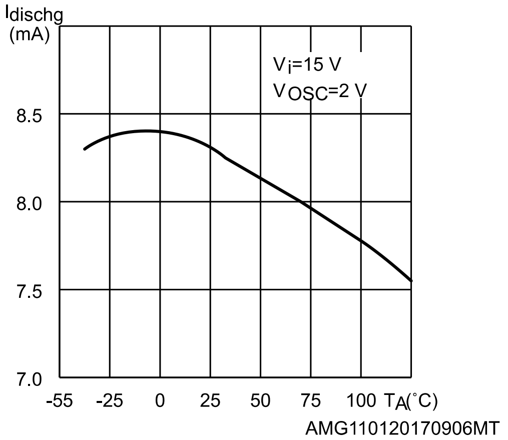


Figure 8: Maximum output duty cycle vs timing resistor

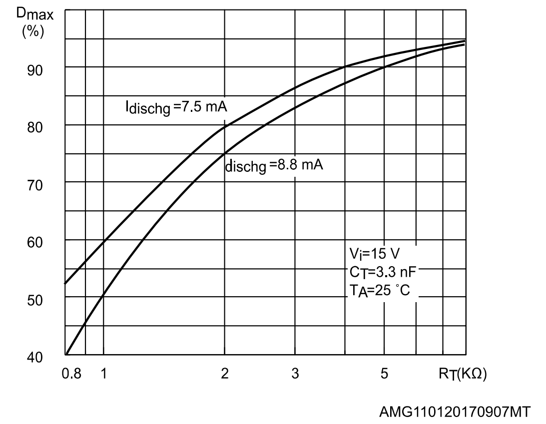


Figure 9: Error amp open-loop gain and phase vs frequency

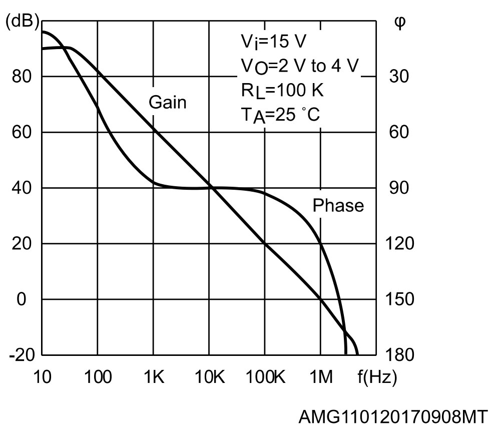


Figure 10: Current sense input threshold vs error amp output voltage

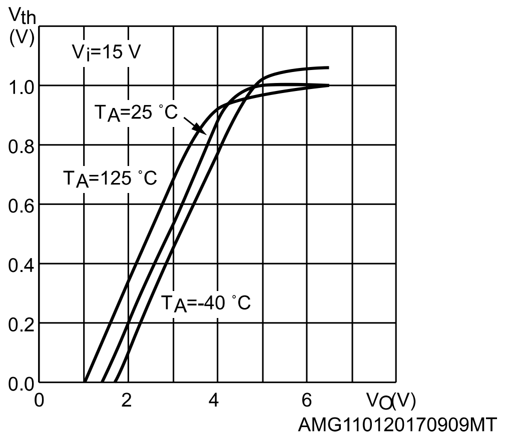


Figure 11: Reference voltage change vs source current

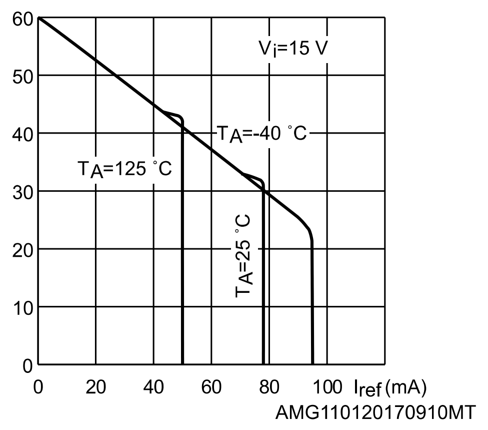


Figure 12: Reference short circuit current vs temperature

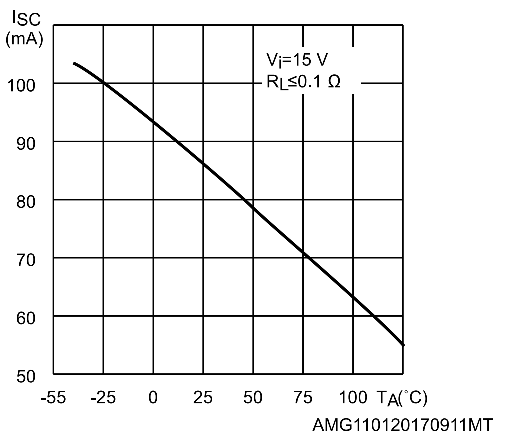


Figure 13: Output saturation voltage vs load current

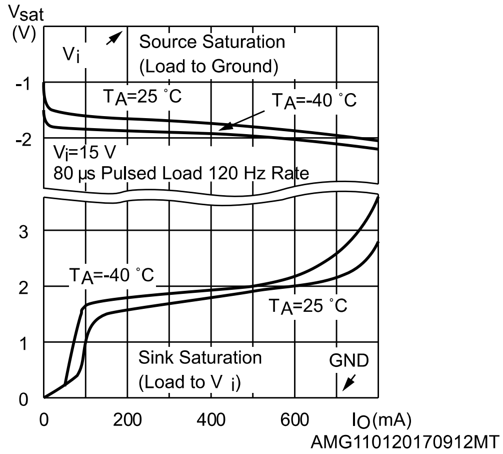


Figure 14: Supply current vs supply voltage

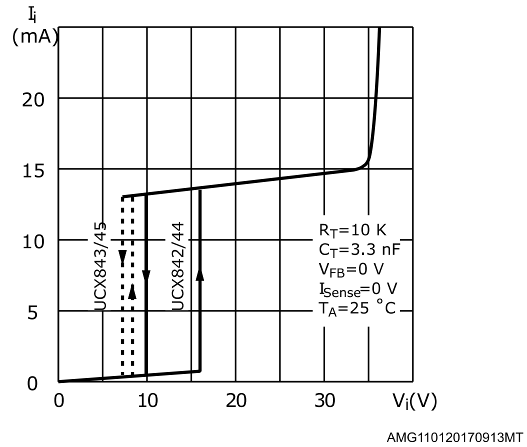


Figure 15: Output waveform

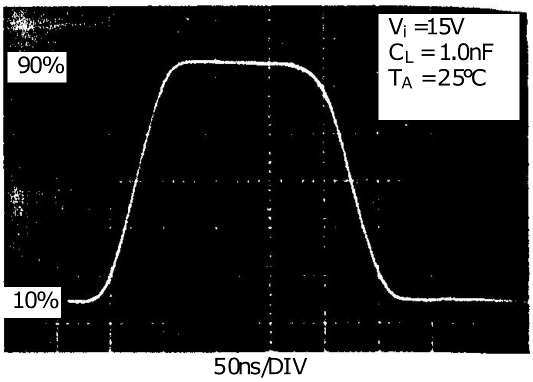


Figure 16: Output cross conduction

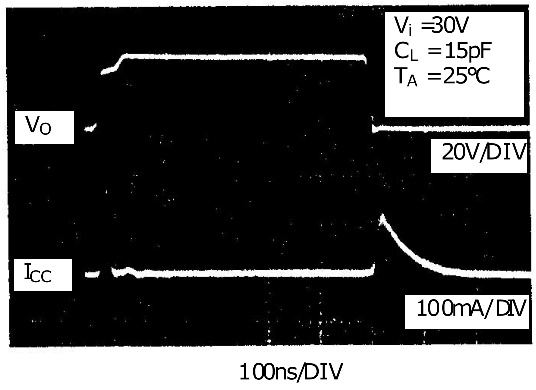


Figure 17: Oscillator and output waveforms

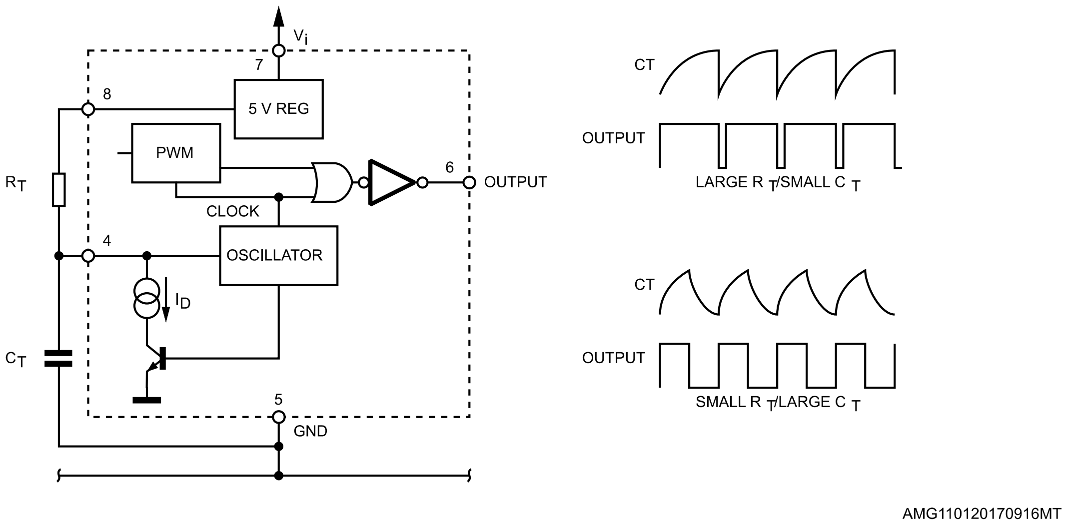


Figure 18: Error amp configuration

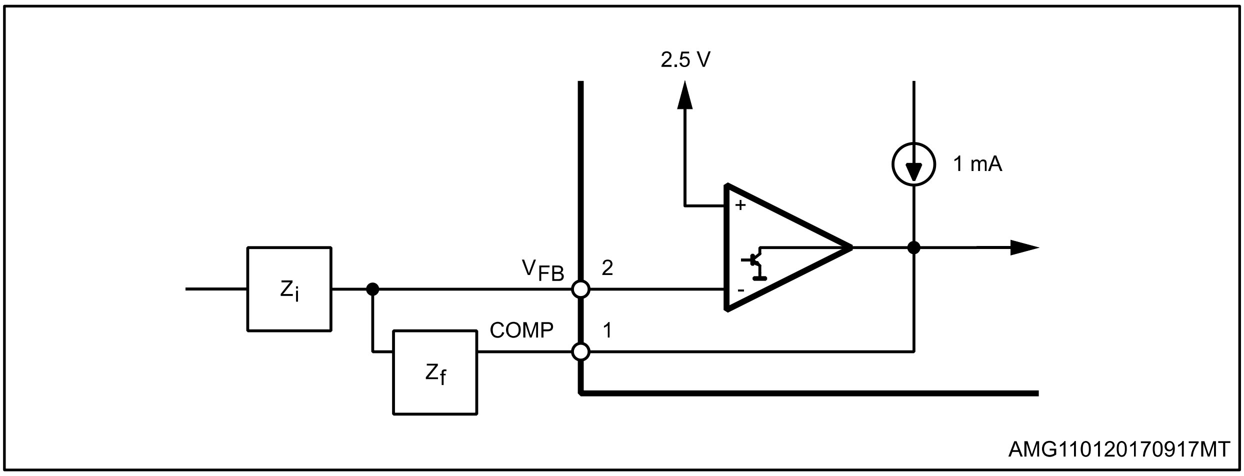


Figure 19: Under voltage lockout

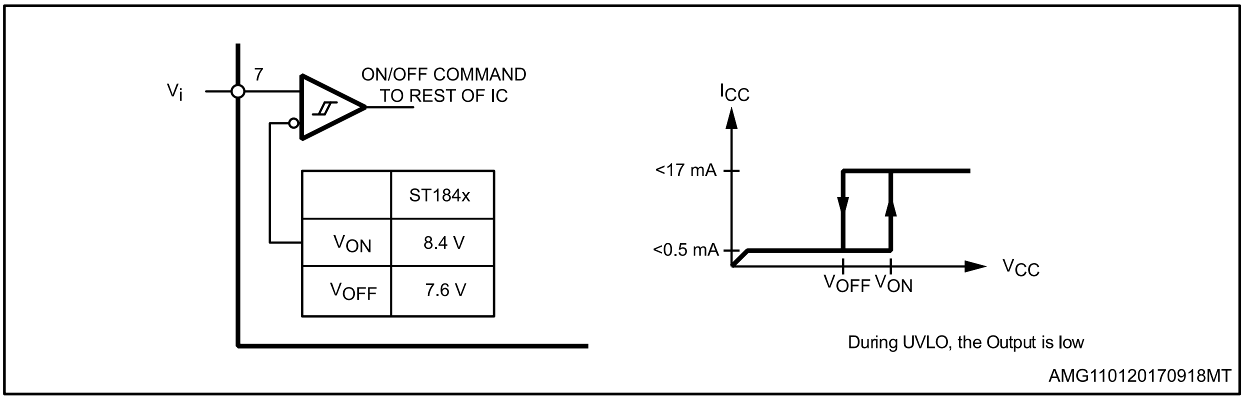
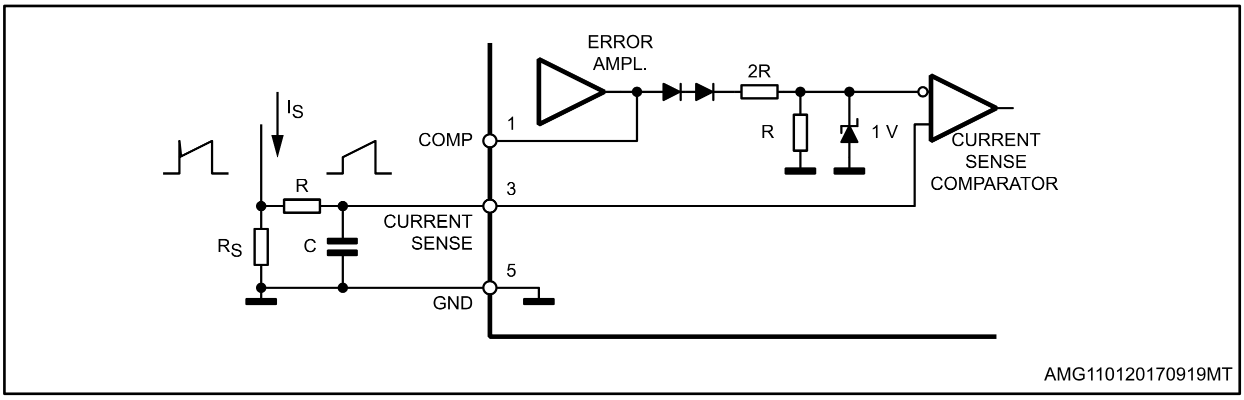


Figure 20: Current sense circuit



Peak current (is) is determined by the formula:

$$I_{Smax} \approx \frac{1.0V}{R_S}$$

A small RC filter may be required to suppress switch transients.

Figure 21: Slope compensation techniques

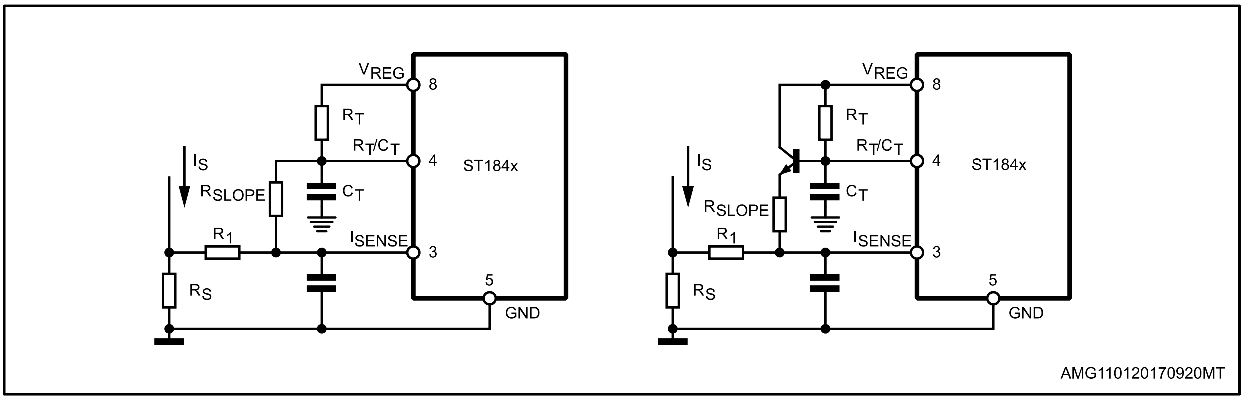


Figure 22: Isolated MOSFET drive and current transformer sensing

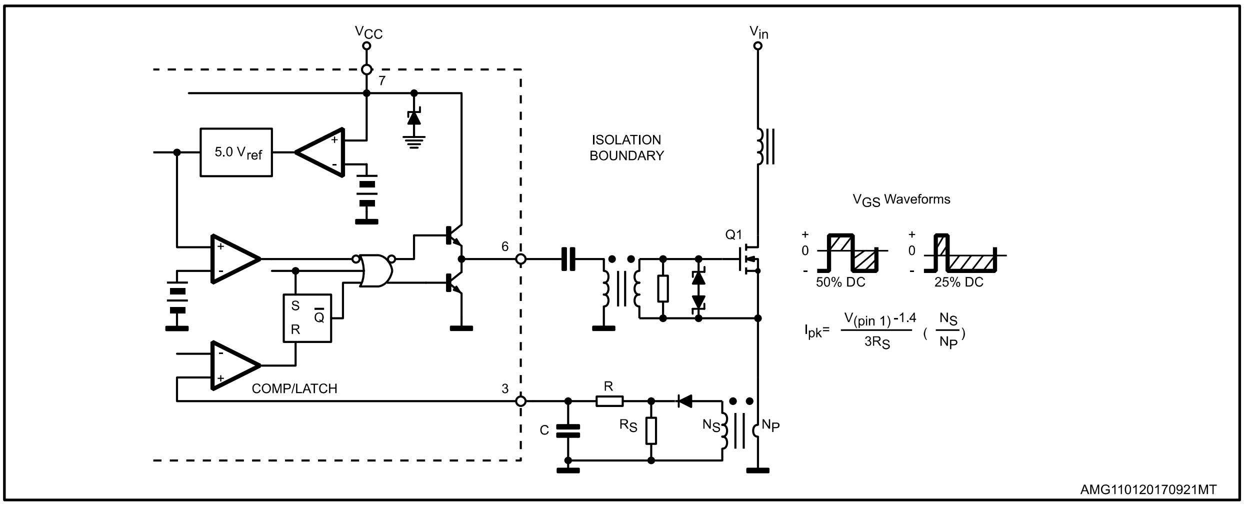


Figure 23: Latched shutdown

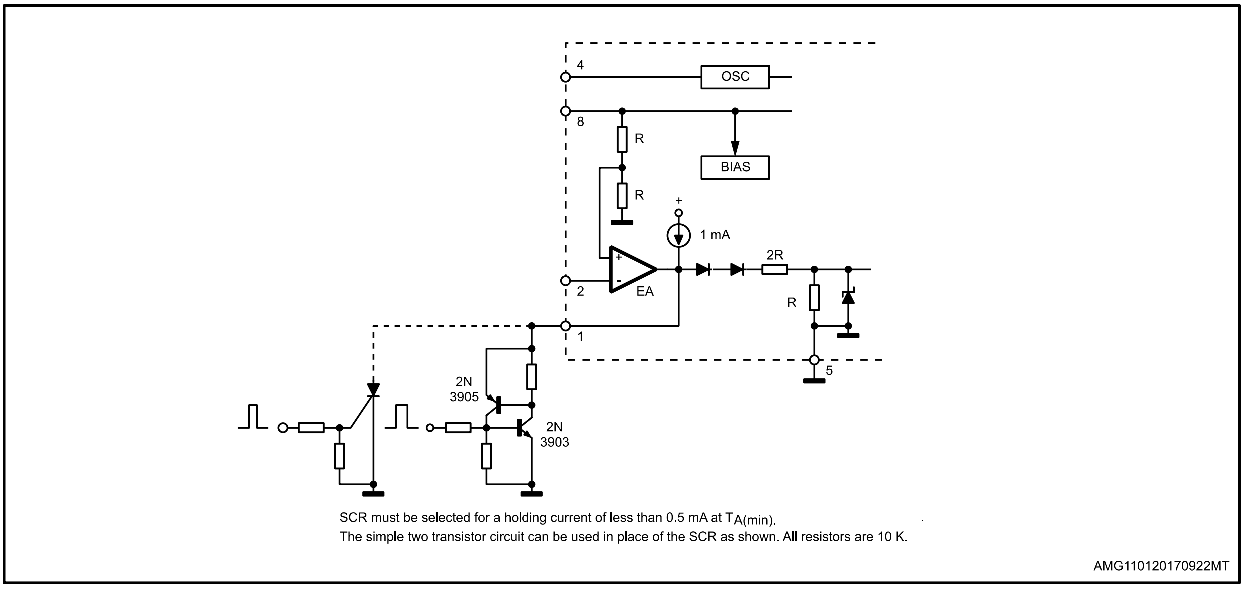


Figure 24: Error amplifier compensation

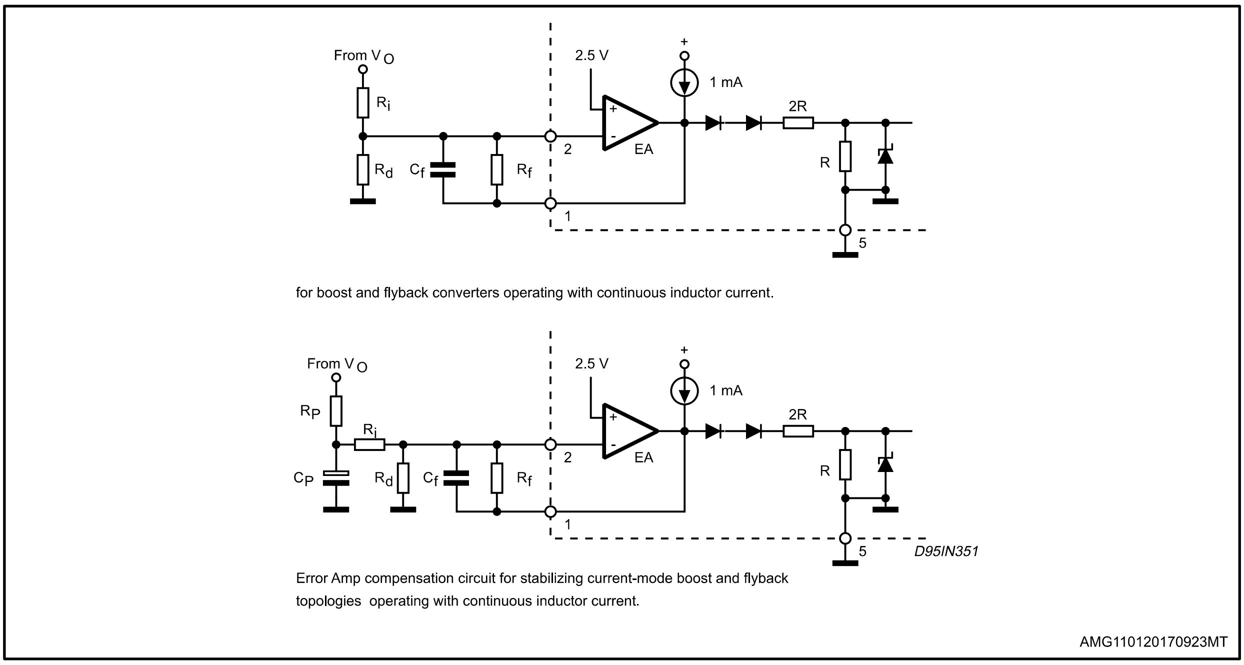


Figure 25: External clock synchronization

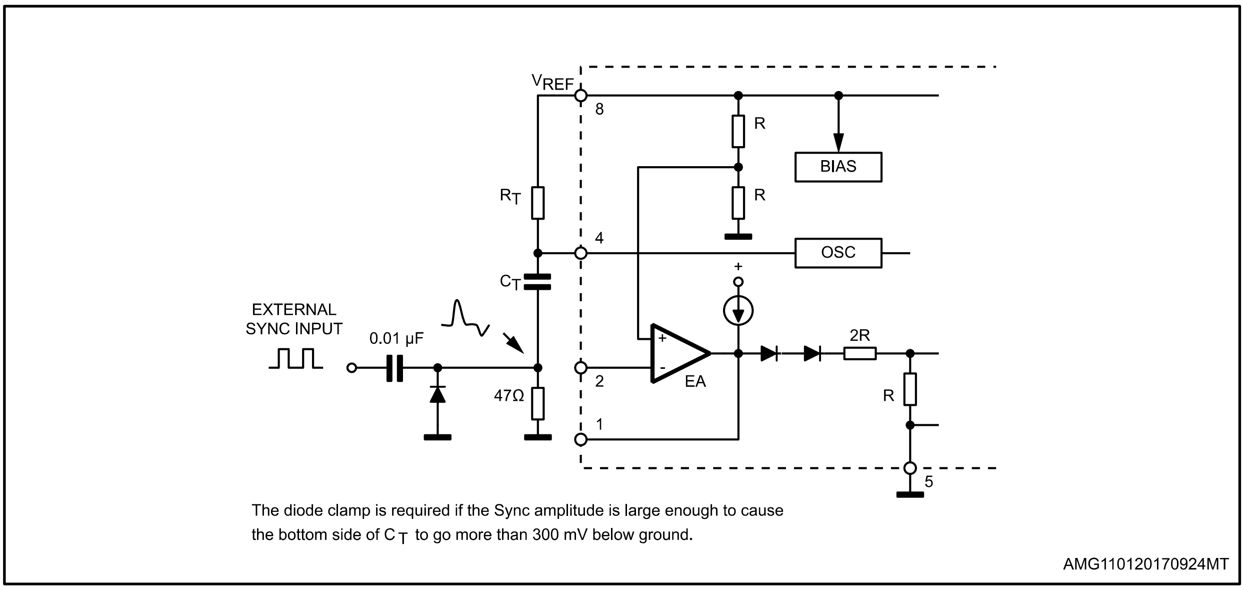


Figure 26: External duty cycle clamp and multi unit synchronization

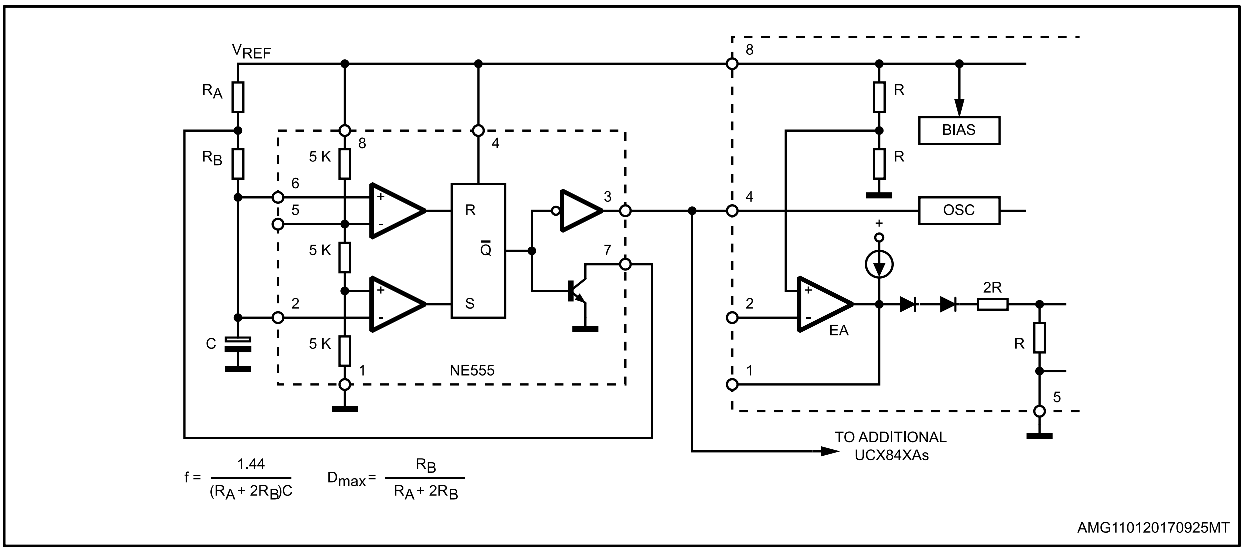


Figure 27: Soft-start circuit

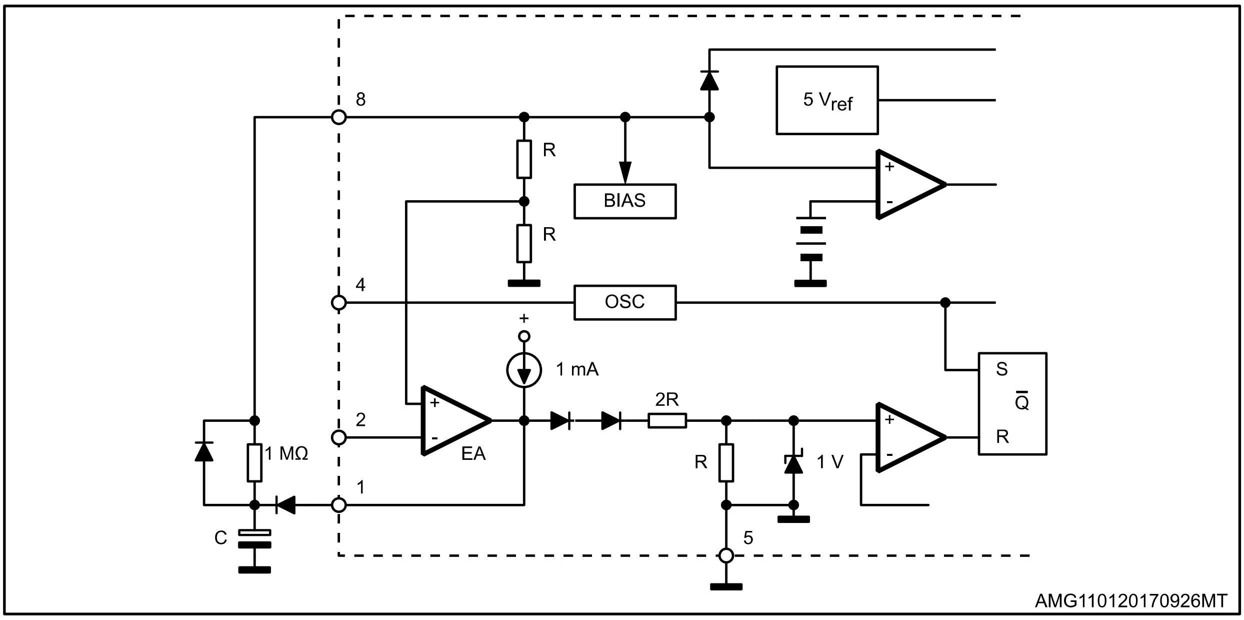
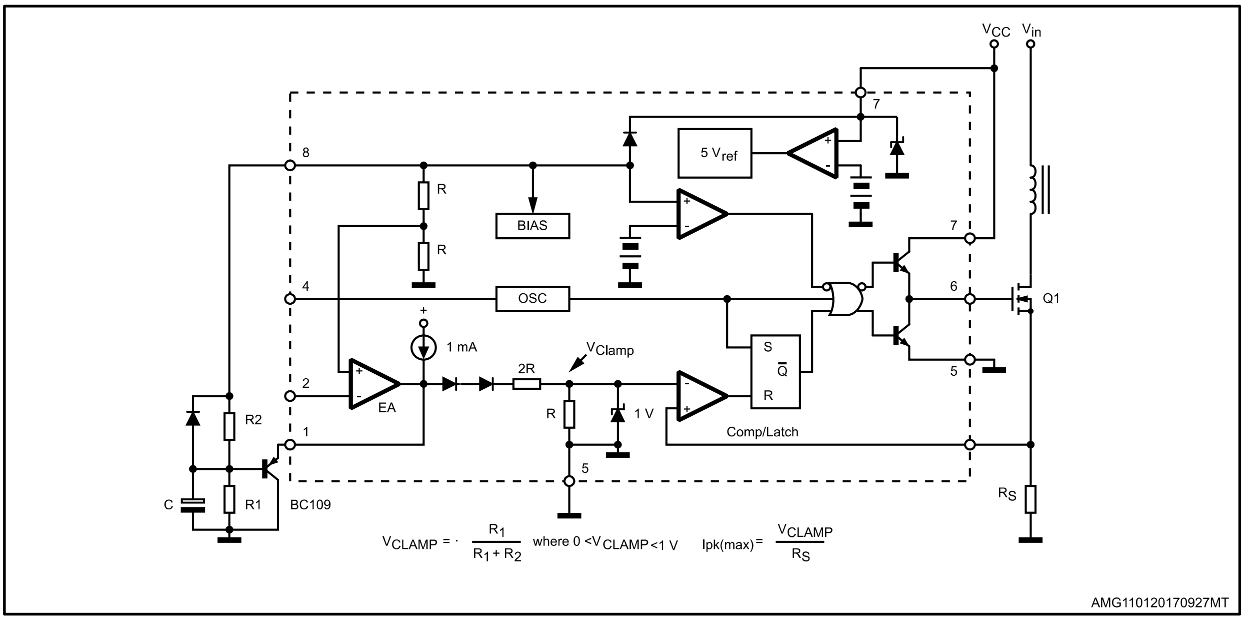


Figure 28: Soft-start and error amplifier output duty cycle clamp



8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

8.1 Flat-8 package information

Figure 29: Flat-8 package outline

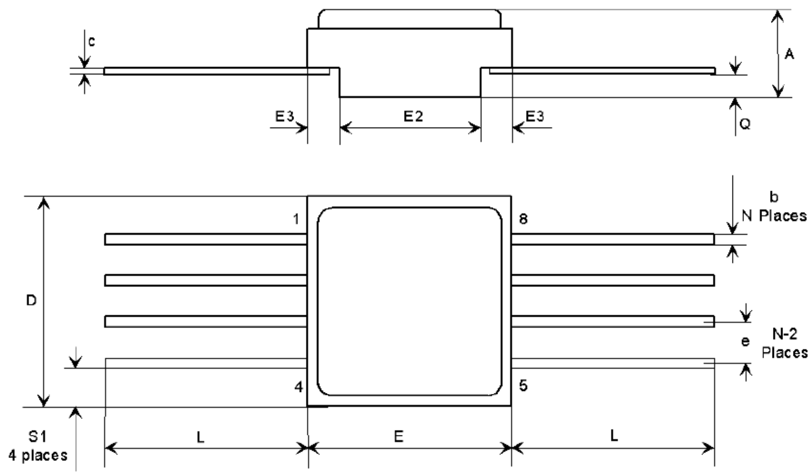


Table 9: Flat-8 mechanical data

Dim.	mm			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.24	2.44	2.64	0.088	0.096	0.104
b	0.38	0.43	0.48	0.015	0.017	0.019
c	0.10	0.13	0.16	0.004	0.005	0.006
D	6.35	6.48	6.61	0.250	0.255	0.260
E	6.35	6.48	6.61	0.250	0.255	0.260
E2	4.32	4.45	4.58	0.170	0.175	0.180
E3	0.88	1.01	1.14	0.035	0.040	0.045
e		1.27			0.050	
L	6.51	-	7.38	0.256	-	0.291
Q	0.66	0.79	0.92	0.026	0.031	0.036
S1	0.92	1.12	1.32	0.036	0.044	0.052
N	08			08		

9 Ordering information

Table 10: Order codes

Order code	Detailed specification	Quality level	EPPL	Package	Lead finish	Marking[(1)]	Packing
ST1843K1	-	Engineering Model	-	Flat-8	Gold	ST1843K1	Strip pack
ST1843FKG	9108/020/01F	ESCC	Target		Gold	9108/020/01F	
ST1843FKT	9108/020/02F				Solder dip	9108/020/02F	
ST1845K1	-	Engineering model	-		Gold	ST1845K1	
ST1845RKG	9108/021/01R	ESCC	Target		Gold	9108/021/01R	
ST1845RKT	9108/021/02R				Solder dip	9108/021/02R	

Notes:

[(1)]Specific marking only. Complete marking includes in addition the following: ST logo, ESCC logo, date code and country of origin.

Contact ST Sales office for information about specific conditions for products in die form, other quality levels and tape and reel packing.

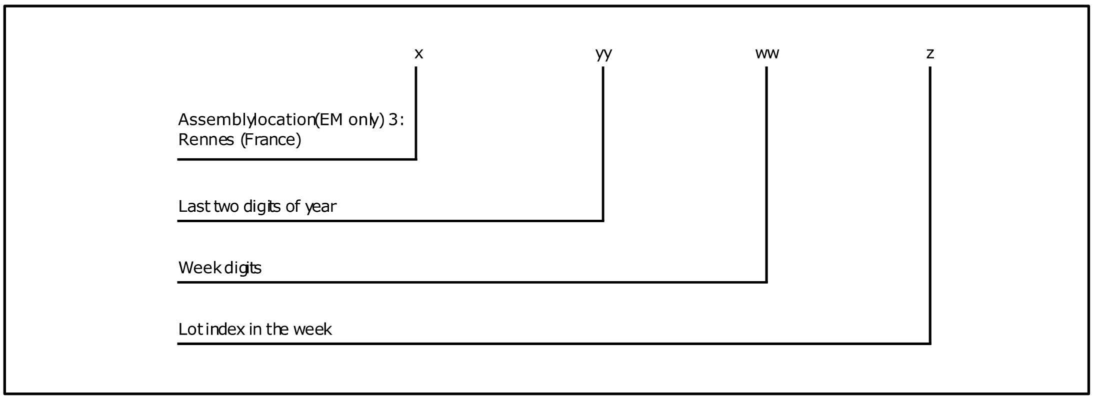
9.1 Other information

9.1.1 Date code

The date code is structured as shown in *Figure 30: "Date code composition"*:

- QML-

Figure 30: Date code composition



9.1.2 Documentation

Each shipment box includes in addition to the parts, an envelop with the documentation summarized in *Table 11: "Documentation per quality level"*:

Table 11: Documentation per quality level

Quality level	Documentation[(1)]
Engineering model	Certificate of Conformance over the Military Temperature Range (including data sheet reference, order summary, assembly lot ID, date code and specific marking)
ESCC flight	Certificate of Conformance to ESCC9000 (including ESCC specification reference, ESCC qualification Maintenance Test Lot reference, order summary, diffusion lot ID, assembly lot ID, date code and specific marking)
	Radiation verification test report

Notes:

[(1)]Default documentation only. Contact STMicroelectronics sales office for optional documentation.

10 Revision history

Table 12: Document revision history

Date	Revision	Changes
12-Sep-2011	1	First revision
21-Mar-2017	2	Updated the features, the description and Table 1: "Device summary" in cover page. Updated Table 2: "Absolute maximum ratings", Figure 2: "Pin connection", Table 5: "Electrical characteristics ", Figure 3: "Unbias conditions", Table 7: "Electrical parameter during irradiation testing", Section 6.1.3: "Heavy Ions" and Table 10: "Order codes". Added Section 9.1: "Other information". Minor text changes.
04-Aug-2017	3	Updated *Table 5: "Electrical characteristics "*, *Figure 3: "Unbias conditions"*, *Figure 19: "Under voltage lockout"* and *Figure 21: "Slope compensation techniques"*. Minor text changes.

IMPORTANT NOTICE – PLEASE READ CAREFULLY