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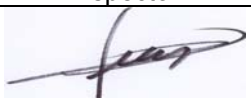
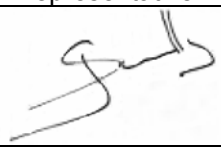
INTEGRATED CIRCUIT,
SILICON MONOLITHIC CMOS GATE ARRAY
INTEGRATED MOTOR CONTROLLER FOR MECHANISMS

BASED ON TYPE MH1RT

ASIC Sheet N°. FPK
ESCC Detail Specification No. 9202/076

Issue / Rev.	Date	Approval		
		ATMEL chief inspector	ATMEL technical representative	Customer representative
0	14/12/06			

DOCUMENTATION CHANGE NOTICE

Rev. Letter	Rev. Date	CHANGE Reference	Item	Approved DCR No.

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1.

GENERAL

1.1. SCOPE

This specification defines the requirements for monolithic silicon, semi-custom CMOS gate array, referred to as 920207619-FPK.
The procurement requirements are defined in the purchase order through the ESCC component number defined in the MH1RT ESCC Detail Specification 9202/076.
It supplements the requirements of, and shall be read in conjunction with, the MH1RT ESCC Detail Specification 9202/076 and the ESCC Generic Specification listed under Applicable Documents

1.2. APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:

(a) ESCC Generic Specification No. 9000
(b) MH1RT ESCC Detail Specification 9202/076
(c) MIL-STD-883 Test Methods and Procedures for Microcircuits
(d) 00/BEM-BDV/IMC/TNS/0015 issue 5 revision2, GSTP2 integrated motor controlled for mechanisms – HBRISC2 design specification and architectural design
(e) APF-FR-DR-HFPK-HBRISC2 revision 1.2, HBRISC2 design review document.

In the event of a conflict between the text of this ASIC Sheet and the references cited herein, the text of this sheet shall take precedence.

1.3. DEVICE TYPE

This gate array was designed on type MH1RT 1558K gates and packaged in a MQFP-F256 which is referred to in the ESCC component number as variant **19** of the MH1RT ESCC Detail Specification 9202/076.

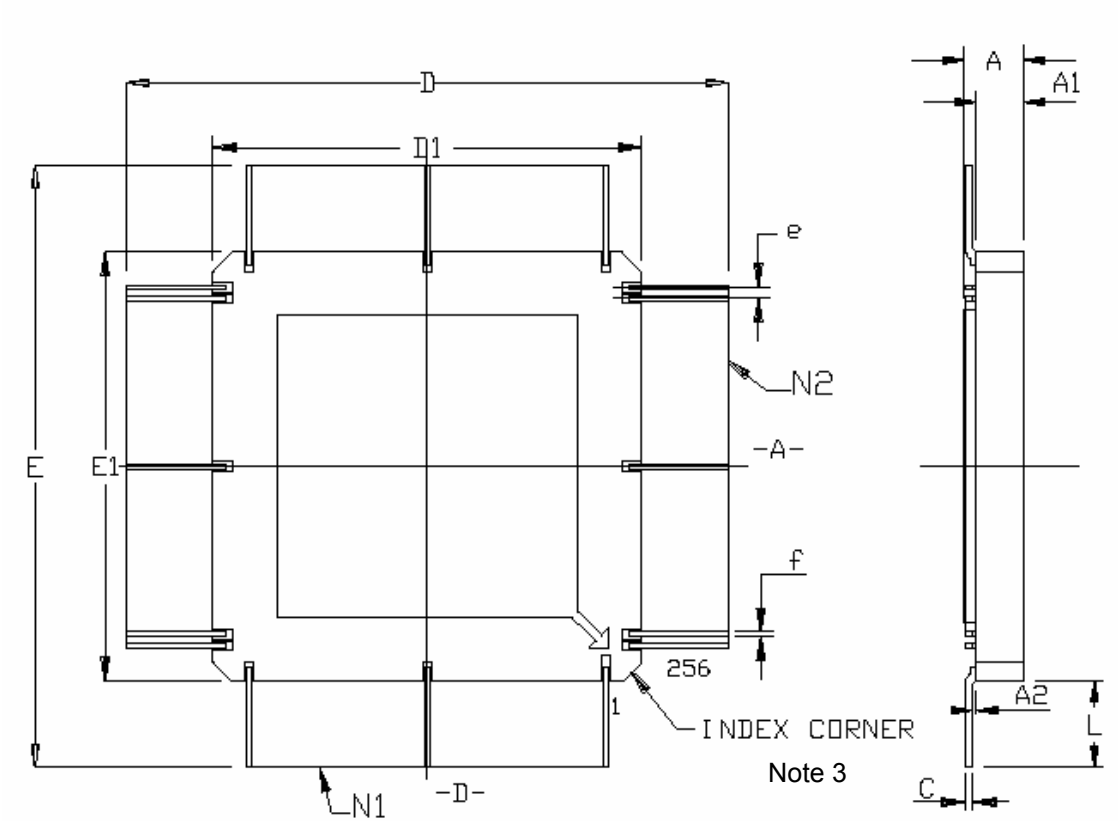
1.4. MAXIMUM RATINGS

The absolute maximum ratings shall not be exceeded at any time during use or storage.
This table shall be read in conjunction with the maximum ratings given in the MH1RT ESCC Detail Specification 9202/076 (supply current IDDOP, operating temperature range TOP, Storage temperature range TSTG and soldering temperature TSOL).

Characteristics	Symbol	Maximum Ratings	Unit	Remarks
Supply Voltage	V_{DD} V_{CC}	-0.5 to 4 -0.5 to 6	V V	Note 1
Input Voltage	V_{IN}	-0.5 to V_{DD} + 0.5 -0.5 To V_{CC} + 0.5	V	Notes 1, 2
Thermal Resistance	$R_{th(j-c)}$	3	°C/W	Junction to case
Device Power Dissipation (Continuous)	P_D	5	W	

1- Device is functional for 3V<=VDD<=3.6V and 4.5V<=VCC<=5.5V with reference to VSS=0V
2- Applicable to all inputs, input current limited to IIC = +/- 10 mA

1.5. PHYSICAL DIMENSION AND TERMINAL IDENTIFICATION



Symbols	Dimensions mm		Notes
	Min	Max	
A	2.41	3.18	
A1	2.06	2.56	
A2	0.05	0.36	
C	0.1	0.2	1
D/E	53.23	55.74	
D1/E1	36.83	37.34	
e	0.508 BSC		1
f	0.15	0.25	1
L	8.2	9.2	1
N1/N2	64		2

NOTES:
1. Applies to all leads
2. Number of leads each side
3. Terminal identification is specified by reference to the index corner as shown.

1.6. FUNCTIONAL DIAGRAM

Reference OO/BEM-BDV/IMC/TNS/0015 Issue 5 Revision 2 Para. 4.

1.7. PIN ASSIGNMENT

Pin	Pin Name	Function
1	Not connected	-
2	bxadd[0]	Output
3	bxadd[1]	Output
4	r_wb	Output
5	d_cbar	Output
6	spiboot_mstr	Input
7	VSSA	V_{SS}
8	VDDA	V_{CC}
9	main_ck	Input
10	progout[0]	Output
11	VSSB	V_{SS}
12	VCCB	V_{DD}
13	adcmuxsel[0]	Output
14	adcmuxsel[1]	Output
15	bxadd[2]	Output
16	bxadd[3]	Output
17	progout[1]	Output
18	progout[2]	Output
19	progout[3]	Output
20	int_bar	Input
21	VSSB	V_{SS}
22	VCCB	V_{DD}
23	serial_clk	Output
24	serial_data	Output
25	adcmuxsel[2]	Output
26	bxadd[4]	Output
27	siop_csbar[0]	Output
28	siop_csbar[1]	Output
29	siop_oebar[0]	Output
30	adcmuxsel[3]	Output
31	siop_oebar[1]	Output
32	VSSB	V_{SS}
33	VCCB	V_{DD}
34	bxadd[5]	Output
35	bxadd[6]	Output
36	siop_oebar[2]	Output
37	siop_csbar[2]	Output
38	siop_csbar[3]	Output
39	siop_oebar[3]	Output
40	VSSB	V_{SS}
41	VCCB	V_{DD}
42	VDD3V1	V_{DD}
43	bxadd[7]	Output
44	bxadd[8]	Output
45	adciobus[0]	Input/Output
46	siop_webar[0]	Output
47	VSSB	V_{SS}
48	VCCB	V_{DD}
49	sel_boot	Input
50	bxadd[9]	Output
51	adciobus[1]	Input/Output

52	siop_webar[1]	Output
53	siop_webar[2]	Output
54	adciobus[2]	Input/Output
55	VSSB	V_{SS}
56	VCCB	V_{DD}
57	VSSA	V_{SS}
58	VDDA	V_{CC}
59	bxadd[10]	Output
60	bxadd[11]	Output
61	adciobus[3]	Input/Output
62	EOCbar[0]	Input
63	VSSB	V_{SS}
64	VCCB	V_{DD}
65	Not connected	N/A
66	adciobus[4]	Input/Output
67	adciobus[5]	Input/Output
68	bxadd[12]	Output
69	EOCbar[1]	Input
70	Not connected	N/A
71	VSSA	V_{SS}
72	VDDA	V_{CC}
73	adciobus[6]	Input/Output
74	VDD3V7	V_{DD}
75	VSSB	V_{SS}
76	VCCB	V_{DD}
77	adciobus[7]	Input/Output
78	adciobus[8]	Input/Output
79	adciobus[9]	Input/Output
80	adciobus[10]	Input/Output
81	adciobus[11]	Input/Output
82	EOCbar[2]	Input
83	VSSB	V_{SS}
84	VCCB	V_{DD}
85	adciobus[12]	Input/Output
86	adciobus[13]	Input/Output
87	adciobus[14]	Input/Output
88	Not connected	-
89	Not connected	-
90	EOCbar[3]	Input
91	tdi	Input
92	tdo	Output (or high impedance)
93	tck	Input
94	tms	Input
95	trst	Input
96	siop_webar[3]	Output
97	VSSB	V_{SS}
98	VCCB	V_{DD}
99	siop_add[0]	Output
100	siop_add[1]	Output
101	bxadd[13]	Output
102	siop_add[2]	Output
103	siop_add[3]	Output
104	siop_add[4]	Output
105	siop_add[5]	Output
106	siop_add[6]	Output
107	siop_add[7]	Output

108	siop_add[8]	Output
109	siop_add[9]	Output
110	VSSB	V_{SS}
111	VCCB	V_{DD}
112	siop_add[10]	Output
113	siop_add[11]	Output
114	siop_add[12]	Output
115	siop_add[13]	Output
116	siop_add[14]	Output
117	siop_add[15]	Output
118	VDD3V6	V_{DD}
119	R_C	Output
120	soft_tic	Output
121	VSSA	V_{SS}
122	VDDA	V_{CC}
123	soft_tic_del	Output
124	synchr_tic	Input
125	test	Input
126	spi_out	Output (or high impedance)
127	VSSB	V_{SS}
128	VCCB	V_{DD}
129	Not connected	-
130	test_se	Input
131	bxadd[14]	Output
132	SOC	Output
133	CS[0]	Output
134	CS[1]	Output
135	VSSA	V_{SS}
136	VDDA	V_{CC}
137	CS[2]	Output
138	CS[3]	Output
139	spi_clk	Input
140	spi_in	Input
141	spi_csbar	Input
142	test_clk	Input
143	VSSB	V_{SS}
144	VCCB	V_{DD}
145	motor_pwm[0]	Output
146	motor_pwm[1]	Output
147	motor_pwm[2]	Output
148	motor_pwm[3]	Output
149	motor_pwm[4]	Output
150	motor_pwm[5]	Output
151	odd_ck	Output
152	crc_check	Output
153	iackbar	Output
154	upload_ip	Output
155	upload_err	Output
156	motor_pwm[6]	Output
157	motor_pwm[7]	Output
158	motor_pwm[8]	Output
159	VSSB	V_{SS}
160	VCCB	V_{DD}
161	VDD3V5	V_{DD}
162	motor_pwm[9]	Output
163	motor_pwm[10]	Output

164	motor_pwm[11]	Output
165	adciobus[15]	Input/Output
166	bxadd[15]	Output
167	motor_pwm[12]	Output
168	motor_pwm[13]	Output
169	VSSB	V_{SS}
170	VCCB	V_{DD}
171	motor_pwm[14]	Output
172	motor_pwm[15]	Output
173	motor_pwm[16]	Output
174	motor_pwm[17]	Output
175	seu_corr_e	Output
176	seu_corr_i	Output
177	seu_error	Output
178	se_pwm[0]	Output
179	se_pwm[1]	Output
180	se_pwm[2]	Output
181	se_pwm[3]	Output
182	se_pwm[4]	Output
183	VSSB	V_{SS}
184	VCCB	V_{DD}
185	VSSA	V_{SS}
186	VDDA	V_{CC}
187	se_pwm[5]	Output
188	siop_add[16]	Output
189	siop_add[17]	Output
190	bxio[38]	Input/Output
191	bxio[37]	Input/Output
192	bxio[36]	Input/Output
193	Not connected	-
194	bxio[35]	Input/Output
195	VSSB	V_{SS}
196	VCCB	V_{DD}
197	bxio[34]	Input/Output
198	VDD3V4	V_{DD}
199	VSSA	V_{SS}
200	VDDA	V_{CC}
201	bxio[33]	Input/Output
202	bxio[32]	Input/Output
203	bxio[31]	Input/Output
204	bxio[30]	Input/Output
205	VSSB	V_{SS}
206	VCCB	V_{DD}
207	bxio[29]	Input/Output
208	bxio[28]	Input/Output
209	bxio[27]	Input/Output
210	bxio[26]	Input/Output
211	bxio[25]	Input/Output
212	VSSB	V_{SS}
213	VCCB	V_{DD}
214	bxio[24]	Input/Output
215	bxio[23]	Input/Output
216	bxio[22]	Input/Output
217	bxio[21]	Input/Output
218	bxio[20]	Input/Output
219	VSSB	V_{SS}

220	VCCB	V_{DD}
221	bxio[19]	Input/Output
222	bxio[18]	Input/Output
223	bxio[17]	Input/Output
224	bxio[16]	Input/Output
225	bxio[15]	Input/Output
226	VSSB	V_{SS}
227	VCCB	V_{DD}
228	bxio[14]	Input/Output
229	bxio[13]	Input/Output
230	bxio[12]	Input/Output
231	bxio[11]	Input/Output
232	VDD3V3	V_{DD}
233	ds	Output
234	bxio[10]	Input/Output
235	VSSB	V_{SS}
236	VCCB	V_{DD}
237	bxio[9]	Input/Output
238	bxio[8]	Input/Output
239	bxio[7]	Input/Output
240	bxio[6]	Input/Output
241	bxio[5]	Input/Output
242	as	Output
243	VSSB	V_{SS}
244	VCCB	V_{DD}
245	Not connected	-
246	bxio[4]	Input/Output
247	bxio[3]	Input/Output
248	bxio[2]	Input/Output
249	VSSA	V_{SS}
250	VDDA	V_{CC}
251	bxio[1]	Input/Output
252	bxio[0]	Input/Output
253	reset_bar	Input
254	VDD3V2	V_{DD}
255	VSSB8	V_{SS}
256	VCCB8	V_{DD}

1.8. INSTRUCTION SET AND TIMING DIAGRAMS

Reference OO/BEM-BDV/IMC/TNS/0015 Issue 5 Revision 2 Para. 5.2, 5.3, 5.4, 5.5.

1.9. FAULT COVERAGE MEASUREMENT OF MANUFACTURING LOGIC TESTS

The fault coverage is 97.25%

2. REQUIREMENTS

2.1. GENERAL

The complete requirements for procurement of the components specified herein are as stated in the MH1RT ESCC Detail Specification 9202/076 and the ESCC Generic Specification.

2.2. MARKING

The marking of the flight models shall be as defined in the MH1RT ESCC Detail Specification 9202/076 and as follows:
920207619-FPK
FPK
HBRISC2 ESCC
Tracability information

2.3. ELECTRICAL MEASUREMENTS AT ROOM, HIGH AND LOW TEMPERATURES

Electrical measurements shall be performed at room, high and low temperatures.
Consolidated notes are given after the tables.

2.3.1. Room temperature electrical measurements

The measurements shall be performed at T = + 22 +/- 3°C.
This table shall be read in conjunction with the room temperature electrical measurements given in the MH1RT ESCC Detail Specification 9202/076.

Characteristics	Symbol	Test Method Mil-Std-883	Test Conditions Note 1	Limits		Unit
				Min	Max	
Functional Test 1	-	3014	Sim 1 to Sim20 V_{DD} = 3.0V V_{CC}=4.5V V_{IH} = 3V, V_{IL} = 0V Note 2	-	-	
Functional Test 2	-	3014	Sim 1 to Sim20 V_{DD} = 3.3V V_{CC}=5V V_{IH} = 3.3V, V_{IL} = 0V Note 2	-	-	
Functional Test 3	-	3014	Sim 1 to Sim20 V_{DD} = 3.6V V_{CC}=5.5V V_{IH} = 3.6V, V_{IL} = 0V Note 2	-	-	
Supply Current Stand-by	IDDSB	3005	Sim2, Static mode Outputs open V_{DD} = 3.6V V_{CC}=0V		2.2	mA
Supply Current Operating	IDDOP	3005	Sim 2 V_{DD} = 3.6V V_{CC}=5.5V		180	mA
Propagation delay Main_ck to ds low	TFDS	3003	Sim1 (note 2) V_{DD} = 3.0V V_{CC} = 4.5V		44	ns
Propagation delay Main_ck to ds high	TRDS	3003	Sim1 (note 2) V_{DD} = 3.0V V_{CC} = 4.5V		26	ns
Propagation delay Main_ck to bxadd	TADDV	3003	Sim2 (note 2) V_{DD} = 3.0V V_{CC} = 4.5V		21	ns

Propagation delay Main_ck to r_wb low	TFRW	3003	Sim2 (note 2) V_{DD} = 3.0V V_{CC} = 4.5V		45	ns
Propagation delay Main_ck to r_wb high	TRRW	3003	Sim2 (note 2) V_{DD} = 3.0V V_{CC} = 4.5V		26	ns
Propagation delay Main_ck to soft_tic low	TFSO	3003	Sim8 (note 2) V_{DD} = 3.0V V_{CC} = 4.5V		29	ns
Propagation delay Main_ck to soft_tichigh	TRSO	3003	Sim8 (note 2) V_{DD} = 3.0V V_{CC} = 4.5V		24	ns
Propagation delay main_ck to siop_add	TADDIOV	3003	Sim15 (note 2) V_{DD} = 3.0V V_{CC} = 4.5V		45	ns
Propagation delay spi_clk to spi_outhigh	TSDOACC1	3003	Sim10 (note 2) V_{DD} = 3.0V V_{CC} = 4.5V		20	ns
Propagation delay spi_clk to spi_outlow	TSDOACC2	3003	Sim10 (note 2) V_{DD} = 3.0V V_{CC} = 4.5V		26	ns
Propagation delay Main_ck to serial_clk	TSCLKACC	3003	Sim8 (note 2) V_{DD} = 3.0V V_{CC} = 4.5V		24	ns
Propagation delay Main_ck to serial_data	TSDACC	3003	Sim8 (note 2) V_{DD} = 3.0V V_{CC} = 4.5V		24	ns

Note 1: Unless otherwise specified, all inputs and outputs shall be tested for each characteristic. Inputs not under test shall be V_{IN}=V_{SS}, V_{CC} or V_{DD} and outputs not under test shall be open. V_{SS}=0V.

Note 2: Functional tests and timing characteristics shall be tested in according with the simulation file number (sim#) as specified in reference APF-FR-DR-HFPK-HBRISC2 revision 1.2. Test conditions: V_{OH} >V_{CC}/2, V_{OL}<V_{CC}/2, Input signals dynamic characteristics: tr, tf < 10ns.

2.3.2.High and low temperatures electrical measurements

The measurements shall be performed at T = + 125 (+0 – 5)°C and T = -55 (+5 – 0)°C.
The characteristics, test methods, conditions and limits shall be the same as specified for room temperature electrical measurements.

2.4. PARAMETER DRIFT VALUES

Unless otherwise specified, the measurements shall be performed at T = 22 +/- 3 °C.
The test methods and test conditions shall be as per the corresponding test defined in room temperature electrical measurements.
The drift values shall not be exceeded for each characteristic specified. In addition the corresponding absolute limit values for each characteristic shall not be exceeded.
This table shall be read in conjunction with the parameter drift values given in the MH1RT ESCC Detail Specification 9202/076.

Characteristics	Symbols	Limits			Unit
		Drift value	Absolute		
		Δ	min	max	
Supply current, Stand-by	IDDSB	+/- 0.22	-	2.2	mA

2.5. INTERMEDIATE AND END-POINT ELECTRICAL MEASUREMENTS

Unless otherwise specified, the measurements shall be performed at T = 22 +/- 3 °C.
The test methods, test conditions and limits shall be as per the corresponding test defined in room temperature electrical measurements.

2.6. POWER BURN-IN CONDITIONS

Characteristics	Symbols	Test conditions (note 1)	Unit
Ambient temperature	T_{amb}	+125 (+0-5)	°C
Outputs (all outputs)	V_{OUT}	V_{DD}/2 (note 2)	V
Inputs (note1)	V_{IN}	V_{DD} (note 3)	V
Inputs (note1)	V_{IN}	$V_{GEN(Sn)}$ (notes 3, 4)	V
Pulse voltage	V_{GEN}	0 to V_{DD}	V
Pulse frequency Square Wave	$f_{GEN(S1)}$	1.65 ±10% 50% duty cycle tr=tf ≤10ns (note 4)	MHz
Positive supply voltages	V_{DD} V_{CC}	3.7 ± 0.2 5.75 ± 0.2	V
Negative supply voltage	V_{SS}	0	V

Notes:
1. Pins connected as follow

Pin	Pin Name	Function	Test Condition
1	Not connected	N/A	Open circuit
2	bxadd[0]	Output	V_{DD}/2 (note 2)
3	bxadd[1]	Output	V_{DD}/2 (note 2)
4	r_wb	Output	V_{DD}/2 (note 2)
5	d_cbar	Output	V_{DD}/2 (note 2)
6	spiboot_mstr	Input	$V_{GEN(S3)}$ (note 4)
7	VSSA	Negative supply	V_{SS}
8	VDDA	Positive supply	V_{CC}
9	main_ck	Input	$V_{GEN(S1)}$ (note 4)
10	progout[0]	Output	V_{DD}/2 (note 2)
11	VSSB	Negative supply	V_{SS}
12	VCCB	Positive supply	V_{CC}
13	adcmuxsel[0]	Output	V_{DD}/2 (note 2)
14	adcmuxsel[1]	Output	V_{DD}/2 (note 2)
15	bxadd[2]	Output	V_{DD}/2 (note 2)
16	bxadd[3]	Output	V_{DD}/2 (note 2)
17	progout[1]	Output	V_{DD}/2 (note 2)
18	progout[2]	Output	V_{DD}/2 (note 2)
19	progout[3]	Output	V_{DD}/2 (note 2)
20	int_bar	Input	$V_{GEN(S2)}$ (note 4)
21	VSSB	Negative supply	V_{SS}
22	VCCB	Positive supply	V_{DD}
23	serial_clk	Output	V_{DD}/2 (note 2)

24	serial_data	Output	V_{DD}/2 (note 2)
25	adcmuxsel[2]	Output	V_{DD}/2 (note 2)
26	bxadd[4]	Output	V_{DD}/2 (note 2)
27	siop_csbar[0]	Output	V_{DD}/2 (note 2)
28	siop_csbar[1]	Output	V_{DD}/2 (note 2)
29	siop_oebar[0]	Output	V_{DD}/2 (note 2)
30	adcmuxsel[3]	Output	V_{DD}/2 (note 2)
31	siop_oebar[1]	Output	V_{DD}/2 (note 2)
32	VSSB	Negative supply	V_{SS}
33	VCCB	Positive supply	V_{DD}
34	bxadd[5]	Output	V_{DD}/2 (note 2)
35	bxadd[6]	Output	V_{DD}/2 (note 2)
36	siop_oebar[2]	Output	V_{DD}/2 (note 2)
37	siop_csbar[2]	Output	V_{DD}/2 (note 2)
38	siop_csbar[3]	Output	V_{DD}/2 (note 2)
39	siop_oebar[3]	Output	V_{DD}/2 (note 2)
40	VSSB	Negative supply	V_{SS}
41	VCCB	Positive supply	V_{DD}
42	VDD3V1	Positive supply	V_{DD}
43	bxadd[7]	Output	V_{DD}/2 (note 2)
44	bxadd[8]	Output	V_{DD}/2 (note 2)
45	adciobus[0]	Input	$V_{GEN(S2)}$ (note 4)
46	siop_webar[0]	Output	V_{DD}/2 (note 2)
47	VSSB	Negative supply	V_{SS}
48	VCCB	Positive supply	V_{DD}
49	sel_boot	Input	$V_{GEN(S3)}$ (note 4)
50	bxadd[9]	Output	V_{DD}/2 (note 2)
51	adciobus[1]	Input	$V_{GEN(S2)}$ (note 4)
52	siop_webar[1]	Output	V_{DD}/2 (note 2)
53	siop_webar[2]	Output	V_{DD}/2 (note 2)
54	adciobus[2]	Input	$V_{GEN(S2)}$ (note 4)
55	VSSB	Negative supply	V_{SS}
56	VCCB	Positive supply	V_{DD}
57	VSSA	Negative supply	V_{SS}
58	VDDA	Positive supply	V_{CC}
59	bxadd[10]	Output	V_{DD}/2 (note 2)
60	bxadd[11]	Output	V_{DD}/2 (note 2)
61	adciobus[3]	Input	$V_{GEN(S7)}$ (note 4)
62	EOCbar[0]	Input	$V_{GEN(S4)}$ (note 4)
63	VSSB	Negative supply	V_{SS}
64	VCCB	Positive supply	V_{DD}
65	Not connected	N/A	Open circuit
66	adciobus[4]	Input	$V_{GEN(S7)}$ (note 4)
67	adciobus[5]	Input	$V_{GEN(S7)}$ (note 4)
68	bxadd[12]	Output	V_{DD}/2 (note 2)
69	EOCbar[1]	Input	$V_{GEN(S4)}$ (note 4)
70	Not connected	N/A	Open circuit
71	VSSA	Negative supply	V_{SS}
72	VDDA	Positive supply	V_{CC}
73	adciobus[6]	Input	$V_{GEN(S7)}$ (note 4)
74	VDD3V7	Positive supply	V_{DD}
75	VSSB	Negative supply	V_{SS}
76	VCCB	Positive supply	V_{DD}
77	adciobus[7]	Input	$V_{GEN(S7)}$ (note 4)
78	adciobus[8]	Input	$V_{GEN(S7)}$ (note 4)
79	adciobus[9]	Input	$V_{GEN(S7)}$ (note 4)

80	adciobus[10]	Input	$V_{GEN(S7)}$ (note 4)
81	adciobus[11]	Input	$V_{GEN(S7)}$ (note 4)
82	EOCbar[2]	Input	$V_{GEN(S4)}$ (note 4)
83	VSSB	Negative supply	V_{SS}
84	VCCB	Positive supply	V_{DD}
85	adciobus[12]	Input	$V_{GEN(S7)}$ (note 4)
86	adciobus[13]	Input	$V_{GEN(S7)}$ (note 4)
87	adciobus[14]	Input	$V_{GEN(S7)}$ (note 4)
88	Not connected	N/A	Open circuit
89	Not connected	N/A	Open circuit
90	EOCbar[3]	Input	$V_{GEN(S4)}$ (note 4)
91	tdi	Input	$V_{GEN(S6)}$ (note 4)
92	tdo	Output	$V_{DD}/2$ (note 2)
93	tck	Input	$V_{GEN(S3)}$ (note 4)
94	tms	Input	$V_{GEN(S4)}$ (note 4)
95	trst	Input	$V_{GEN(S4)}$ (note 4)
96	siop_webar[3]	Output	$V_{DD}/2$ (note 2)
97	VSSB	Negative supply	V_{SS}
98	VCCB	Positive supply	V_{DD}
99	siop_add[0]	Output	$V_{DD}/2$ (note 2)
100	siop_add[1]	Output	$V_{DD}/2$ (note 2)
101	bxadd[13]	Output	$V_{DD}/2$ (note 2)
102	siop_add[2]	Output	$V_{DD}/2$ (note 2)
103	siop_add[3]	Output	$V_{DD}/2$ (note 2)
104	siop_add[4]	Output	$V_{DD}/2$ (note 2)
105	siop_add[5]	Output	$V_{DD}/2$ (note 2)
106	siop_add[6]	Output	$V_{DD}/2$ (note 2)
107	siop_add[7]	Output	$V_{DD}/2$ (note 2)
108	siop_add[8]	Output	$V_{DD}/2$ (note 2)
109	siop_add[9]	Output	$V_{DD}/2$ (note 2)
110	VSSB	Negative supply	V_{SS}
111	VCCB	Positive supply	V_{DD}
112	siop_add[10]	Output	$V_{DD}/2$ (note 2)
113	siop_add[11]	Output	$V_{DD}/2$ (note 2)
114	siop_add[12]	Output	$V_{DD}/2$ (note 2)
115	siop_add[13]	Output	$V_{DD}/2$ (note 2)
116	siop_add[14]	Output	$V_{DD}/2$ (note 2)
117	siop_add[15]	Output	$V_{DD}/2$ (note 2)
118	VDD3V6	Positive supply	V_{DD}
119	R_C	Output	$V_{DD}/2$ (note 2)
120	soft_tic	Output	$V_{DD}/2$ (note 2)
121	VSSA	Negative supply	V_{SS}
122	VDDA	Positive supply	V_{CC}
123	soft_tic_del	Output	$V_{DD}/2$ (note 2)
124	synchr_tic	Input	$V_{GEN(S4)}$ (note 4)
125	test	Input	$V_{DD}/2$ (note 2)
126	spi_out	Output	V_{DD} (note 3)
127	VSSB	Negative supply	V_{SS}
128	VCCB	Positive supply	V_{DD}
129	Not connected	N/A	Open circuit
130	test_se	Input	$V_{GEN(S9)}$ (note 4)
131	bxadd[14]	Output	$V_{DD}/2$ (note 2)
132	SOC	Output	$V_{DD}/2$ (note 2)
133	CS[0]	Output	$V_{DD}/2$ (note 2)
134	CS[1]	Output	$V_{DD}/2$ (note 2)
135	VSSA	Negative supply	V_{SS}

136	VDDA	Positive supply	V_{CC}
137	CS[2]	Output	V_{DD}/2 (note 2)
138	CS[3]	Output	V_{DD}/2 (note 2)
139	spi_clk	Input	$V_{GEN(S2)}$ (note 4)
140	spi_in	Input	$V_{GEN(S3)}$ (note 4)
141	spi_csbar	Input	$V_{GEN(S3)}$ (note 4)
142	test_clk	Input	V_{DD} (note 3)
143	VSSB	Negative supply	V_{SS}
144	VCCB	Positive supply	V_{DD}
145	motor_pwm[0]	Output	V_{DD}/2 (note 2)
146	motor_pwm[1]	Output	V_{DD}/2 (note 2)
147	motor_pwm[2]	Output	V_{DD}/2 (note 2)
148	motor_pwm[3]	Output	V_{DD}/2 (note 2)
149	motor_pwm[4]	Output	V_{DD}/2 (note 2)
150	motor_pwm[5]	Output	V_{DD}/2 (note 2)
151	odd_ck	Output	V_{DD}/2 (note 2)
152	crc_check	Output	V_{DD}/2 (note 2)
153	iackbar	Output	V_{DD}/2 (note 2)
154	upload_ip	Output	V_{DD}/2 (note 2)
155	upload_err	Output	V_{DD}/2 (note 2)
156	motor_pwm[6]	Output	V_{DD}/2 (note 2)
157	motor_pwm[7]	Output	V_{DD}/2 (note 2)
158	motor_pwm[8]	Output	V_{DD}/2 (note 2)
159	VSSB	Negative supply	V_{SS}
160	VCCB	Positive supply	V_{DD}
161	VDD3V5	Positive supply	V_{DD}
162	motor_pwm[9]	Output	V_{DD}/2 (note 2)
163	motor_pwm[10]	Output	V_{DD}/2 (note 2)
164	motor_pwm[11]	Output	V_{DD}/2 (note 2)
165	adciobus[15]	Input	$V_{GEN(S7)}$ (note 4)
166	bxadd[15]	Output	V_{DD}/2 (note 2)
167	motor_pwm[12]	Output	V_{DD}/2 (note 2)
168	motor_pwm[13]	Output	V_{DD}/2 (note 2)
169	VSSB	Negative supply	V_{SS}
170	VCCB	Positive supply	V_{DD}
171	motor_pwm[14]	Output	V_{DD}/2 (note 2)
172	motor_pwm[15]	Output	V_{DD}/2 (note 2)
173	motor_pwm[16]	Output	V_{DD}/2 (note 2)
174	motor_pwm[17]	Output	V_{DD}/2 (note 2)
175	seu_corr_e	Output	V_{DD}/2 (note 2)
176	seu_corr_i	Output	V_{DD}/2 (note 2)
177	seu_error	Output	V_{DD}/2 (note 2)
178	se_pwm[0]	Output	V_{DD}/2 (note 2)
179	se_pwm[1]	Output	V_{DD}/2 (note 2)
180	se_pwm[2]	Output	V_{DD}/2 (note 2)
181	se_pwm[3]	Output	V_{DD}/2 (note 2)
182	se_pwm[4]	Output	V_{DD}/2 (note 2)
183	VSSB	Negative supply	V_{SS}
184	VCCB	Positive supply	V_{DD}
185	VSSA	Negative supply	V_{SS}
186	VDDA	Positive supply	V_{CC}
187	se_pwm[5]	Output	V_{DD}/2 (note 2)
188	siop_add[16]	Output	V_{DD}/2 (note 2)
189	siop_add[17]	Output	V_{DD}/2 (note 2)
190	bxio[38]	Input	$V_{GEN(S8)}$ (note 4)
191	bxio[37]	Input	$V_{GEN(S8)}$ (note 4)

192	bxio[36]	Input	$V_{GEN(S8)}$ (note 4)
193	Not connected	N/A	Open circuit
194	bxio[35]	Input	$V_{GEN(S8)}$ (note 4)
195	VSSB	Negative supply	V_{SS}
196	VCCB	Positive supply	V_{DD}
197	bxio[34]	Input	$V_{GEN(S8)}$ (note 4)
198	VDD3V4	Positive supply	V_{DD}
199	VSSA	Negative supply	V_{SS}
200	VDDA	Positive supply	V_{CC}
201	bxio[33]	Input	$V_{GEN(S8)}$ (note 4)
202	bxio[32]	Input	$V_{GEN(S8)}$ (note 4)
203	bxio[31]	Input	$V_{GEN(S7)}$ (note 4)
204	bxio[30]	Input	$V_{GEN(S7)}$ (note 4)
205	VSSB	Negative supply	V_{SS}
206	VCCB	Positive supply	V_{DD}
207	bxio[29]	Input	$V_{GEN(S7)}$ (note 4)
208	bxio[28]	Input	$V_{GEN(S7)}$ (note 4)
209	bxio[27]	Input	$V_{GEN(S7)}$ (note 4)
210	bxio[26]	Input	$V_{GEN(S7)}$ (note 4)
211	bxio[25]	Input	$V_{GEN(S7)}$ (note 4)
212	VSSB	Negative supply	V_{SS}
213	VCCB	Positive supply	V_{DD}
214	bxio[24]	Input	$V_{GEN(S7)}$ (note 4)
215	bxio[23]	Input	$V_{GEN(S7)}$ (note 4)
216	bxio[22]	Input	$V_{GEN(S7)}$ (note 4)
217	bxio[21]	Input	$V_{GEN(S7)}$ (note 4)
218	bxio[20]	Input	$V_{GEN(S7)}$ (note 4)
219	VSSB	Negative supply	V_{SS}
220	VCCB	Positive supply	V_{DD}
221	bxio[19]	Input	$V_{GEN(S6)}$ (note 4)
222	bxio[18]	Input	$V_{GEN(S6)}$ (note 4)
223	bxio[17]	Input	$V_{GEN(S6)}$ (note 4)
224	bxio[16]	Input	$V_{GEN(S6)}$ (note 4)
225	bxio[15]	Input	$V_{GEN(S6)}$ (note 4)
226	VSSB	Negative supply	V_{SS}
227	VCCB	Positive supply	V_{DD}
228	bxio[14]	Input	$V_{GEN(S6)}$ (note 4)
229	bxio[13]	Input	$V_{GEN(S6)}$ (note 4)
230	bxio[12]	Input	$V_{GEN(S5)}$ (note 4)
231	bxio[11]	Input	$V_{GEN(S5)}$ (note 4)
232	VDD3V3	Positive supply	V_{DD}
233	ds	Output	$V_{DD}/2$ (note 2)
234	bxio[10]	Input	$V_{GEN(S5)}$ (note 4)
235	VSSB	Negative supply	V_{SS}
236	VCCB	Positive supply	V_{DD}
237	bxio[9]	Input	$V_{GEN(S5)}$ (note 4)
238	bxio[8]	Input	$V_{GEN(S5)}$ (note 4)
239	bxio[7]	Input	$V_{GEN(S5)}$ (note 4)
240	bxio[6]	Input	$V_{GEN(S5)}$ (note 4)
241	bxio[5]	Input	$V_{GEN(S4)}$ (note 4)
242	as	Output	$V_{DD}/2$ (note 2)
243	VSSB	Negative supply	V_{SS}
244	VCCB	Positive supply	V_{DD}
245	Not connected	N/A	Open circuit
246	bxio[4]	Input	$V_{GEN(S4)}$ (note 4)
247	bxio[3]	Input	$V_{GEN(S4)}$ (note 4)

248	bxio[2]	Input	$V_{GEN(S4)}$ (note 4)
249	VSSA	Negative supply	V_{SS}
250	VDDA	Positive supply	V_{CC}
251	bxio[1]	Input	$V_{GEN(S4)}$ (note 4)
252	bxio[0]	Input	$V_{GEN(S4)}$ (note 4)
253	reset_bar	Input	$V_{GEN(S10)}$ (note 4)
254	VDD3V2	Positive supply	V_{DD}
255	VSSB8	Negative supply	V_{SS}
256	VCCB8	Positive supply	V_{DD}

2. Outputs loaded with 2 resistors R=5.6 kΩ ± 5% between V_{DD} and V_{SS}
3. Input load =2.2 kΩ
4. Pulse voltage, $V_{GEN(Sn)}$, applied to each input, S1 to S10 where $f_{GEN(Sn+1)} = f_{GEN(Sn)} /2$

2.7. OPERATING LIFE CONDITIONS

The conditions shall be as specified for power burn-in.

2.8. TOTAL DOSE IRRADIATION TESTING

Not applicable