




DOCUMENT CHANGE REQUEST

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|---|--------------------------------------|------|--------|-------------------------------|--|-------------------------------|--|
| DCR number | | 1525 | | Changes required for: General | | Originator: Stephan Hernandez | |
| Date: 2024/02/15 | | | | Date sent: 2022/09/30 | | Organisation: ESTEC | |
| Status: IMPLEMENTED | | | | | | | |
| Title: | REP007 European Preferred Parts List | | | | | | |
| Number: | REP007 | | Issue: | 43 | | | |
| Other documents affected: | | | | | | | |
| | | | | | | | |
| Page: | | | | | | | |
| - | | | | | | | |
| Paragraph: | | | | | | | |
| - | | | | | | | |
| Original wording: | | | | | | | |
| - | | | | | | | |
| Proposed wording: | | | | | | | |
| STM / France, EPPL part1 (ESCC QML) 65nm ASIC Platform, based on type C65Space | | | | | | | |
| NanoXplore / France, EPPL part1 (ESCC QPL) Integrated Circuits, Silicon, Monolithic, 35KLUT Radiation-Hardened FPGA (NG-Medium) | | | | | | | |
| Cobham Gaisler / Sweden, EPPL part1 (MIL QML) GR740, Quad Core LEON4 SPARC V8 Microprocessor Moved from EPPL part 2 to EPPL part 1 | | | | | | | |
| Teledyne e2V / France, EPPL part1 (MIL QML) EV12AQ600AMGHY , Quad 12bit 1.6 GSps ADC with embedded crosspoint switch, Digitizing up to 6.4 GSps | | | | | | | |
| Arquimea / Spain, EPPL part 2 AQLVD01, Quad Bus Low Voltage Differential Signals (LVDS) Driver AQLVR02, Quad Bus Low Voltage Differential Signals (LVDS) Receiver | | | | | | | |
| Justification: | | | | | | | |
| Publication EPPL August 2022 | | | | | | | |

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| Attachments: |
| N/A |
| Modifications: |
| N/A |
| Approval signature: |
|  |
| Date signed: |
| 2024-02-15 |