DOCUMENT CHANGE REQUEST

DCR number 1804	Changes required for: General	Originator: Khlifa Hadre
Date: 2026/05/18	Date sent: 2026/03/04	Organisation: ST Microelectronics
Status: IMPLEMENTED		

Title:	CMOS Presettable Divide-by-N Counter, based on type 4018B		
Number:	9204/021	Issue:	5

Other documents affected:

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Paragraph:

2.3.1 Room Temperature Electrical Measurements

Original wording:

The initial maximum input capacitance limit (CIN) of input pins 1, 2, 3, 7, 9, 10, 12, 14, and 15 is set at 7.5 pF.

Proposed wording:

Keep the initial maximum limit of 7.5 pF for input pins: 1, 2, 3, 7, 9, 10, 12, and 15. We propose a new limit 10.0 pF solely for input pin 14 (CLK Input).

Justification:

The value measured on input pin 14 (CLK Input) in 6-inch recent diffusion lots exceeds the initial maximum limit of 7.5 pF. The new maximum limit of 10.0 pF is a result of our shift from 5 inches to 6 inches with fresh diffusion lots.

Attachments:

N/A

Modifications:

N/A

Approval signature:

Date signed:

2026-05-18