DOCUMENT CHANGE REQUEST

DCR number 227	Changes required for: N/A	Originator: Carol Brooks
Date: 2005/12/20	Date sent: 2005/12/20	Organisation: ESA/ESTEC
Status: IMPLEMENTED		

Title:	Advanced CMOS Quad 2-Input NAND Gates, based on type 54ACT00		
Number:	9201/128	Issue:	2

Other documents affected:

9201/143-2

Page:

See below

Paragraph:

See below

Original wording:

Proposed wording:

Para 2.6.1 and 2.6.2, page 16/17, Notes 1 and 2 - the minimum resistor value is 200 ohms; in the tables, positive supply voltage is 5.5, not 6

Para 2.7, page 18, The test condition for Output is Open; the input(s) are at Vgen; the pulse frequency test condition for Tr=Tf is less than or equal to 8ns/v; positive supply voltage is 5.5 instead of 6; for Notes 1 and 2 - the minimum resistor value is 200 ohms.

Para 2.9.1 becomes:

Continuous bias shall be applied during irradiation testing as specified below.

The total dose level applied shall be as specified in the component type variant information herein or in the Purchase Order.

Para 2.9.1.1 and 2.9.1.2 are deleted. The table in 2.9.1.1 becomes part of 2.9.1 with the following modifications:

Add (Note 1) tot he column heading Test Conditions.

The Test Condition for inputs becomes Note 2.

Note 2 is "Vin such that Vout=0 with a maximum input at Vdd

Justification:

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This DCR reflects the changes recommended by STMicroelectonics to reflect the actual conditions used for their products.

Attachments:

N/A

Modifications:

N/A

Approval signature:

Date signed:

2005-12-20