DOCUMENT CHANGE REQUEST

DCR number 406	Changes required for: General	Originator: S Jeffery - ESCC
Date: 2008/05/19	Date sent: 2008/05/19	Organisation:
Status: IMPLEMENTED		

Title:	CMOS 8-Stage Shift and Store Bus Register with Synchronous Serial Outputs and 3-State Parallel		
Number:	9306/026	Issue:	2

Other documents affected:

Page:

Pg. 7 Para. 1.7.1; Pg. 8 Para. 1.7.2; Pg. 10 Para. 1.7.3; Pg. 11 Para. 1.7.4; Pg. 13 Para. 1.10

Paragraph:

Pg. 7 Para. 1.7.1; Pg. 8 Para. 1.7.2; Pg. 10 Para. 1.7.3; Pg. 11 Para. 1.7.4; Pg. 13 Para. 1.10

Original wording:

Proposed wording:

Flat Package Dimensions Symbol F and Small Outline Ceramic Package Dimensions Symbol F changed from 1.27 TYPICAL to 1.27 TP

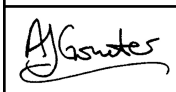
Dual-in-line Package Dimensions Symbol e changed from 2.54 TYPICAL to 2.54 TP

Chip Carrier Package Dimensions Symbols d, d1 and e, e1 changed from 1.27 TYPICAL to 1.27 TP

Title of Para. 1.10 changed from TRUTH TABLE AND TIMING DIAGRAM to TRUTH TABLE AND TIMING CHART

Justification:

This DCR covers all the required supplementary editorial and technical changes to ESCC 9306/026 Issue 2 which have not been defined in the approved, but not yet implemented, DCRs 371 and 255. The changes defined herein are required for the purposes of accuracy, clarification, and consistency with other ESCC Detail Specifications of the CMOS 4000B series and the 54HCxx series.

Attachments:
N/A
Modifications:
N/A
Approval signature:

Date signed:
2008-05-19