DOCUMENT CHANGE REQUEST

DCR number 415	Changes required for: N/A	Originator: Ron Fidler
Date: 2008/06/20	Date sent: 2008/06/20	Organisation: ESA/ESTEC
Status: IMPLEMENTED		

Title:	CMOS 32/40-Bit IEEE Floating Point Digital Signal Processor, based on Type TSC21020F		
Number:	9512/002	Issue:	2

Other documents affected:

Page:

Re-format as part of the ongoing conversion to the ESCC format and correction to errors.

Paragraph:

Re-format as part of the ongoing conversion to the ESCC format and correction to errors.

Original wording:

Proposed wording:

The format of this document complies with the current ESCC format for 9000 series detail specifications therefore no changes, except for minor amendments or typos, are made to the text. Better quality drawings have been inserted to make them clear and readable but these are technically unchanged. Some reformatting of tables has been performed to align this document with the other Atmel specifications but apart from correcting the errors listed below they are also technically unchanged.

NB: There is known support for active procurement against this specification from the manufacturer ATMEL.

1) Page 1, WITH THREE STATE OUTPUTS added to the title.

2) Para. 1.5, Maximum Ratings ± added to the IOUT rating.

3) Para. 1.7, Physical Dimensions better quality drawing used to enable dimensions to be clearly read.

4) Para. 1.8, Functional Diagram, a more meaningful and comprehensive drawing from the SMD/Atmel Data Sheet used in place of the original top-down drawing.

5) Para. 1.9, Pin Assignment and Description
The bar removed from above all DMD pins to comply with the SMD and the Atmel data Sheet.
The term TSC212020F replaced by processor in many places in the Pin Descriptions.
For the TRST bar the pin description comment changed from pulsed low to pulled low in accordance with the SMD.

6) Para. 1.10, Instruction Set and Timing Diagrams
The paragraph concerning Instruction Set removed as this is application information not usually included in a procurement

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specification.
Better quality timing diagrams inserted to enable the characteristics to be clearly read.

7) Para. 1.11, Input Protect Networks better quality drawings inserted.

8) Para. 2.3.1, Electrical Measurements at Room Temperature re-formatted per latest requirements. Other changes are:-
Test Method 3014 added to all Functional Tests and fCLK , VIH and VIL test conditions moved from the Notes to the body of the table
For both Supply Current tests IVDD Pins requirement move to the Notes
Input current symbols changed from IIL and IILT to IIL1 and IIL2
Test condition VIN=2.5V added to Input Capacitance per the SMD and Atmel Datasheet
TDWAK limits corrected from 15ns max to 15ns min per the SMD and Atmel Datasheet
Notes modified to clarify the pins to be tested
The Output Load drawing added to the Timing Characteristic note

9) Para. 2.4, Parameter Drift Values Input current symbols changed from IIL and IILT to IIL1 and IIL2

10) Para. 2.8.2, Total Dose Irradiation Testing as Item 9

Justification:

See above.

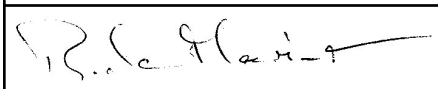
Attachments:

N/A

Modifications:

N/A

Approval signature:



Date signed:

2008-06-20