DOCUMENT CHANGE REQUEST

DCR number 143	Changes required for: N/A	Originator: P. GRIFFIN
Date: 2004/10/06	Date sent: 2004/10/06	Organisation: ESA/ESTEC
Status: IMPLEMENTED		

Title:	CMOS 14-Stage Ripple-Carry Binary Counter/Divider and Oscillator, based on type 4060B		
Number:	9204/052	Issue:	1

Other documents affected:

Page:

Figure 4(b) Page 32

Paragraph:

Figure 4(b) Page 32

Original wording:

Proposed wording:

See attached 9204052 draft issue 2 para 2.3.3 note 3

Justification:

Correction of error in 9204052 issue 1 Figure 4(b)-Quiescent Current Test Table. (Patterns 4 and 6 are incorrect)
A copy of the figure is attached with the errors highlighted.

Attachments:

9204052_DCR1.pdf, 9204052_DCR2.pdf, null

Modifications:

N/A

Approval signature:



Date signed:

2004-10-06

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Threshold Voltage N-Channel	V_{THN}	-	CLR Input at Ground All Other Inputs: V_{IN}=5V V_{DD}=5V, I_{SS}=-10µA T_{amb}=+125°C T_{amb}=- 55°C	 -0.3 -0.7	 -3.5 -3.5	V
Threshold Voltage P-Channel	V_{THP}	-	CLR Input at Ground All Other Inputs: V_{IN}=-5V V_{SS}=-5V, I_{DD}=10µA T_{amb}=+125°C T_{amb}=- 55°C	 0.3 0.7	 3.5 3.5	V

2.3.3 Notes to Electrical Measurement Tables

1. Unless otherwise specified all inputs and outputs shall be tested for each characteristic, inputs not under test shall be $V_{IN} = V_{SS}$ or V_{DD} and outputs not under test shall be open.
2. Functional tests shall be performed to verify Truth Table with $V_{OH} \geq V_{DD}$ -0.5V, $V_{OL} \leq$ 0.5V. The Maximum time to output comparator strobe = 300µs.
3. Quiescent Current shall be tested using the following input conditions:
   (a) Input CLR = V_{IH} ; Input CLK = V_{IL}.
   (b) Input CLR = CLK = V_{IL}.
   (c) Input CLR = V_{IL} ; 5461 pulses applied to CLK to configure outputs QE, QG, QI, QM to high level.
   (d) Input CLR = V_{IL} ; 5461 additional pulses applied to CLK to configure outputs QD, QF, QH, QJ, QL, QN to a high level.
   (e) Input CLR = V_{IL} ; 5461 additional pulses applied to CLK to configure all outputs QD to QN to a high level.
   (f) Input CLR = V_{IL} ; 1 additional pulse applied to CLK to configure all outputs QD to QN to a low level.
4. Interchange of forcing and measuring parameters is permitted.
5. Input Clamp Voltage 2 to V_{DD}, V_{IC2}, shall be tested on each input as follows:-

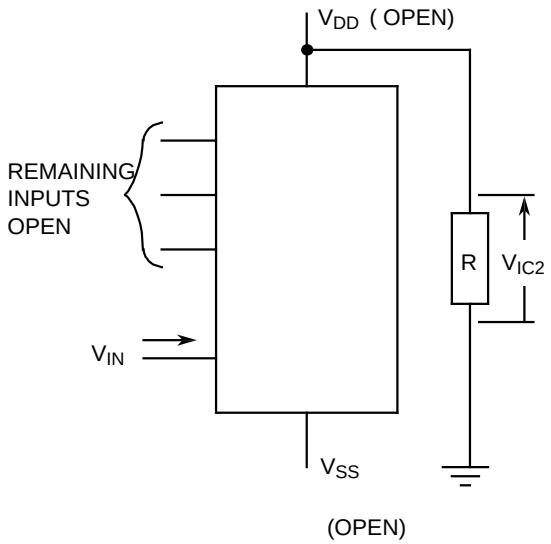

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS

FIGURE 4(a) - FUNCTIONAL TEST TABLE

PATTERN No.	PIN NUMBERS														D.C. SUPPLY	
	1	2	3	4	5	6	7	9	10	11 (NOTE 3)	12	13	14	15	8	16
1	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	V_{DD}
2	0	0	0	0	0	0	0	0	1	0	0	0	0	0		
3	0	0	0	0	0	0	0	1	0	1	0	0	0	0		
4	0	0	0	0	0	0	0			0	1	0	0	0		
5	0	0	0	0	0	0	0			0	0	0	0	0		
6	0	0	0	0	0	0	0			5461	0	0	0	0		
7	0	1	0	0	1	1	0			0	0	1	0	0		
8	0	1	0	0	1	1	0			5461	0	1	0	0		
9	1	0	1	1	0	0	1			0	0	0	1	1		
10	1	0	1	1	0	0	1			5461	0	0	1	1		
11	1	1	1	1	1	1	1			0	0	1	1	1		
12	0	0	0	0	0	0	0			1	0	0	0	0		

NOTES

1. Figure 4(a) illustrates one series of Test Patterns. Any other pattern series must be agreed with the Qualifying Space Agency and shall be included as an Appendix.
2. Logic Level Definitions: $1 = V_{IH} = V_{DD}$, $0 = V_{IL} = V_{SS}$.
3. From pattern 6 onwards, the figure indicated in the "Pin 11" column is the total number of $\phi 1$ pulses that must be applied to obtain the indicated output conditions.

FIGURE 4(b) - QUIESCENT CURRENT TEST TABLE

PATTERN No.	PIN NUMBERS														I_{DD} TEST	D.C. SUPPLY	
	1	2	3	4	5	6	7	9	10	11 (NOTE 3)	12	13	14	15		8	16
1	0	0	0	0	0	0	0	0	1	0	1	0	0	0		0	V_{DD}
2	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1		
3	0	0	0	0	0	0	0	1	0	5461	0	0	0	0			
4	1	0	1	0	1	1	0			0	0	1	0	0	2		
5	0	1	0	0	1	1	0			5461	0	1	0	0			
6	0	1	0	1	0	0	1			0	0	0	1	1	3		
7	1	0	1	1	0	0	1			5461	0	0	1	1			
8	1	1	1	1	1	1	1			0	0	1	1	1	4		
9	0	0	0	0	0	0	0			0	0	0	0	0	5		

NOTES

1. Figure 4(b) illustrates one series of Test Patterns. Any other pattern series must be agreed with the Qualifying Space Agency and shall be included as an Appendix.
2. Logic Level Definitions: $1 = V_{IH} = V_{DD}$, $0 = V_{IL} = V_{SS}$.
3. The figure indicated in the "Pin 11" column is the total number of $\phi 1$ pulses that must be applied to obtain the indicated output conditions.