DOCUMENT CHANGE REQUEST

DCR number 149	Changes required for: N/A	Originator: S Thacker
Date: 2005/03/30	Date sent: 2005/03/30	Organisation: ESA/ESTEC
Status: IMPLEMENTED		

Title:	Generic Specification for Discrete Semiconductor Components		
Number:	5000	Issue:	1

Other documents affected:

Page:

Specification 5000 issue 1 is re-written as issue 2 draft F to incorporate changes as summarised herein (see Appendix 1 for proposed issue 2 draft F).

The layout, format and general content of 5000 issue 2 draft F are based closely on the latest re-writ

Paragraph:

Specification 5000 issue 1 is re-written as issue 2 draft F to incorporate changes as summarised herein (see Appendix 1 for proposed issue 2 draft F).

The layout, format and general content of 5000 issue 2 draft F are based closely on the latest re-writ

Original wording:

Proposed wording:

The following changes have been applied to ESCC 5000 issue 1 (as contained in both ESCC 5000 issue 2 and ESCC 5000H Draft 1'D'):

a) Qualification and Lot Acceptance Testing have been incorporated, with some modifications, into a single Chart "Qualification and Periodic Tests".
Periodic testing is mandatory for ESCC qualified components with a defined testing schedule.
Lot Acceptance Testing has been deleted but an option for Lot Validation Testing during procurement has been added.
Specific changes to qualification & LAT testing include:
- High Temperature storage Test has been deleted from Qualification testing.
- Operating Life is always 2000hours (previously was 2000hours for Qual / 1000hours for LAT2)
- Solderability testing is deleted from Qual/LAT and is now part of Screening on a sample basis.

b) The SCC testing level C has been deleted; there is now only a single ESCC testing level equivalent to old SCC level B.

c) Final Production Tests & Burn-in and Electrical Measurements Charts have been incorporated, with some minor modifications, into a single Chart "Screening Tests"

d) Lot failure notification time is now 5 working days (was 2).

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e) The minimum required documentation for procurement is only a Certificate of Conformity & a Cover sheet.

f) Check for lot failure during Screening (PDA), only includes Electrical Parameter limit and Drift limit failures (excluding the mechanical, handling, lost, visual and seal test failures counting towards PDA in ESCC 5000 issue 1)

g) High Temperature Stabilisation Bake duration has been changed from 48 hours to 24 hours.

h) Constant Acceleration during Screening has been deleted.

i) For PIND testing the additional notes relating to PIND pre-screening, internal package height & test frequency, requirement for 5 test cycles, cumulative defects allowed and PDA requirements are deleted.

j) Dimension check is performed on 3 samples instead of 5.

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Many of the various changes incorporated into ESCC 9000 issue 3 as detailed and justified in DCR50/DCR138 have also been included in ESCC 5000 issue 2 draft F. These include the following main editorial, policy and technical changes:

k) The Specification has been made applicable and fully usable for procurement of unqualified components as well as for ESCC Qualified components.

l) Reference to the MIL-STD & IEC sampling standards have been deleted.

m) The requirements for Radiation testing and the Radiation test level have been clarified.

n) The General Flow Chart has been redrawn to clarify the flow of components for Procurement plus a new Chart for Production Control has been added.

o) The "check for lot failure" requirement during Screening has been clarified.

p) Solderability testing has been clarified to allow the use of suitable empty packages or electrical rejects plus to identify the samples as destructive.

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Additional changes that apply specifically to ESCC 5000 issue 1 and/or ESCC 5000H Draft 1'D' (not related to DCR50/DCR138) are as follows:

q) Scanning Electron Microscope (SEM) Inspection has been added to Wafer Lot Acceptance testing during Production Control. Originally in 5000H Draft 1'D' SEM was required on all types and all lots of components processed to ESCC 5000.

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This has been changed in ESCC 5000 issue 2 draft F to only require SEM inspection if specified in the detail specification. (SEM was not required in ESCC 5000 issue 1).

r) The sample size applicable to High & Low Temperature Electrical Measurements during Screening is changed in ESCC 5000 issue 2 draft F to be the equivalent fixed sample (5 components) rather than "GI Level II AQL 2.5%" per ESCC 5000H Draft 1'D'. (Note: the sample was LTPD7 = 32 components originally in ESCC 5000 issue 1)

s) The Power Burn-in duration is amended to be "168 hours minimum to 264 hours maximum".Previously only 168 hours (minimum) was specified.

t) A note is added to the Screening Chart in ESCC 5000 issue 2 draft F: "Verification of Safe Operating Area may be performed at any point prior to Initial Parameter Drift Value measurements."

u) see attachment

v) For Seal test additional notes and requirements have been added in ESCC 5000H Draft1'D' and ESCC 5000 issue 2 draft F as follows:
- Fine leak is not to be tested for components with cavities <=0.05ccm; for components with cavities >0.05 to 40ccm specific leak rate limits have been specified.
- A different method (MIL-STD-750 Method 1071 Condition E) shall apply to components without cavities
- Glass diodes shall not be painted until after seal test during Screening. Any paint shall be removed before seal testing during qualification and periodic tests.

w) Operating Life has an added category test method for "MOSFETs" in ESCC 5000 issue 2 draft F.

x) HTRB Burn-in has added categories for test methods and durations for "MOSFETs" and "All Other Devices" in ESCC 5000 issue 2 draft F.

y) Power Burn-in has added categories for test methods for "MOSFETs" and "All Other Devices" in ESCC 5000 issue 2 draft F.

Justification:

All changes have been defined and included to serve the purposes of technical improvement, clarification, accuracy, completeness, simplification and consistency. The aim is to simplify and improve the content and interpretation of the specification and it's requirements whilst maintaining an acceptable technical baseline and the same overall structure as the previous ESCC 5000 issue 1 (ESA/SCC 5000 issue 9A) and ESCC 5000H Draft 1'D' specifications.

In addition 5000 issue 2 draft F has been re-written to closely follow the layout, format and content of new ESCC 9000 issue 3 per DCR50/DCR138. The justifications for the same changes given in DCR50/DCR138 also apply to this DCR.

Justifications for the additional changes that apply specifically to ESCC 5000 issue 1 and/or ESCC 5000H Draft 1'D' (not

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related to DCR50) are as follows:

q) SEM inspection only applies to a limited range of component types covered by ESCC 5000. The majority of component types do not require SEM inspection.

r) The use of a fixed, defined, equivalent sample is considered a clearer option.

s) By specifying upto 240 (+24) hours as the burn-in duration it allows amnufactuers to provide ESCC components to customers who request a 240 hours minimum burn-in whilst still maintaining the minumum ESCC standard of 168 hours minimum.

x), y) All possible component types are served by this addition.

t) This restores some flexibility for the manufacturer to perform V.S.O.A. test as was applied in ESCC 5000 issue 1 (to be performed immediately prior to pre-burn-in electrical test) without any impact on quality.

u) The conditions specified for Thermal Shock in Screening and Qualification tests were potentially inconsistent with the ratings of the individual devices (maximum storage temperature rating), inconsistent with the aim of defining more severe test conditions for Qualification tests and inconsistent with the JANS equivalent requirements.

v) An option to remove paint from painted glass diodes before qual level seal testing is added to ensure a successful and valid seal test.

w), x), y) MOSFET is one of the standard component types used within ESCC 5000 plus all possible component types are served by this addition.

Attachments:

Attachment_to_DCR_149.pdf, 5000.pdf, null

Modifications:

N/A

Approval signature:

Date signed:

2005-03-30

DISCRETE SEMICONDUCTOR COMPONENTS, HERMETICALLY SEALED

ESCC Generic Specification No. 5000

Issue 2 - Draft F	June 2005

Document Custodian: European Space Agency - see https://escies.org

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(Refer to https://escies.org for ESCC DCR content)

DCR No.	CHANGE DESCRIPTION
147, 149	Specification upissued to incorporate editorial technical and Policy changes per DCR.

TABLE OF CONTENTS

1. INTRODUCTION

1.1 SCOPE

This specification defines the general requirements for the qualification, qualification maintenance, procurement, and delivery of hermetically sealed discrete semiconductor components for space applications. This specification contains the appropriate inspection and test schedules and also specifies the data documentation requirements.

1.2 APPLICABILITY

This specification is primarily applicable to the granting of qualification approval to a component in accordance with ESCC Basic Specification No. 20100 and the procurement of such components from qualified Manufacturers. It may also be applied for procurement of unqualified components.

2. APPLICABLE DOCUMENTS

The following documents form part of, and shall be read in conjunction with, this specification. The relevant issues shall be those in effect on the date of starting qualification or placing the Purchase Order.

2.1 ESCC SPECIFICATIONS

– No. 20100, Requirements for the Qualification of Standard Electronic Components for Space Application.
– No. 20400, Internal Visual Inspection.
– No. 20500, External Visual Inspection.
– No. 20600, Preservation, Packaging and Dispatch of ESCC Electronic Components.
– N0. 20900, Radiographic Inspection.
– No. 21300, Terms, Definitions, Abbreviations, Symbols and Units.
– No. 21400, Scanning Electron Microscope Inspection of Semiconductor Dice.
– No. 21700, General Requirements for the Marking of ESCC Components.
– No. 22800, ESCC Non-conformance Control System.
– No. 22900, Total Dose Steady-State Irradiation Test Method.
– No. 23500, Lead Materials and Finishes for Components for Space Application.
– No. 23800, Electrostatic Discharge Sensitivity Test Method.
– No. 24600, Minimum Quality System Requirements.
– No. 24800, Resistance to Solvents of Marking, Materials and Finishes.

For qualification and qualification maintenance or procurement of qualified components, with the exception of ESCC Basic Specifications Nos. 20100, 21700, 22800 and 24600, where Manufacturers' specifications are equivalent to, or more stringent than, the ESCC Basic Specifications listed above, they may be used in place of the latter, subject to the approval of the ESCC Executive.

Such replacements shall be clearly identified in the applicable Process Identification Document (PID).

For procurement of unqualified components, where Manufacturers' specifications are equivalent to or more stringent than the ESCC Basic Specifications listed above, they may be used in place of the latter subject to the approval of the Orderer.

Such replacements may be listed in an appendix to the appropriate Detail Specification at the request of the Manufacturer or Orderer, subject to the approval of the ESCC Executive.

Unless otherwise stated herein, references within the text of this specification to "the Detail Specification" shall mean the relevant ESCC Detail Specification.

2.2 OTHER (REFERENCE) DOCUMENTS

– ECSS-Q-70-02, Thermal Vacuum Test for the Screening of Space Materials.
– MIL-STD-202, Test Methods for Electronic and Electrical Component Parts.
– MIL-STD-750, Test Methods for Semiconductor Devices.
– MIL-STD-883, Test Methods and Procedures for Micro-electronics.

2.3 ORDER OF PRECEDENCE

For the purpose of interpretation and in case of conflict with regard to documentation, the following order of precedence shall apply:

(a) ESCC Detail Specification.
(b) ESCC Generic Specification.
(c) ESCC Basic Specification.
(d) Other documents, if referenced herein.

3. TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

The terms, definitions, abbreviations, symbols and units specified in ESCC Basic Specification No. 21300 shall apply.

4. REQUIREMENTS

4.1 GENERAL

The test requirements for the component type qualification of a component shall comprise Special In-Process Controls, Wafer Lot Acceptance with radiation tests (if specified), Screening Tests and Component Type Qualification Testing.

The test requirements for procurement of components shall comprise Special In-Process Controls, Wafer Lot Acceptance with radiation tests if required in the Purchase Order, Screening Tests, together with Periodic Testing for qualified components and Lot Validation Testing for qualified (if required in the Purchase Order) and unqualified components (see Chart F1).

4.1.1 Specifications

For qualification, qualification maintenance, procurement and delivery of components in conformity with this specification, the applicable specifications listed in Section 2 of this document shall apply in total unless otherwise specified herein or in the Detail Specification.

4.1.2 Conditions and Methods of Test

The conditions and methods of test shall be in accordance with this specification, the ESCC Basic Specifications referenced herein and the Detail Specification.

4.1.3 Manufacturer's Responsibility for Performance of Tests and Inspections

The Manufacturer shall be responsible for the performance of tests and inspections required by the applicable specifications. These tests and inspections shall be performed at the plant of the Manufacturer of the components unless it is agreed by the ESCC Executive (for qualification, qualification maintenance, or procurement of qualified components) or the Orderer (for procurement of unqualified

components), to use an approved external facility.

4.1.4 Inspection Rights

The ESCC Executive (for qualification, qualification maintenance, or procurement of qualified components) or the Orderer (for procurement of unqualified components) reserves the right to monitor any of the tests and inspections scheduled in the applicable specifications.

4.1.5 Pre-encapsulation Inspection Witnessing

If required in the Purchase Order, the Orderer may witness or perform the pre-encapsulation inspection and the Manufacturer must notify the Orderer at least 2 working weeks before the commencement of the inspection.

4.2 QUALIFICATION AND QUALIFICATION MAINTENANCE REQUIREMENTS ON A MANUFACTURER

To obtain and maintain the component type qualification of a component, or family of components, a Manufacturer shall satisfy the requirements of ESCC Basic Specification No. 20100.

4.3 DELIVERABLE COMPONENTS

Components delivered to this specification shall be processed and inspected in accordance with the relevant Process Identification Document (PID). Each delivered component shall be traceable to its production lot. Components delivered to this specification shall have satisfactorily completed all the required tests.

ESCC qualified components delivered to this specification shall be produced from lots that are capable of passing all applicable tests, and sequences of tests, that are defined in Chart F4. The Manufacturer shall not knowingly supply components that cannot meet this requirement. In the event that, subsequent to delivery and prior to operational use, a component is found to be in a condition such that it could not have passed these tests at the time of manufacture, this shall be grounds for rejection of the delivered lot.

4.3.1 Lot Failure

Lot failure may occur during Special In-Process Controls (Chart F2), Wafer Lot Acceptance (Chart F2), Screening Tests (Chart F3), or Qualification and Periodic Tests (Chart F4).

Should such failure occur during qualification, qualification maintenance or procurement of qualified components the Manufacturer shall initiate the non-conformance procedure in accordance with ESCC Basic Specification No. 22800. The Manufacturer shall notify the Orderer and the ESCC Executive by any appropriate written means, within 5 working days, giving details of the number and mode of failure and the suspected cause. No further testing shall be performed on the failed components.

Should such failure occur during procurement of unqualified components the Manufacturer shall notify the Orderer by any appropriate written means within 5 working days, giving details of the number and mode of failure and the suspected cause. No further testing shall be performed on the failed components. The Orderer shall inform the Manufacturer within 5 working days of receipt of notification what action shall be taken.

4.4 MARKING

All components procured and delivered to this specification shall be marked in accordance with ESCC Basic Specification No. 21700.

4.5 MATERIALS AND FINISHES

Specific requirements for materials and finishes are specified in the Detail Specification. Where a definite material or finish is not specified a material or finish shall be used so as to ensure that the component meets the performance requirements of this specification and the Detail Specification. Acceptance or approval of any constituent material or finish does not guarantee acceptance of the finished product.

Unless otherwise specified in the Detail Specification the component shall be hermetically sealed.

All non-metallic materials and finishes, that are not within a hermetically sealed enclosure, of the components specified in the detail specification shall meet the outgassing requirements as outlined in ECSS-Q-70-02.

4.6 RADIATION TESTING

For qualification or qualification maintenance radiation testing shall be performed when specified in the Detail Specification to the total dose level given.

For procurement as required in the Purchase Order radiation testing shall be performed to the total dose level given in the Detail Specification or to an alternate level if so required in the Purchase Order.

The qualification status of the procured components shall not be impacted by any change to the total dose level applied.

For procurement any lot of components that fails the required total dose radiation test level may be accepted to a lower level of radiation subject to satisfactory test results at the lower level. In this case the total dose radiation level letter for the lot shall be modified accordingly.

5. PRODUCTION CONTROL

5.1 GENERAL

The minimum requirements for production control are defined in the Process Identification Document (PID).

Unless otherwise specified in the Detail Specification all lots of components used for qualification and qualification maintenance, Lot Validation Testing and for delivery shall be subject to tests and inspections in accordance with Chart F2.

Any components which do not meet these requirements shall be removed from the lot and at no future time be resubmitted to the requirements of this specification.

The applicable test requirements are detailed in the paragraphs referenced in Chart F2.

In the case of lot failure, the manufacturer shall act in accordance with Para. 4.3.1.

5.2 SPECIAL IN-PROCESS CONTROLS

5.2.1 Pre-encapsulation Inspection

Pre-encapsulation inspection shall consist of Internal Visual Inspection in accordance with Para. 8.1 plus Bond Strength and Die Shear tests in accordance with Para. 8.2.

Bond Strength and Die Shear tests shall be performed on test samples in accordance with Para. 8.2. A single failure shall be cause for lot failure. These tests are considered as destructive and therefore components so tested shall not form part of the delivery lot.

5.2.2 Dimension Check

In accordance with Para. 8.10 on 3 samples only.

If a failure occurs, the complete lot shall be checked.

5.2.3 Weight

The maximum weight of the component specified in the Detail Specification shall be guaranteed but not tested.

5.2.4 Documentation

Documentation of Special In-Process Controls shall be in accordance with Para. 9.5.

5.3 WAFER LOT ACCEPTANCE

5.3.1 Process Monitoring Review

Process monitoring review shall be done in compliance with the Manufacturer's SPC rules described in the PID.

A wafer shall be rejected if one or more process control data parameters exceed the allowed distribution as specified in the PID.

5.3.2 Scanning Electron Microscope (SEM) Inspection

If specified in the Detail Specification, components supplied to this specification shall be produced from wafer lots that have been subjected to, and successfully met, the scanning electron microscope inspection requirements in accordance with Para. 8.3.

5.3.3 Total Dose Radiation Testing

For qualification or qualification maintenance:

– If specified in the Detail Specification, components shall be produced from a wafer lot which has been subjected to and successfully completed Total Dose Radiation Testing in accordance with Para. 8.4 to the total dose level given.

During procurement:

– If specified in the Detail Specification and required in the Purchase Order, components shall be produced from a wafer lot which has been subjected to and successfully completed Total Dose

Radiation Testing in accordance with Para. 8.4 to the required total dose level.

5.3.4 Documentation

Documentation of Wafer Lot Acceptance shall be in accordance with Para. 9.6.

6. SCREENING TESTS

6.1 GENERAL

Unless otherwise specified in the Detail Specification, all components used for qualification and qualification maintenance, Lot Validation Testing, and for delivery, shall be subjected to tests and inspections in accordance with Chart F3. All components shall be serialised prior to the tests and inspections.

Unless otherwise specified in the Detail Specification, the tests shall be performed in the order shown.

Any components which do not meet these requirements shall be removed from the lot and at no future time be resubmitted to the requirements of this specification.

The applicable test methods and conditions are specified in the paragraphs referenced in Chart F3.

6.2 FAILURE CRITERIA

6.2.1 Environmental and Mechanical Test Failure

The following shall be counted as component failures:- components which fail during tests for which the pass/fail criteria are inherent in the test method, i.e. PIND, Radiographic Inspection, Solderability, Seal.

6.2.2 Parameter Drift Failure

The acceptable change limits are shown in Parameter Drift Values in the Detail Specification. A component shall be counted as a parameter drift failure if the changes during High Temperature Reverse Bias Burn-in or during Power Burn-in are larger than the drift values (Δ) specified.

6.2.3 Parameter Limit Failure

A component shall be counted as a limit failure if one or more parameters exceed the limits shown in Room Temperature Electrical Measurements or High and Low Temperatures Electrical Measurements in the Detail Specification.

Any component which exhibits a limit failure prior to the submission to HTRB Burn-in shall be rejected and not counted when determining lot rejection.

6.2.4 Other Failures

A component shall be counted as a failure in any of the following cases:

– External Visual Inspection failure.
– Mechanical failure.
– Handling failure.
– Lost component.

6.3 FAILED COMPONENTS

A component shall be considered as a failed component if it exhibits one or more of the failure modes described in Para. 6.2.

6.4 LOT FAILURE

In the case of lot failure, the Manufacturer shall act in accordance with Para. 4.3.1.

6.4.1 Lot Failure during 100% Testing

If the number of components failed on the basis of the failure criteria specified in Paras. 6.2.2 and 6.2.3 exceeds 5% (rounded upwards to the nearest whole number) of the components submitted to initial measurements of Parameter Drift Values of Chart F3, the lot shall be considered as failed.

If a lot is composed of groups of components of one family defined in one ESCC Detail Specification, but separately identifiable for any reason, then the lot failure criteria shall apply separately to each identifiable group.

6.4.2 Lot Failure during Sample Testing

A lot shall be considered as failed if the number of allowable failures during sample testing as specified in the Detail Specification, is exceeded.

If a lot failure occurs, a 100% testing may be performed but the cumulative percent defective shall not exceed that given in Para. 6.4.1.

No failures are allowed for the Solderability test.

6.5 DOCUMENTATION

Documentation of Screening Tests shall be in accordance with Para. 9.7.

7. QUALIFICATION, QUALIFICATION MAINTENANCE AND LOT VALIDATION TESTING

Requirements of this paragraph are applicable to the tests performed for component type qualification and qualification maintenance and also for Lot Validation Testing.

7.1 COMPONENT TYPE QUALIFICATION TESTING

7.1.1 General

Qualification testing shall be in accordance with the requirements given in Chart F4. The tests of Chart F4 shall be performed on the specified sample, chosen at random from components which have successfully passed the tests in Chart F3 (Screening Tests). This sample constitutes the qualification test lot.

The qualification test lot is divided into subgroups of tests and all components assigned to a subgroup shall be subjected to all of the tests in that subgroup, in the sequence shown. The applicable test requirements are detailed in the paragraphs referenced in Chart F4.

The conditions governing component type qualification testing are given in ESCC Basic Specification No. 20100.

7.1.2 Distribution within the Qualification Test Lot

Where a Detail Specification covers a range, or series of components that are considered similar, then

the qualification test lot shall be comprised of component types so selected that they adequately represent all of the various mechanical, structural and electrical peculiarities of that range or series.

The distribution shall be as specified by, or agreed with, the ESCC Executive.

7.2 QUALIFICATION MAINTENANCE (PERIODIC TESTING)

Component type qualification is maintained through periodic testing and the test requirements of Para. 7.1 shall apply. For each subgroup the period between successive subgroup testing shall be as given in Chart F4. The conditions governing qualification maintenance are given in ESCC Basic Specification No. 20100.

7.3 LOT VALIDATION TESTING

7.3.1 General

For qualified components, Lot Validation Testing as defined in compliance with Chart F4, Subgroup 2, shall only be performed on the procured lot if required in the Purchase Order.

If unqualified components are procured using this specification then the Orderer shall define in the Purchase Order the required subgroups from Chart F4 to be used for Lot Validation Testing.

7.3.2 Distribution within the Sample for Lot Validation Testing

Where the Detail Specification covers a range, or series, of components that are considered similar, then it is only necessary to perform Lot Validation Testing on representative types if a number of different types are procured together. The sample for Lot Validation Testing should be comprised of component types so selected that they adequately represent all of the various mechanical, structural and electrical peculiarities of the components procured from the range or series.

The distribution of component types will vary from procurement to procurement and shall be as required in the Purchase Order.

7.4 FAILURE CRITERIA

The following criteria shall apply to qualification, qualification maintenance and Lot Validation Testing.

7.4.1 Environmental and Mechanical Test Failures

The following shall be counted as component failures:-

Components which fail during tests for which the pass/fail criteria are inherent in the test method, e.g. Seal, Terminal Strength, etc.

7.4.2 Electrical Failures

The following shall be counted as component failures:

Components which fail one or more of the applicable limits at each of the relevant data points specified for environmental, mechanical and endurance testing in Intermediate and End-point Electrical Measurements in the Detail Specification.

7.4.3 Other Failures

A component shall be counted as a failure in any of the following cases:

– Visual Inspection failure

– Mechanical failure
– Handling failure
– Lost component

7.5 FAILED COMPONENTS

A component shall be considered as failed if it exhibits one or more of the failure modes detailed in Para. 7.4.

When requested by the ESCC Executive (for qualification, qualification maintenance or procurement of qualified components) or the Orderer (for procurement of qualified or unqualified components), failure analysis of failed components shall be performed by the Manufacturer and the results provided.

Failed components shall be retained at the Manufacturer's plant until the final disposition has been agreed and certified.

7.6 LOT FAILURE

For qualification and qualification maintenance, the lot shall be considered as failed if one component in any subgroup of Chart F4 is a failed component based on the criteria given in Para. 7.4.

For procurement, the lot shall be considered as failed if one component in any test specified for Lot Validation Testing is a failed component based on the criteria given in Para. 7.4.

In the case of lot failure, the Manufacturer shall act in accordance with Para. 4.3.1.

7.7 QUALIFICATION, QUALIFICATION MAINTENANCE AND LOT VALIDATION TESTING SAMPLES

All tests of Chart F4 are considered to be destructive and therefore components so tested shall not form part of the delivery lot.

7.8 DOCUMENTATION

Documentation of qualification, qualification maintenance and Lot Validation Testing shall be in accordance with Para. 9.8.

8. TEST METHODS AND PROCEDURES

If a Manufacturer elects to eliminate or modify a test method or procedure, the Manufacturer is still responsible for delivering components that meet all of the performance, quality and reliability requirements defined in this specification and the Detail Specification.

For a qualified component, documentation supporting the change shall be approved by the ESCC Executive and retained by the Manufacturer. It shall be copied, when requested, to the ESCC Executive. The change shall be specified in an appendix to the Detail Specification and in the PID.

For an unqualified component the change shall be approved by the Orderer. The change may be specified in an appendix to the Detail Specification at the request of the Manufacturer or Orderer, subject to the approval of the ESCC Executive.

8.1 INTERNAL VISUAL INSPECTION

ESCC Basic Specification No. 20400.

8.2 BOND STRENGTH AND DIE SHEAR

8.2.1 Bond Strength

MIL-STD-750, Test Method 2037, Test Condition A or B.

Test Condition B shall only be permitted when Test Condition A cannot be used and never for bond wires of diameter less than 0.127mm.

Test Samples: For Special In-Process Controls 3 test samples shall be selected at random from the lot of components accepted after Internal Visual Inspection.

For Qualifications and Periodic Tests 3 test samples shall be selected from the components in subgroup 3 of Chart F4.

If agreed by the ESCC Executive (for qualification or qualification maintenance) or the Orderer (for procurement) the test samples for Special In-Process Controls may have only passed the low magnification phase of the Internal Visual Inspection.

Individual separation forces and categories shall be recorded. A single failure shall be cause for lot failure.

8.2.2 Die Shear

MIL-STD-750, Test Method 2017.

The same test samples submitted to Bond Strength shall be used. Individual separation forces and categories shall be recorded. A single failure shall be cause for lot failure.

8.3 SCANNING ELECTRON MICROSCOPE INSPECTION

Only applicable if specified in the Detail Specification.

ESCC Basic Specification No. 21400.

8.4 TOTAL DOSE RADIATION TESTING

ESCC Basic Specification No. 22900 to the total dose level specified in the Detail Specification or as required in the Purchase Order.

8.5 HIGH TEMPERATURE STABILISATION BAKE

MIL-STD-750, Test Method 1032, Duration: 24 hours at maximum storage temperature rating specified in the Detail Specification.

8.6 TEMPERATURE CYCLING

8.6.1 Screening Tests

MIL-STD-750, Test Method 1051, Test Condition C, 20 cycles or maximum storage temperature rating specified in the Detail Specification.

8.6.2 Qualification and Periodic Tests

Not applicable for axial lead glass diodes.

MIL-STD-750, Test Method 1051, Test Condition C, 100 cycles or maximum storage temperature rating specified in the Detail Specification.

8.7 PARTICLE IMPACT NOISE DETECTION (PIND)

Only applicable to devices with cavities.

MIL-STD-750, Test Method 2052, Test Condition A.

The use of the same attachment medium for the Sensitivity Test Unit and for the components under test is not mandatory.

8.8 SEAL

Glass diodes shall not be painted during Screening until after seal tests are completed. Any paint shall be removed prior to seal tests during Qualification and Periodic Tests.

8.8.1 Seal, Fine Leak

MIL-STD-750, Test Method 1071, Condition H1 or H2.

This test is not applicable to components with a cavity ≤0.05ccm. For components with cavities >0.05ccm, the maximum leak rate shall be as follows:

>0.05ccm to 0.3ccm	: $5x10^{-8}$ atm ccm/sec
>0.3ccm to 3ccm	: $5x10^{-7}$ atm ccm/sec
>3ccm to 40ccm	: $5x10^{-6}$ atm ccm/sec

8.8.2 Seal, Gross Leak

MIL-STD-750, Test Method 1071, Condition C or K for components with cavities.

MIL-STD-750, Test Method 1071, Condition E for clear glass components without cavities.

8.9 ELECTRICAL MEASUREMENTS

8.9.1 Parameter Drift Values

At each of the relevant data points during Screening Tests, Parameter Drift Values shall be measured as specified in the Detail Specification. All values obtained shall be recorded against serial numbers and the parameter drift calculated.

8.9.2 High and Low Temperatures Electrical Measurements

High and Low Temperatures Electrical Measurements shall be performed as specified in the Detail Specification. All values obtained shall be recorded against serial numbers. Unless otherwise specified measurements shall be performed on a sample of 5 components with 0 failures allowed. Alternatively a 100% inspection may be performed.

8.9.3 Room Temperature Electrical Measurements

Room Temperature Electrical Measurements shall be performed as specified in the Detail Specification. All values obtained shall be recorded against serial numbers.

8.9.4 Intermediate and End-Point Electrical Measurements

At each of the relevant data points during Qualification and Periodic Tests Intermediate and End-point Electrical Measurements shall be performed as specified in the Detail Specification. All values obtained shall be recorded against serial numbers and the parameter drift calculated, if specified.

8.10 EXTERNAL VISUAL INSPECTION AND DIMENSION CHECK

External Visual Inspection shall be performed in accordance with ESCC Basic Specification No. 20500.

Dimension Check (during Special In-Process Controls only) shall be performed in accordance with ESCC Basic Specification No. 20500 and the Detail Specification on a sample of 3 components. If a failure occurs the complete lot shall be checked.

8.11 MECHANICAL SHOCK

MIL-STD-750, Test Method 2016, 1500g, 0.5ms duration, 5 shocks, planes X1, Y1 and Z1.

8.12 VIBRATION

MIL-STD-750, Test Method 2056, 20g, 10-2000Hz, cross over at 50Hz.

8.13 CONSTANT ACCELERATION

MIL-STD-750, Test Method 2006, 20000g, planes X1, Y1 and Y2.

8.14 THERMAL SHOCK

Only applicable for axial lead glass diodes.

MIL-STD-750, Test Method 1056, Test Condition A, 25 cycles.

8.15 MOISTURE RESISTANCE

MIL-STD-750, Test Method 1021.

8.16 SOLDERABILITY

For procurement lots: 5 samples. A single failure shall be cause for lot failure.

MIL-STD-750, Test Method 2026, to be performed on all terminals.

Solderability testing may be performed on empty packages or electrical rejects. The test samples used must be of the same package type and must have been manufactured using the same process, at the same time and have been subjected to the same screening as the packages of the delivery lot with which they are associated.

For components with gold plated lead finish activated fluxes (RMA and RA) may be used but shall be immediately cleaned off after dipping using an acceptable solvent.

Solderability testing is classed as destructive and therefore components so tested shall not form part of the delivery lot.

8.17 PERMANENCE OF MARKING

ESCC Basic Specification No. 24800.

8.18 TERMINAL STRENGTH

MIL-STD-883, Test Method 2004, Test Condition D for chip carrier packages.

MIL-STD-750, Test Method 2036 for all other packages. Test Condition as specified in the Detail Specification.

8.19 OPERATING LIFE

Bipolar Devices: MIL-STD-750, Test Method 1026.

MOSFETs: MIL-STD-750, Test Method 1042, Conditions A and B

All other Devices: The test method shall be as specified in the Detail Specification.

– Duration: 2000 hours.

– Conditions: As specified in Operating Life in the Detail Specification.

– Data Points
As specified in Intermediate and End-point Electrical Measurements in the Detail Specification at 0 hours, 1000 ± 48 hours and 2000 ± 48 hours. If drift values are specified, the drift shall always be related to the 0-hour measurement.

8.20 HIGH TEMPERATURE REVERSE BIAS BURN-IN

Diodes and Rectifiers: MIL-STD-750, Test Method 1038, Test Condition A.

Bipolar Transistors: MIL-STD-750, Test Method 1039, Test Condition A.

MOSFETs: The test method shall be as specified in the Detail Specification.

All other Devices: The test method shall be as specified in the Detail Specification.

– Duration and Test Conditions
As specified in High Temperature Reverse Bias Burn-in in the Detail Specification. Unless otherwise specified the duration shall be:

MOSFETs: 48 hours minimum
All other devices: 12 hours minimum

– Data Points
As specified in the Parameter Drift Values in the Detail Specification at 0 hours and T (+24 -0) hours (where T is the specified duration).

8.21 POWER BURN-IN

Diodes and Rectifiers: MIL-STD-750, Test Method 1038, Test Condition B.

Bipolar Transistors: MIL-STD-750, Test Method 1039, Test Condition B.

Thyristors: MIL-STD-750, Test Method 1040, Test Condition B.

MOSFETs: The test method shall be as specified in the Detail Specification.

All other Devices: The test method shall be as specified in the Detail Specification.

– Duration
Unless otherwise specified in the Detail Specification, components shall be subjected to a total Power Burn-in period of 168 hours minimum and 264 hours maximum.

– Test Conditions
As specified in Power Burn-in in the Detail Specification.

– Data Points
As specified in Parameter Drift Values in the Detail Specification at T (+24 -0) hours (where T is the specified duration).

If High Temperature Reverse Bias Burn-in is not being performed, the 0 hours (initial) measurement is also required.

8.22 VERIFICATION OF SAFE OPERATING AREA

If specified in the Detail Specification, a verification of the safe operating area shall be performed. The specified Test Method(s), specific conditions and limits shall be as given in the Detail Specification.

The Test Method(s) shall be selected from the following:

Bipolar Transistors :	Maximum Continuous d.c.	: MIL-STD-750, Test Method 3051.
	Pulsed	: MIL-STD-750, Test Method 3052.
	Switching	: MIL-STD-750, Test Method 3053. The load conditions shall also be specified.

MOSFETs and Insulated Gate Bipolar Transistors (IGBT): MIL-STD-750, Test Method 3474.

All other Devices: The test method shall be as specified in the Detail Specification.

8.23 RADIOGRAPHIC INSPECTION

Not applicable for diodes with transparent packages.

ESCC Basic Specification No. 20900.

9. DATA DOCUMENTATION

9.1 GENERAL

For the qualification, qualification maintenance and procurement for each lot a data documentation package shall exist in a printed or electronic form.

This package shall be compiled from:

(a) Cover sheet (or sheets).
(b) List of equipment (testing and measuring).
(c) List of test references.
(d) Special In-Process Controls data (Chart F2).
(e) Wafer Lot Acceptance data (Chart F2) (when applicable).
(f) Screening Tests data (Chart F3).
(g) Qualification and Periodic Tests data including Lot Validation Testing data (when applicable) (Chart F4).
(h) Failed components list and failure analysis report (when applicable).
(i) Certificate of Conformity.

Items (a) to (i) inclusive shall be grouped, preferably as subpackages and, for identification purposes, each page shall include the following information:

– ESCC Component Number.
– Manufacturer's name.
– Lot identification.
– Date of establishment of the document.
– Page number.

Whenever possible, documentation should preferably be supplied in electronic format suitable for reading using a compatible PC. The format supplied shall be legible, durable and indexed. The preferred storage media are 3 1/2 inch diskettes or CD-ROMs and the preferred file formats are ASCII or PDF.

9.1.1 Qualification and Qualification Maintenance

In the case of qualification or qualification maintenance, the items listed in Para. 9.1(a) to (i) are required.

9.1.2 Component Procurement and Delivery

For all deliveries of components procured to this specification, the following documentation shall be supplied:

(a) Cover sheet (if all of the information is not included on the Certificate of Conformity).
(b) Certificate of Conformity (including range of delivered serial numbers).

9.1.3 Additional Documentation

The Manufacturer shall deliver additional documentation containing data and reports to the Orderer, if required in the Purchase Order.

9.1.4 Data Retention/Data Access

If not delivered, all data shall be retained by the Manufacturer for a minimum of 5 years during which time it shall be available for review, if requested, by the Orderer or the ESCC Executive (for qualified components).

9.2 COVER SHEET(S)

The cover sheet(s) of the data documentation package shall include as a minimum:

(a) Reference to the Detail Specification, including issue and date.
(b) Reference to the applicable ESCC Generic Specification, including issue and date.
(c) ESCC Component Number and the Manufacturers part type number.

(d) Lot identification.
(e) Range of delivered serial numbers.
(f) Number of the Purchase Order.
(g) Radiation testing level (if applicable).
(h) Information relative to any additions to this specification and/or the Detail Specification.
(i) Manufacturer's name and address.
(j) Location of the manufacturing plant (specify place of diffusion, assembly and test).
(k) Signature on behalf of Manufacturer.
(l) Total number of pages of the data package.

9.3 LIST OF EQUIPMENT USED

A list of equipment used for tests and measurements shall be prepared, if not in accordance with the data given in the PID. Where applicable, this list shall contain inventory number, Manufacturer's type number, serial number, etc. This list shall indicate for which tests such equipment was used.

9.4 LIST OF TEST REFERENCES

This list shall include all Manufacturer's references or codes which are necessary to correlate the test data provided with the applicable tests specified in the tables of the Detail Specification.

9.5 SPECIAL IN-PROCESS CONTROLS DATA (CHART F2)

A test result summary shall be compiled, showing the total number of components submitted to, and the total number rejected after each of the tests. For the Bond Strength and Die Shear tests, the separation forces and categories shall be recorded.

9.6 WAFER LOT ACCEPTANCE DATA (CHART F2)

Data of SEM Inspection shall be prepared in accordance with the requirements of ESCC Basic Specification No. 21400 (if specified).

Radiation test report shall be prepared in accordance with the requirements of ESCC Basic Specification No. 22900 (if specified).

9.7 SCREENING TESTS DATA (CHART F3)

A test result summary shall be compiled showing the total number of components submitted to and the total number rejected after each of the tests. For each test requiring electrical measurements the results shall be recorded against component serial number. Component drift calculations shall be recorded for each specified test against component serial number.

9.8 QUALIFICATION AND PERIODIC TESTS DATA (CHART F4)

9.8.1 Qualification Tests

A test result summary shall be compiled showing the components submitted to and the number rejected after each test in each subgroup. Component serial numbers for each subgroup shall be identified. For each test requiring electrical measurements the results shall be recorded against component serial number. Where a drift value is specified during a test the drift calculation shall be recorded against component serial number.

9.8.2 Periodic Testing for Qualification Maintenance

A test result summary shall be compiled showing the components submitted to and the number rejected after each test in each subgroup. Component serial numbers for each subgroup shall be identified. For each test requiring electrical measurements the results shall be recorded against component serial number. Where a drift value is specified during a test the drift calculation shall be recorded against component serial number.

In addition to the full test data a report shall be compiled for each subgroup of Chart F4 to act as the most recent Periodic Testing summary. These reports shall include a list of all tests performed in each subgroup, the ESCC Component Numbers and quantities of components tested, a statement confirming all the results were satisfactory, the date the tests were performed and a reference to the full test data.

9.8.3 Lot Validation Testing

A test result summary shall be compiled showing the components submitted to and the number rejected after each test in each subgroup (as applicable). Component serial numbers for each subgroup shall be identified. For each test requiring electrical measurements the results shall be recorded against component serial number. Where a drift value is specified during a test the drift calculation shall be recorded against component serial number.

9.9 FAILED COMPONENTS LIST AND FAILURE ANALYSIS REPORT

The failed components list and failure analysis report shall provide full details of:

(a) The reference and description of the test or measurement performed as defined in this specification and/or the Detail Specification during Special In-Process Controls, Wafer Lot Acceptance, Screening Tests and Qualification and Periodic Tests.
(b) The serial number (if applicable) of the failed component.
(c) The failed parameter and the failure mode of the component.
(d) Detailed failure analysis (if requested by the ESCC Executive or Orderer).

9.10 CERTIFICATE OF CONFORMITY

A Certificate of Conformity shall be established as defined in ESCC Basic Specification No. 20100.

10. DELIVERY

For procurement, for each order, the items forming the delivery are:

(a) The delivery lot.
(b) The components used for Lot Validation Testing (when applicable), but not forming part of the delivery lot.
(c) The relevant documentation in accordance with the requirements of Section 9.

In the case of a component for which a valid qualification is in force, all data of all components submitted to Lot Validation Testing shall also be copied, when requested, to the ESCC Executive.

For qualification or qualification maintenance, the disposition of the test lot and its related documentation shall be as specified in ESCC Basic Specification No 20100 and the relevant paragraphs of Section 9 of this specification.

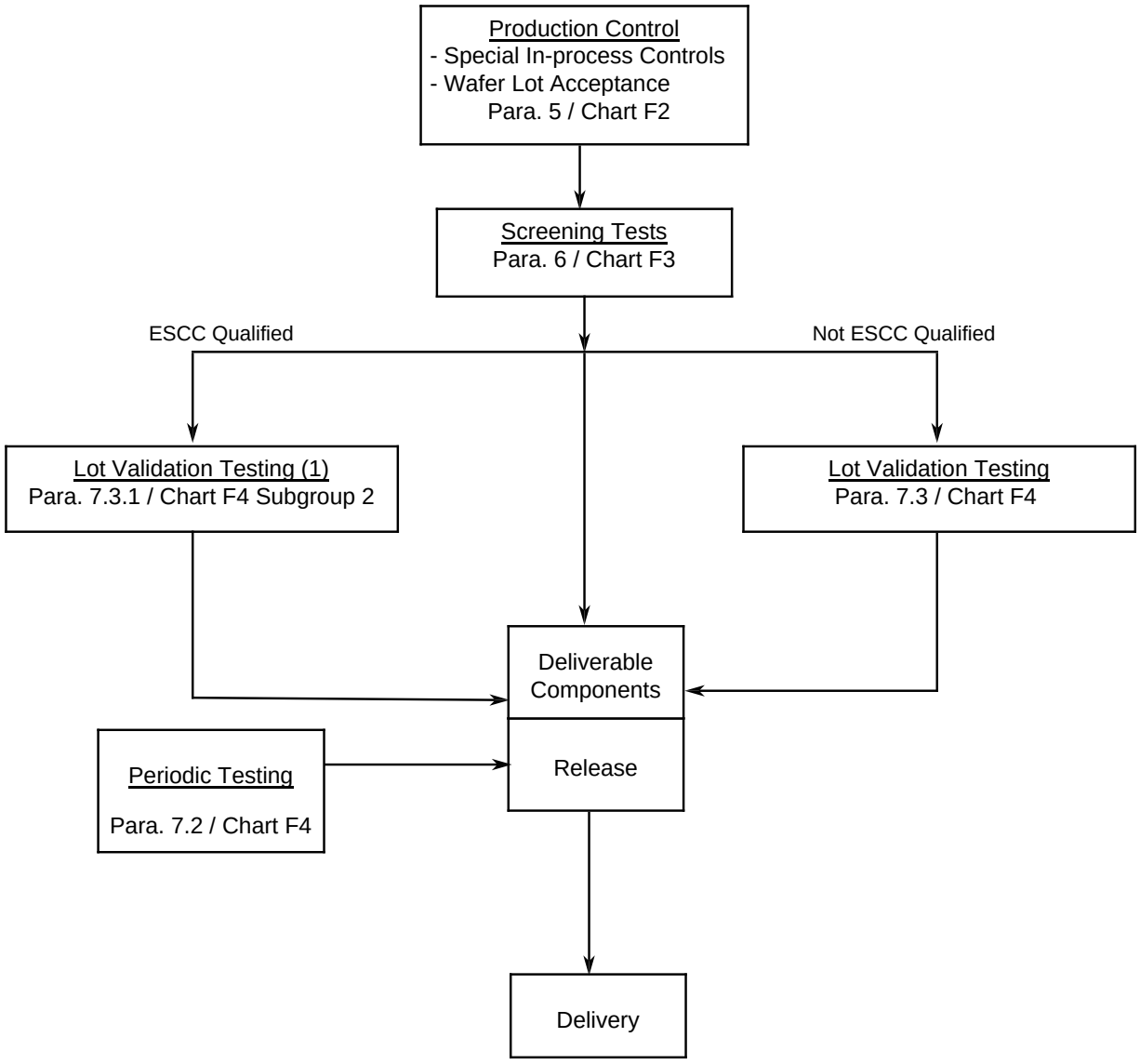
11. PACKAGING AND DISPATCH

The packaging and dispatch of components to this specification shall be in accordance with the

requirements of ESCC Basic Specification No. 20600.

12. CHARTS

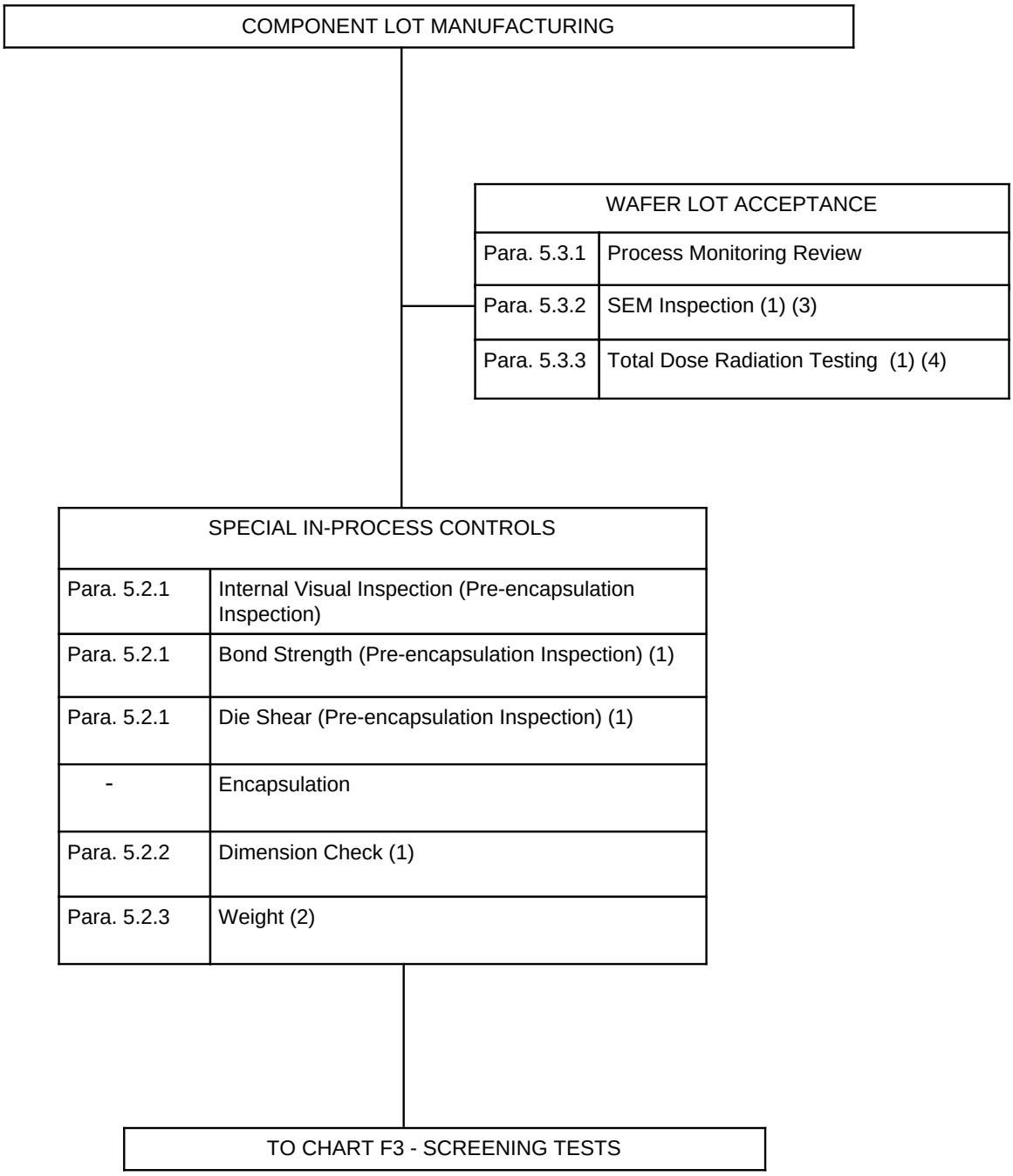
12.1 CHART F1 - GENERAL FLOW FOR PROCUREMENT



NOTES:

1. Lot Validation Testing is optional for qualified components and shall only be performed if required in the Purchase Order.

12.2 CHART F2 - PRODUCTION CONTROL



NOTES:
1. Performed on a sample basis.
2. Guaranteed but not tested.
3. If specified in the Detail Specification.
4. If specified in the Detail Specification and required in the Purchase Order.

12.3 CHART F3 - SCREENING TESTS

COMPONENTS FROM PRODUCTION CONTROL (1)	
Para. 8.22	Verification of Safe Operating Area (2)
Para. 8.5	High Temperature Stabilisation Bake
Para. 8.6.1	Temperature Cycling
Para. 8.7	Particle Impact Noise Detection (PIND)
Para. 8.9.1	Parameter Drift Values (Initial Measurements)
Para. 8.20	High Temperature Reverse Bias Burn-in
Para. 8.9.1	Parameter Drift Values (Final Measurements for HTRB; Initial Measurements for Power Burn-in) (3)
Para. 8.21	Power Burn-in
Para. 8.9.1	Parameter Drift Values (Final Measurements) (3)
Para. 8.9.2	High and Low Temperatures Electrical Measurements (3) (4)
-	Hot Solder Dip (if applicable) (5)
Para. 8.9.3	Room Temperature Electrical Measurements (3) (6)
Para. 6.4.1	Check for Lot Failure (7)
Para. 8.23	Radiographic Inspection (8)
Para. 8.8.1 and Para. 8.8.2	Seal (Fine and Gross Leak)
Para. 8.10	External Visual Inspection
Para. 8.16	Solderability (3) (4)
TO CHART F4 WHEN APPLICABLE	

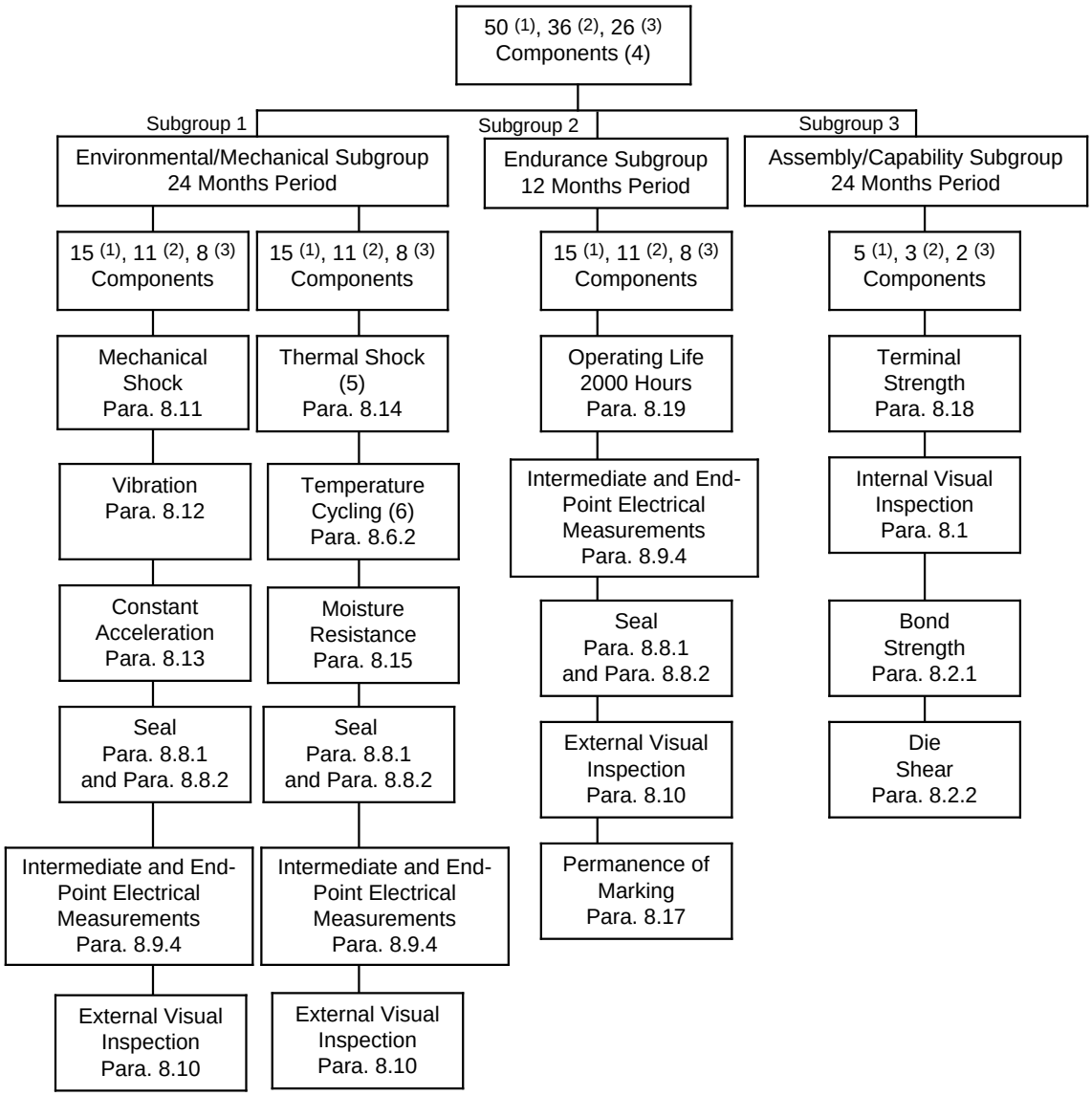
NOTES:

1. All components shall be serialised prior to Screening Tests.
2. If specified in the Detail Specification. Verification of Safe Operating Area may be performed at any point prior to Initial measurements of Parameter Drift Values.
3. The lot failure criteria of Para. 6.4 apply to this test.
4. Performed on a sample basis.
5. For components with hot solder dip final lead finish the hot solder dip processing shall be performed

at any time prior to Room Temperature Electrical Measurements during Screening Tests. The requirements for hot solder dip are specified in ESCC Basic Specification No. 23500.

6. Measurements of Parameter Drift Values need not be repeated in Room Temperature Electrical Measurements.
7. Check for Lot Failure shall take into account all electrical parameter failures that may occur during Screening Tests in accordance with Para. 8.9.1, 8.9.2, 8.9.3 subsequent to HTRB Burn-in.
8. Radiographic Inspection may be performed at any point during Screening Tests. It is not applicable for diodes with transparent packages.

12.4 CHART F4 - QUALIFICATION AND PERIODIC TESTS



NOTES:

1. Single type (see Para. 7.1.2)
2. Per type for two types selected (see Para. 7.1.2)
3. Per type for three or more types selected (see Para. 7.1.2)
4. No failures are permitted.
5. Only applicable to axial lead glass diodes.
6. Not applicable to axial lead glass diodes.

Attachment to DCR 149

Proposed Wording of Change Continued

u) Thermal Shock during Screening tests and Qualification testing is modified to align the conditions with the equivalent as specified for JANS devices per MIL-PRF-19500M.

Thermal Shock during screening is amended to the Temperature Cycling as follows:

Package	Current Conditions	New Conditions
Metal/Ceramic	-65 to +125°C, 20 cycles, air	-55 to +175°C (or max rating) 20 cycles, air
Glass	-65 to +200°C, 20 cycles, air	

Thermal Shock during Qualification is split into Thermal Shock and Temperature Cycling as follows:

Package	Current Conditions	New Conditions
Metal/Ceramic	-65 to +125°C, 20 cycles, air	-55 to +175°C (or max rating) 100 cycles, air (T. Cycling)
Glass	0 to +100°C, 10 cycles, liquid	0 to 100°C, 25 cycles, liquid (glass diodes) (T. Shock)