DOCUMENT CHANGE REQUEST

DCR number 994	Changes required for: General	Originator: Steve Thacker
Date: 2017/04/19	Date sent: 2016/05/18	Organisation: ESCC Executive Secretariat
Status: IMPLEMENTED		

Title:	Generic Specification for Discrete Microwave Semiconductor Components		
Number:	5010	Issue:	2

Other documents affected:

Page:

See attached 5010 Draft 3A (Naked Die amend per 5000) (with track changes + comments) for review.docx that details all changes.

Paragraph:

See attached 5010 Draft 3A (Naked Die amend per 5000) (with track changes + comments) for review.docx that details all changes.

Original wording:

See current ESCC5010 issue 2

Proposed wording:

Specification is amended throughout in order to implement changes applicable to “Naked Die Components” to make them consistent with the requirements applicable to procurement of active chips in ECSS-Q-ST-60-05C and Naked Die Components in ESCC5000 Draft 7C per DCR944.

All changes (both editorial and technical) made to ESCC 5010 issue 2 are identified and detailed in the DCR attachment: ESCC 5010 draft 3A.

Changes are summarised as follows (para numbers generally refer to ESCC5010 draft 3A):

1) General
Editorial changes necessary to make the requirements consistent with ESCC5000 draft 7C. In addition some other minor editorial changes are made as detailed below.

Note: Apart from item 3 below, there are no technical changes in this DCR that are applicable to the existing ‘Packaged components’; all technical changes apply due to the amendment of requirements for ‘Naked Die components’ in the Generic Specification.

2) Para. 4.1, 4.3.2, 4.3.3, 4.4, 5.2.2, 5.2.35.3.1, 5.3.3, 5.3.5, 6.1, 6.4, 6.4.1.1, 6.4.1.2, 6.4.2.1, 6.4.2.2, 7.1.1, 7.4, 8.1.1.1, 8.1.1.2, 8.1.2,8.5.18.5.28.18, 9.1, 9.1.2, 9.2, 9.5, 9.7, 9.9, 10, Charts F1A & F1B, F2, F3A, F3B, F4B
Requirements for Naked Die Components are amended; see attached ESCC5010 draft 3A for details.

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Notes on the amendments to Naked Die components requirements:

• Para 4.1, 7.5.1.1, 8.18, Chart F1B & F4B: 1000h LVT life test on each wafer lot for Naked Die Components is deleted (see below for justification).

• Para 4.3.2, 4.4, 9.1.2, 9.2, 9.5, 9.9: traceability to wafer is deleted (only wafer lot traceability is required) for Naked Die Components (based on ECSS-Q-ST-60-05C Para 8.3).

• Para 5.2, 9.5 & Chart F2: Testing at wafer/die level applicable to Naked Die IC components is specified based on the requirements in ECSS-Q-ST-60-05C Para 8.3.1. (& also ESCC5000 Draft 7C)

Note: The procurement lot based user LAT 1000h/125°C life test and post life wire pull/shear tests of ECSS-Q-ST-60-05C Para 8.3.3.2.4 are not included as requirements in ESCC5010 Draft 3A on the basis that:
a) As part of ESCC qualification and maintenance of qualification, a (2000h or) 1000h life test is performed on a sample of components every 24 months (i.e. on assembled Naked Die components from a Packaged Test Sublot)(the same as for qualified Packaged components).
b) Bond pull/shear tests are performed on each lot after assembly of the Packaged Test Sublot samples plus are also performed as part of ESCC qualification and maintenance of qualification on a sample of components that have either been Screened or subjected to a 1000h life test, every 24 months.
c) The user LAT requirements of ECSS-Q-ST-60-05C should be performed by the hybrid Manufacturer/customer using his own assembly processes (not the die Manufacturer).

• Para 5.2.2, 8.1.2.1, Chart F2: High & Low Temp electrical measurements are deleted during wafer screening for Naked Die Components.

• Para 5.3.1, 6.4.2, 8.5.1, 8.5.2, Chart F3B: Sampling and allowed failures requirements for testing of Naked Die components (tested on the assembled Packaged Test Sublot samples) is defined based on the user LAT sampling specified in ECSS-Q-ST-60-05C Table 8-2. The tests to be performed on the Naked Die Components (Charts F2 Special In-process Controls & F3B Screening Tests) are based on the procurement of active chips requirements in Para 8.3 of ECSS Q ST-60-05C i.e. bondability test & user LAT (& also ESCC5000 Draft 7C)
PDA0 and the related electrical measurements are deleted.

• Para 8.1.1.1, electrical measurements during wafer screening for Naked Die Component are made go-no-go (based on ECSS-Q-ST-60-05C Para 8.3).

• Para 10: an option to order the Packaged Test Sublot is added.

• Chart F4B: The sample size of the De-encapsulation subgroup (4 max components from the Endurance subgroup samples) is consistent with ECSS-Q-ST-60-05C Paras 8.3.2 and 8.3.3.2.4c 8 & 9.

• Chart F3B: new chart has been produced specifically for Naked Die components in order to make the different requirements applicable to Packaged components and Naked Die components clear.

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3) Para 2.1, 2.2 & 4.5: reference to ESCC 22600 for materials and finishes restrictions is added

Justification:

Currently ST, TESAT, as supported by ESA, wish to implement the possibility of Naked Die component qualification and procurement against ESCC5000 (similar to how it has already been implemented in ESCC5010). This DCR proposes to implement Naked Die IC components in the same way to how it is proposed for ESCC5000 (at ESA's request for consistency purposes).

Attachments:

5010_draft_3c_(die_implementation)_dcr994_attachment_2017_02_15.docx,
5010_draft_3a_(naked_die_amend_per_5000)(finalised)_for_review.docx,
5010_draft_3a_(naked_die_amend_per_5000)_(with_track_changes_+_comments)_for_review.docx

Modifications:

The contents of the original DCR994 are replaced in full by the following:

Specification is amended throughout in order to implement changes applicable to "Die Components" based on the requirements for Die Components implemented in ESCC5000 Draft 7E per DCR944 and ESCC9000 per DCR991 (with reference to the requirements for procurement of active chips in ECSS-Q-ST-60-05C Rev.1) and the current requirements for Naked Die Components in ESCC5010 issue 2.

All changes (both editorial and technical) made to ESCC 5010 issue 2 are identified (highlighted yellow) and detailed in the DCR attachment: ESCC 5010 draft 3C.
Note: Changes per DCR904 are also highlighted (green) in the DCR attachment ESCC 5010 draft 3C.

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Note:
For information & clarification purposes, the following requirements specified for die components in ECSS-Q-ST-60-05C are not applied to ESCC5010 Draft 3C per this DCR (i.e. the requirements of 5010 issue 2 are retained):

• Para 4.3.2, 4.4, 5.3.1, 9.1.2, 9.2, 9.5, 9.9, etc.: Traceability: traceability to each wafer (not just wafer lot) per 5010 issue 2 is retained as concluded by PSWG#77 (not in 5000 & 9000)

• Para 5.2.2(b), Chart F2: the High & Low Temp electrical measurements are retained during wafer screening for die components

• Para 5.3.1, 6.4.2, 8.5.1, 8.5.2 & Chart F3B: Sampling and allowed failures requirements for testing of Die Components (tested on the assembled Packaged Test Sublot samples) are not changed from ESCC5010 issue 2
i.e.: they are not defined based on the bondability & user LAT requirements specified in ECSS Q ST 60-05C Rev.1 Para 8.3 & Table 8-2.

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Changes are summarised as follows (para numbers refer to ESCC5010 draft 3C):

1) Para 2.1, 2.2 & 4.5: reference to ESCC 22600 for materials and finishes restrictions is added (ref to ECSS-Q-ST-70-02 is deleted).

2) Para 3: Definitions of ‘Die Components’ & ‘Packaged Components’ are specified.

3) Additions and modifications to existing requirements for die components & packaged components:
Spec title, Para 4.1, 4.1.5.1, 4.1.5.2, 4.3.3, 4.4, 4.5, 4.7, 5.2.2, 5.2.3, 5.3.4, 5.3.5, 6.1, 6.4, 6.4.1.1, 6.4.2.1, 6.4.2.2, 7.4, 8.1.1.1, 8.1.1.2, 8.1.2.1, 8.5.1, 8.9, 8.18, 9.1, 9.5, 10, Chart F1B, Chart F2, Charts F3A & F3B, Chart F4B :
Requirements for Die Components are amended; see attached ESCC5010 draft 3C for details.

Notes on specific amended requirements:

• Para 4.1, 7.4, 8.18, Chart F1B & F4B: 1000h LVT life test on each wafer lot for qualified Die Components is deleted (see below for justification).

Note: The procurement lot based user LAT 1000h/125°C life test and post life wire pull/shear tests of ECSS-Q-ST-60-05C Rev.1 Para 8.3.3.2.4 are not included as requirements in ESCC5010 Draft 3C on the basis that:
a) As part of ESCC qualification and maintenance of qualification, a (2000h or) 1000h life test is performed on a sample of components every 24 months (i.e. on assembled Naked Die components from a Packaged Test Sublot)(the same as for qualified Packaged components).
b) Bond pull/shear tests are performed on each lot after assembly of the Packaged Test Sublot samples plus are also performed as part of ESCC qualification and maintenance of qualification on a sample of components that have either been Screened or subjected to a 1000h life test, every 24 months.
c) The user LAT requirements of ECSS-Q-ST-60-05C Rev.1 should be performed by the hybrid Manufacturer/customer using his own assembly processes (not the die Manufacturer).
d) ESCC 5000 draft 7E per DCR944 does not include a 1000h LVT life test on each wafer lot for qualified Die Components.

• Para 5.2.2, 9.5 & Chart F2: Testing at wafer/die level applicable to Die Components is specified based on the requirements in ECSS-Q-ST-60-05C Rev.1 Para 8.3.1 (& ESCC5000 Draft 7E) but note that the High & Low Temp electrical measurements (Para 5.2.2(b)) are retained during wafer screening for die components.

• Para 6.4.1.1; Failures to high and low temperature electrical measurements do now count towards PDA3 (in order to be consistent with ESCC5000 & 9000 plus Para 6.4.2.2 of ESCC5010 for die components)

• Para 6.4.2.1, Optional high and low temp electrical measurements are added to Chart F3B to be consistent with ESCC5000 & ECSS-Q-ST-60-05C

• Para 10: an option to be able to deliver the Packaged Test Sublot samples is added.

• Chart F3A: Room Temperature Electrical Measurements prior to Burn-in 1 are retained but are made optional in order to be consistent with ESCC5000 & 9000 which do not require this test at this point during Screening Tests.

• Chart F3B: new chart has been produced specifically for Die Components in order to make the different requirements applicable to Packaged Components and Die Components clear.
Serialisation is moved to be before Room Temperature Electrical Measurements which is now read and record (not go-no-go)

An optional High and Low Temperatures Electrical Measurements is added before PDA0 (to be consistent with ESCC5000 & ECSS-Q-60-05C).

Justification:

The requirements for die components (and packaged components) already included in ESCC 5010 issue 2 are reviewed and amended to be consistent with the same requirements being implemented into ESCC 5000 & 9000 (by DCRs 944 & 991) except for specific requirements in line with conclusions made by the PSWG during their review of all 3 DCRs (944, 994, 991).

Approval signature:



Date signed:

2017-04-19