	ESC	C	DOCUMENT	CHANGE REQUEST						
DCR number	1264	Changes required for:	Qualification	Originator: Valerie Lepaludier						
Date: 2019/07/04 Date sent: 2019/04/26				Organisation: Atmel Microchip						
Status: IMPLE	MENTED									
Title:	INTEGRATED CIRCUITS, SILICON MONOLITHIC, CMOS, CELL-BASED ARRAY BASED ON TYPE									
Number:	9202/083	Issue:	2							
Other documents affected:										
Page:	Page:									
All For all modifications/corrections requested, see document attached.										
Paragraph:										
§1.4.2 §1.6 §1.7 § 2.3.1										
Original wording	g:									
 MQFP and MCGA packages Component type variant in §1.4.2 handling precautions : minimum path failure of 1000V in §1.6 physical dimensions and terminal identification in §1.7 Electrical table §2.3.1 										
Proposed wordi	ng:									
For all modifications requested, see document attached. 1. CQFP and CCGA packages 2. new variants from 75 to 114 3. §1.6 handling precautions : minimum path failure of 500V 4. see attached document for package drawing 5. see attached document for corrections										
Justification:										
 Change of wording: all references to MQFP and MCGA packages shall be replaced by CQFP and CCGA packages introduction of new die size and packages Correction new packages added Parameters not specified in the table, but read and recorded 										

	ESC	<u>;</u>		DC	CUMENT	CHANGE REQUEST		
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Date: 2019/07	7/04	Date sent: 2	2019/04/26	i		Organisation: Atmel Microchip		
Status: IMPLE	EMENTED							
Title:	INTEGRATED CIF	RCUITS, SILICO	ON MONOL	_ITHI	C, CMOS, CELL	-BASED ARRAY BASED ON TYPE		
Number:	9202/083		lssue:		2			
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Justification:								
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Attachments:								
modifs_9202083_issue_2.doc								
Modifications:								
Regarding 3-digit Component Type variant Numbers ESA has verified that they could accept three digit variants (ref email from Fernando Martinez dated 1rst July 2019) Therefore this open point is considered closed.								
Following further email correspondence with the manufacturer, the Technical writer has updated the Detail Spec. the applicable Low and High level Drift value limits to CMOS buffers and LVDS buffers (para. 2.4 Parameter Drift Values) should be different ie 10% of the absolute limits for IIL/IIH and this had been omitted from 9202/083 Draft 3A see attached Draft 3b								
Approval signature:								
Aluran Reux								

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2019-07-04