




DOCUMENT CHANGE REQUEST

DCR number		1606		Changes required for: General		Originator: Steve Thacker	
Date: 2024/01/12				Date sent: 2023/10/20		Organisation: ESCC Executive Secretariat	
Status: IMPLEMENTED							
Title:	TRANSISTORS, POWER, MOSFET, P-CHANNEL, RAD-HARD BASED ON TYPE STRH40P10						
Number:	5205/025		Issue:	8			
Other documents affected:							
Page:							
15							
Paragraph:							
2.12.2							
Original wording:							
Drain-to-Source Voltage, VDSS, Drift Value limit = +/-5%							
Proposed wording:							
Drain-to-Source Voltage, VDSS, Drift Value limit = +/-15%							
Justification:							
<p>This DCR is raised on behalf of Manufacturer STM.</p> <p>STM justification: The latest TID result showed a drift around 6.5% on wafers 8 inch on VDSS test. In order to accept the wafers 8 inch, the drift value +-5% by change to +-15% for VDSS.</p>							

Attachments:
escc5205025iss_draft_9a_in_review.docx
Modifications:
N/A
Approval signature:

Date signed:
2024-01-12