DOCUMENT CHANGE REQUEST

DCR number 1782	Changes required for: General	Originator: Steve Thacker
Date: 2026/10/20	Date sent: 2025/12/16	Organisation: ESCC Executive Secretariat
Status: IMPLEMENTED		

Title:	Integrated Circuits: Monolithic Microcircuits, Wire-Bonded, Plastic Encapsulated and Flip-Chip		
Number:	9030	Issue:	4

Other documents affected:

Page:

Various; see below & attached spec Mark-up

Paragraph:

Various; see below & attached spec Mark-up

Original wording:

As per spec issue 4 (& below)

Proposed wording:

Manufacturer ST proposes the following changes :
See attached spec mark-up Draft 5 for full details of all changes (changes are highlighted yellow for information):.

1) Change to Radiographic Inspection in Chart F3/Para. 8.10 (also Para. 5.3.8 & Chart F2):
For Flip Chip, X-ray shall be performed during Special In-Process Controls (Chart F2) after Add-on Components Attach, on a sample quantity as specified in the PID. In the event of a failure, the lot shall be tested 100%. The inspection shall be limited to the mounted add-on components used within the component.

(Note: in the current spec 9030 issue 4, Xray is a 100% test, performed on serialised components during Screening Chart F3 with no limitations on which part of the component is inspected)

2) Change the Data Point for final electrical measurements time margin for Power Burn-in Para 8.16 & Operating Life Para 8.22:
Final measurements of Parameter Drift Values / Intermediate and End-Point Electrical Measurements may be performed up to 96 hours after completion of Power Burn-In & Operating Life.

(Note: in the current spec 9030 issue 4:
For Power Burn-in: The final Data Point for Parameter Drift Values electrical measurements shall be performed within 24 hours of completion of Power Burn-in.
For Operating Life: The final Data Point for Intermediate and End-Point Electrical Measurements is within +/- 48 hours of the nominal 2000 hour test duration.)

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3) Change to the Lot Failure criteria of Chart F3/Para 6.4.1:
Lot Failure during 100% Testing (Para. 6.4.1) shall be checked for as follows:
If the number of components failed on the basis of the failure criteria specified in Para. 6.2.2, and 6.2.3 (during Room Temperature Electrical Measurements only) exceeds 5% (rounded upwards to the nearest whole number) of the components submitted to Power Burn-In of Chart F3, the lot shall be considered as failed.
i.e.
Any post-burn-in Screening failures during high & Low temperature electrical measurements shall not be counted when determining Lot Failure.

(Note: in the current spec 9030 issue 4: The Chart F3 Check for Lot Failure does take into account any post-burn-in Screening failures during high & Low Temperature electrical measurements)

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Several additional minor changes are proposed by ESCC-TW for consistency purposes; see attached spec mark-up Draft 5 Paras 5.3.1, 5.3.2, 5.3.3 & Charts F2, F4A, F4B (with blue highlights).

Justification:

This DCR is raised on behalf of Manufacturer STMicroelectronics.

ST has provided justifications for the various changes which are also included in the review margin of the attached spec mark-up Draft 5.

i.e.:
1) Change to Radiographic Inspection in Chart F3/Para. 8.10:
In ESCC9030, the X-ray inspection specified in Chart F3 after thermal cycling is affected by interference from the ball grid array, making defect detection challenging. Relocating the inspection to after the add-on component attachment improves the visibility and inspection of the add-on capacitor solder joints. Furthermore, the modified (i.e. reduced; & the same as for all other Chart F2 tests) sampling size enhances inspection efficiency without compromising defect detection, thereby preserving product quality.
This adjustment also aligns the inspection process with industry standards, such as MIL-PRF-38535, which does not require post-serialization X-ray inspection for Flip-Chip technology.
The additional option (in Chart F2 note 10) to permit Xray inspection to be performed at any subsequent point in Chart F2 or F3 provides flexibility for any Manufacturer.

2) Change the Data Point final electrical measurements time margin for Power Burn-in Para 8.16 & Operating Life Para 8.22:
The maximum allowed time to complete the electrical measurement after Chart F3 Burn-In or Chart F4B Operating Life (once the device has been removed) is not clearly specified and may be confused with the datapoint timing. According to MIL-STD-883 test methods 1005 and 1015, the maximum completion time permitted is 96 hours.

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3) Change to the Lot Failure criteria of Chart F3/Para 6.4:
Hot and cold failures observed after Burn-In do not indicate any reliability issues when both the electrical wafer sort and the pre Burn-In final test are performed at room temperature. The PDA calculation in MIL-PRF-38535 does not account for post Burn-In hot and cold failures.
To include this post Burn-In hot and cold failures in the PDA calculation, it is necessary to add corresponding pre Burn-In hot and cold tests, to identify parts to be removed prior to Burn-In. This addition increases the number of touchdowns and may potentially impact the overall yield.

Attachments:

escc9030iss5_draft_b_in_review.docx

Modifications:

o DCR item 1) Radiographic Change for Flip-Chip: is rejected; Ref PSWG#111 item 3.1.1
o DCR item 2) Post test Data Point for Burn-in & Op. Life to be +96hours: Accepted
o DCR item 3) Screening PDA Lot Failure criteria to exclude Hi & Lo Temp failures: is rejected; Ref PSWG#111 item 3.1.1

Approval signature:



Date signed:

2026-10-20