DOCUMENT CHANGE REQUEST

DCR number 206	Changes required for: General	Originator: S Thacker (pp Christian
Date: 2005/10/25	Date sent: 2005/10/25	Organisation: ESA/ESTEC
Status: IMPLEMENTED		

Title:	IC Silicon Monolithic, 32-BIT SPARC Embedded Processor, based on Type TSC695F		
Number:	9512/003	Issue:	1

Other documents affected:

Page:

Page 8 Para 1.8 Functional Diagram
Page 16, 19, 20, 22, Para1.10 Timing Diagrams
Page 31 Para 2.3.1 Room Temperature Electrical Measurements (Input Capacitance)
Page 34 Para 2.3.3 Notes to Electrical Measurements Table

Paragraph:

Page 8 Para 1.8 Functional Diagram
Page 16, 19, 20, 22, Para1.10 Timing Diagrams
Page 31 Para 2.3.1 Room Temperature Electrical Measurements (Input Capacitance)
Page 34 Para 2.3.3 Notes to Electrical Measurements Table

Original wording:

Proposed wording:

DCR raise on behalf of the Manufacturer Atmel (Christian Ferré: Atmel Aerospace Quality Operations & Chief Inspector)

See attachment for details.

1) Para 1.8 Functional diagram - replace diagrams with amended diagram

2) 3) 4) 5) Para 1.10 Timing diagrams - replace several specific diagrams by corrected versions. Details are as shown in the attachment

6) Para 2.3.1 Room Temperature Electrical Measurements - Correct maximum limit for Input Capacitance (CI) to be 7pf (was 10pf)

7) Para 2.3.3 Notes to Electrical Measurements Table
Add new note to introduce internal timing parameters, T69 & T70 which are used to facilitate producing timing results related to CLK2 instead of SYSCLK. See attachment for details

Justification:

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1), 2), 3), 4), 5), 6), Correction of errors in first issue of the spec

7) The additional note serves to explain T69 & T70, which will be recorded in the data documentation produced for this device, but are parameters without a specified min or max limit and not required to be tested for standard procurement. T69 & T70 were introduced into Atmel's process to satisfy a specific customers request to have the Timing results referenced to CLK2 (instead of SYSCKL as is the standard). The results for T69 & T70 are used together with the standard Timing results to calculate the timings related to CLK2.

Attachments:

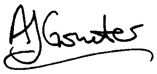
Attachment_to_DCR_on_9512003.doc, null

Modifications:

DCR is approved with the following amendment to point 7):

The original wording for point 7 is deleted and replaced with the folowing:
Page 28 Para. 1.10 Instruction Set and Timing diagrams
Add new timing diagra as attached with title:
SYSCLK to CLK2 Timing
plus note:
"Timings specified with respect to SYSCLK can be specified with respect to CLK2 by means of T69 and T70."

Approval signature:



Date signed:

2005-10-25