DOCUMENT CHANGE REQUEST

DCR number 259	Changes required for: General	Originator: Steve Thacker
Date: 2006/06/07	Date sent: 2006/06/07	Organisation: ESA/ESTEC
Status: IMPLEMENTED		

Title:	HCMOS 8 Channel Multiplexer Register with 3-State Latches, based on type 54HC356		
Number:	9306/055	Issue:	1

Other documents affected:

Page:

Page 11 & 12, figure 3(b) Truth Table

Paragraph:

Page 11 & 12, figure 3(b) Truth Table

Original wording:

Proposed wording:

See attached proposed Truth Table & notes for details.

Main truth table rows are reordered based on function plus a "Function" column is added. The CLK column is amended to include all possible conditions (i.e. adding CLK = H & CLK = L)

The 2 mini-truth Tables for internal elements of the device are deleted ("Internal Latch" & "Internal Latch (Flip-Flop)"

Notes 3, 4, 5 & 6 are deleted and replaced by new notes 3 & 4 :

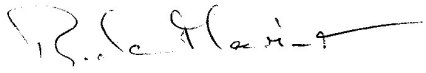
Note 3. D0n to D7n = The level of D0 to D7, respectively, latched into the data latch during the previous Transition Low to High on the CLK.

Note 4. S0 to S2 select latch contents when SC-bar = L. (When SC-bar = H, S0 to S2 inputs are disabled and the select latch contents are unaffected).

Justification:

The original details specifying the functionality are unclear, inconsistent and incomplete.
The 2 mini-Truth Tables are unclear without an explanation of how the device internal logic circuit is structured and unnecessary for specification of the functionality of the component.
Some terms are undefined in terms of the component itself e.g. D0n-bar to D7n-bar; ST; D; Q; Q-bar.

The amended truth table with its Function column and new notes fully specifies the functionality.

Attachments:
DCR_attachment_for_9306055.pdf, null
Modifications:
N/A
Approval signature:

Date signed:
2006-06-07

1.9 PIN ASSIGNMENT

Pin	Function	Pin	Function
1	D7 Input (Data)	11	$\overline{SC}$ Input (Select Control)
2	D6 Input (Data)	12	S2 Input (Select)
3	D5 Input (Data)	13	S1 Input (Select)
4	D4 Input (Data)	14	S0 Input (Select)
5	D3 Input (Data)	15	$\overline{G1}$ Input (Output Enable)
6	D2 Input (Data)	16	$\overline{G2}$ Input (Output Enable)
7	D1 Input (Data)	17	G3 Input (Output Enable)
8	D0 Input (Data)	18	W Output
9	CLK Input (Clock)	19	Y Output
10	V_{SS}	20	V_{DD}

1.10 TRUTH TABLE

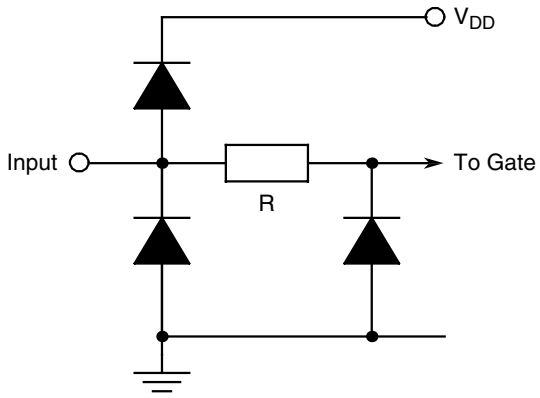
1. Logic Level Definitions: L = Low Level, H = High Level, X = Irrelevant, Z = High Impedance.
2. ↑ = Transition Low to High, ↓ = Transition High to Low.
3. D0n to D7n = The level of D0 to D7, respectively, latched into the data latch during the previous Transition Low to High on the CLK.
4. S0 to S2 select latch contents when $\overline{SC}$ = L. (When $\overline{SC}$ = H S0 to S2 inputs are disabled and the select latch contents are unaffected).

INPUTS							OUTPUTS (Note 3)		FUNCTION
SELECT (NOTE 4)			CLK	OUTPUT ENABLE					
S2	S1	S0		$\overline{G1}$	$\overline{G2}$	G3	W	Y	
X	X	X	X	H	X	X	Z	Z	OUTPUTS DISABLED
X	X	X	X	X	H	X	Z	Z	
X	X	X	X	X	X	L	Z	Z	
L	L	L	↑	L	L	H	$\overline{D0}$	D0	DATA (D0 to D7) IS CLOCKED INTO DATA LATCH
L	L	H	↑	L	L	H	$\overline{D1}$	D1	
L	H	L	↑	L	L	H	$\overline{D2}$	D2	
L	H	H	↑	L	L	H	$\overline{D3}$	D3	
H	L	L	↑	L	L	H	$\overline{D4}$	D4	
H	L	H	↑	L	L	H	$\overline{D5}$	D5	
H	H	L	↑	L	L	H	$\overline{D6}$	D6	
H	H	H	↑	L	L	H	$\overline{D7}$	D7	

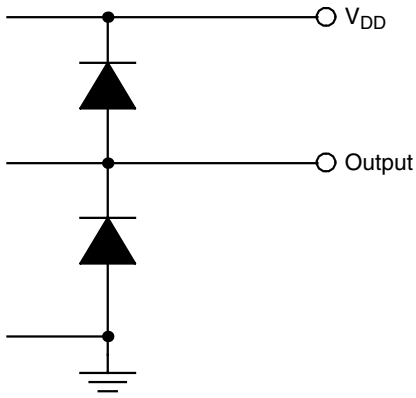
INPUTS							OUTPUTS (Note 3)		FUNCTION
SELECT (NOTE 4)			CLK	OUTPUT ENABLE					
S2	S1	S0		$\overline{G1}$	$\overline{G2}$	G3	W	Y	
L	L	L	H, L, ↓	L	L	H	$\overline{D0n}$	D0n	OUTPUTS DO NOT CHANGE STATES
L	L	H	H, L, ↓	L	L	H	$\overline{D1n}$	D1n	
L	H	L	H, L, ↓	L	L	H	$\overline{D2n}$	D2n	
L	H	H	H, L, ↓	L	L	H	$\overline{D3n}$	D3n	
H	L	L	H, L, ↓	L	L	H	$\overline{D4n}$	D4n	
H	L	H	H, L, ↓	L	L	H	$\overline{D5n}$	D5n	
H	H	L	H, L, ↓	L	L	H	$\overline{D6n}$	D6n	
H	H	H	H, L, ↓	L	L	H	$\overline{D7n}$	D7n	

1.11 PROTECTION NETWORKS

INPUT PROTECTION



OUTPUT PROTECTION



2. REQUIREMENTS

2.1 GENERAL

The complete requirements for procurement of the components specified herein are as stated in this specification and the ESCC Generic Specification. Permitted deviations from the Generic Specification, applicable to this specification only, are listed below.

Permitted deviations from the Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESCC requirement and do not affect the component's reliability, are listed in the appendices attached to this specification.