



DOCUMENT CHANGE REQUEST

DCR number 253 Changes required for: General

Date: 2006/04/04

Date sent: 2006/04/04

Originator: S JEFFERY

Organisation:

Status: IMPLEMENTED

Title: Transistors Low Power PNP, based on type 2N5401

Number: 5202/014

Issue: 1

Other documents affected:

Page:

Total Re-write

Paragraph:

Total Re-write

Original wording:

Proposed wording:

Total reformat of this Detail Specification (under Generic Specification No. 5000) as part of the ongoing conversion to the ESCC format. See below for summary of changes and attached Issue 2 Draft A of the Specification.

Note: known support for active procurement against this specification includes the following manufacturers:

STMICROELECTRONICS/F (ESCC QPL listed with qualified Variants 01, 02, 04 and 05)

Summary of changes to the current format, layout and content is as follows:

1. Rewording and restructure of various sections and paragraphs of the specification plus other editorial changes based on the layout and editorial content of other Detail Specifications already converted to ESCC format (e.g. changes described in DCR No. 203).
2. Deletion of any redundant paragraphs and information, e.g.: Mechanical Requirements.
3. Para. 1.7 High Temperature Test Precautions requirements moved to be a note in the Maximum Ratings table.
4. Deletion of obsolete lead finish D7 / Variant 03 from the available range (not supported by STM).
5. Maximum Ratings table: maximum rating for VEBO corrected from .6.0 to .5.
6. Figure 1 Parameter Derating Information moved to be a note in the Maximum Ratings table.
7. Para. 4.3.2 Weight requirements moved to Component Type Variants table.
8. Figure 2 re-named .Physical Dimensions and Terminal Identification.; Figure 2(a) amended to reflect the TO-18 package currently supplied. Notes revised, including addition of a terminal identification note.
9. Para. 4.4.1 Case requirements for Variants 01 and 02 corrected to reflect a TO-18 metal can.
10. Para. 4.4.2 Lead Material and Finish replaced by a reference to the Component Type Variants Para.
11. Delete requirement for marking of the test level letter from ESCC component number as per latest ESCC No. 21700.
12. Figure 3 (Functional Diagram): Note added to clarify that the lids of the CCP packaged devices are not connected to



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any terminal.

13. Table 2, Characteristic .D.C. Forward Current Transfer Ratio. has been changed to .Forward-Current Transfer Ratio..

14. Table 2, Characteristic .A.C. Forward Current Transfer Ratio. has been changed to .Small-Signal Current Gain..

15. Table 2, Characteristic .Collector-Base Capacitance. has been changed to .Output Capacitance. and its Symbol has been changed from Ccbo to Cobo.

16. Table 2: Replace LTPD7 sampling for AC parameters tests (designated by .Note 2.) with an equivalent fixed sample of 32 components with 0 failures (or 100%).

17. Table 3 (High and Low Temperature Electrical Measurements), Test Conditions: standard tolerances have been added to the specified Tamb.

18. Tables 3, 4 and 6, Characteristic .D.C. Forward Current Transfer Ratio 2. has been changed to .Forward-Current Transfer Ratio 2..

19. Table 3: 100% inspection has been replaced by a sample of 5 components with 0 failures, or 100%, in line with the new Generic 5000 Issue 3.

20. Table 4: Absolute limits have been added for information.

21. Tables 2, 3 and 4 . Test Conditions column: addition of Test, or Bias, conditions for referenced MIL-STD-750 Test Methods as and where applicable.

22. Conditions for High Temperature Reverse Bias Burn-in: standard tolerance has been added to the specified Tamb. Duration amended to 48 hours minimum, in line with new Generic 5000 and MIL specifications.

23. Appendix A for STM: Para. 4.2.2 corrected to delete reference to .Para. 9.12. as this inspection is a specific in-process requirement to check die attachment per the STM procedure. The STM procedure is updated from 0011828 to 0076637.

24. Appendix A for STM: Addition of note about wafer level pilot lot testing in that AC characteristics during screening may be considered guaranteed but not tested. Note STM is an ESCC QPL listed manufacturer and this device is ESCC qualified; accordingly there is an ESCC approved PID for this device. This amendment is considered technically acceptable on this basis.

Justification:

(see also change details for each item above)

1. Part of the ongoing activity of conversion of cover-sheeted ESA/SCC specifications to the ESCC format.

2. To make the format and presentation consistent with the various other ESCC Detail Specifications already converted to ESCC format.


3. To make the content consistent with ESCC Generic Specification No. 5000 Issue 3.

4. To incorporate specific deviations requested by manufacturer STM within Appendix A which are considered technically acceptable (based on ESCC approved PID for this and other ESCC qualified components manufactured by STM).

5. To update the manufacturer.s current product availability.

6. To make corrections to technical errors in the previous issue.

7. Standardisation of the TO-18 and CCP packages in all applicable ESCC detail specs.

Attachments:
5202014_Issue_2_-_Draft_A.pdf, null
Modifications:
N/A
Approval signature:

Date signed:
2006-04-04



Pages 1 to 14

TRANSISTORS, LOW POWER, PNP

BASED ON TYPE 2N5401

ESCC Detail Specification No. 5202/014

Issue 2 - Draft A	March 2006
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(Refer to <https://escies.org> for ESCC DCR content)

DCR No.	CHANGE DESCRIPTION
187, TBD	Specification up issued to incorporate editorial and technical changes per DCR.

TABLE OF CONTENTS

<u>1.</u>	<u>GENERAL</u>	<u>5</u>
1.1	Scope	5
1.2	Applicable Documents	5
1.3	Terms, Definitions, Abbreviations, Symbols and Units	5
1.4	The ESCC Component Number and Component Type Variants	5
1.4.1	The ESCC Component Number	5
1.4.2	Component Type Variants	5
1.5	Maximum Ratings	5
1.6	Physical Dimensions and Terminal Identification	7
1.6.1	Metal Can Package (TO-18) - 3 lead	7
1.6.2	Chip Carrier Package (CCP) - 3 terminal	8
1.7	Functional Diagram	9
1.8	Materials and Finishes	9
<u>2.</u>	<u>REQUIREMENTS</u>	<u>9</u>
2.1	General	9
2.1.1	Deviations from the Generic Specification	9
2.2	Marking	10
2.3	Terminal Strength	10
2.4	Electrical Measurements at Room, High and Low Temperatures	10
2.4.1	Room Temperature Electrical Measurements	10
2.4.2	High and Low Temperatures Electrical Measurements	12
2.5	Parameter Drift Values	12
2.6	Intermediate and End-Point Electrical Measurements	13
2.7	High Temperature Reverse Bias Burn-in Conditions	13
2.8	Power Burn-in Conditions	13
2.9	Operating Life Conditions	13
APPENDIX 'A'		14

1. GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics and test and inspection data for the component type variants and/or the range of components specified below. It supplements the requirements of, and shall be read in conjunction with, the ESCC Generic Specification listed under Applicable Documents.

1.2 APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:

- (a) ESCC Generic Specification No. 5000
- (b) MIL-STD-750, Test Methods and Procedures for Semiconductor Devices

1.3 TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESCC Basic Specification No. 21300 shall apply.

1.4 THE ESCC COMPONENT NUMBER AND COMPONENT TYPE VARIANTS

1.4.1 The ESCC Component Number

The ESCC Component Number shall be constituted as follows:

Example: 520201401

- Detail Specification Reference: 5202014
- Component Type Variant Number: 01 (as required)

1.4.2 Component Type Variants

The component type variants applicable to this specification are as follows:

Variant Number	Based on Type	Case	Lead/Terminal Material and/or Finish	Weight max g
01	2N5401	TO-18	D2	0.4
02	2N5401	TO-18	D3 or D4	0.4
04	2N5401	CCP	2	0.06
05	2N5401	CCP	4	0.06

The lead/terminal material and/or finish shall be in accordance with the requirements of ESCC Basic Specification No. 23500.

1.5 MAXIMUM RATINGS

The maximum ratings shall not be exceeded at any time during use or storage.

Maximum ratings shall only be exceeded during testing to the extent specified in this specification and when stipulated in Test Methods and Procedures of the ESCC Generic Specification.

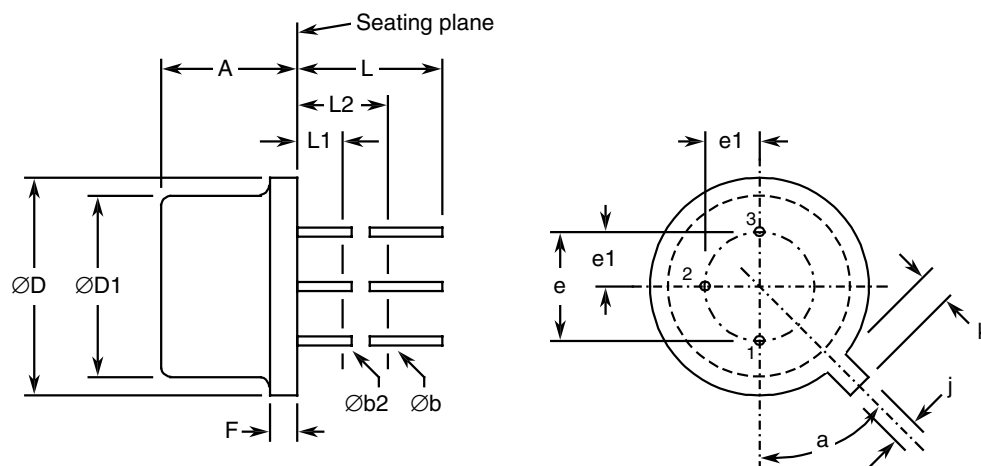
Characteristics	Symbols	Maximum Ratings	Unit	Remarks
Collector-Base Voltage	V_{CBO}	-160	V	Over entire operating temperature range
Collector-Emitter Voltage	V_{CEO}	-150	V	
Emitter-Base Voltage	V_{EBO}	-5	V	
Collector Current For TO-18 For CCP	I_C	-600 -500	mA	Continuous
Power Dissipation For TO-18 and CCP For CCP For TO-18	P_{tot1}	0.36	W	At $T_{amb} \leq +25^{\circ}C$ Note 1
	P_{tot2}	0.58 (Note 2)	W	
	P_{tot3}	1.2	W	At $T_{case} \leq +25^{\circ}C$ Note 1
Operating Temperature Range	T_{op}	-65 to +200	$^{\circ}C$	Note 3
Storage Temperature Range	T_{stg}	-65 to +200	$^{\circ}C$	Note 3
Soldering Temperature For TO-18 For CCP	T_{sol}	+260 +245	$^{\circ}C$	Note 4 Note 5

NOTES:

- For T_{amb} or $T_{case} > +25^{\circ}C$, derate linearly to 0W at $+200^{\circ}C$.
- When mounted on an 8 x 10 x 0.6mm ceramic substrate.
- For Variants with tin-lead plating or hot solder dip lead finish all testing performed at $T_{amb} > +125^{\circ}C$ shall be carried out in a 100% inert atmosphere.
- Duration 10 seconds maximum at a distance of not less than 1.5mm from the device body and the same lead shall not be resoldered until 3 minutes have elapsed.
- Duration 5 seconds maximum and the same terminal shall not be resoldered until 3 minutes have elapsed.

1.6 PHYSICAL DIMENSIONS AND TERMINAL IDENTIFICATION

1.6.1 Metal Can Package (TO-18) - 3 lead



Symbols	Dimensions mm		Notes
	Min	Max	
A	4.32	5.33	
Øb	0.406	0.533	2, 3
Øb2	0.406	0.483	2, 3
ØD	5.31	5.84	
ØD1	4.52	4.95	
e	2.54 BSC		4
e1	1.27 BSC		4
F	-	0.762	
j	0.914	1.17	
k	0.711	1.22	5
L	12.7	-	2
L1	-	1.27	3
L2	6.35	-	3
a	45° BSC		1, 4, 6

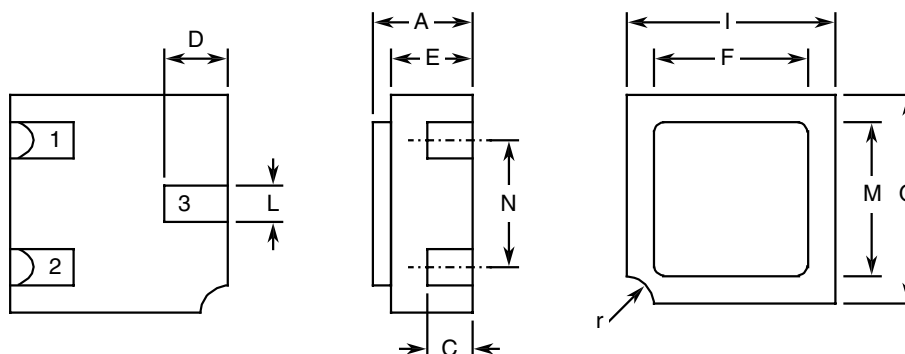
NOTES:

- Terminal identification is specified by reference to the tab position where lead 1 = emitter, lead 2 = base, lead 3 = collector.
- Applies to all leads.
- Øb2 applies between L1 and L2. Øb applies between L2 and 12.7mm from the seating plane. Diameter is uncontrolled within L1 and beyond 12.7mm from the seating plane.
- Leads having maximum diameter 0.483mm measured in the gauging plane 1.37(+0.025,-0)mm

below the seating plane of the device shall be within 0.178mm of their true position relative to a maximum-width-tab.

5. Measured from the maximum diameter of the actual device.
6. Tab centreline.

1.6.2 Chip Carrier Package (CCP) - 3 terminal

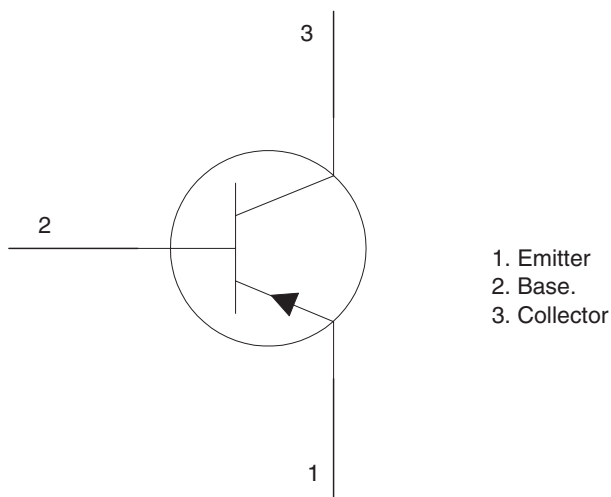


Symbols	Dimensions mm		Notes
	Min	Max	
A	1.15	1.5	
C	0.45	0.56	2
D	0.6	0.91	2
E	0.91	1.12	
F	1.9	2.15	
G	2.9	3.25	
I	2.4	2.85	
L	0.4	0.6	2
M	2.4	2.65	
N	1.8	2	
r	0.3 TYPICAL		1

NOTES:

1. Terminal identification is specified by reference to the corner notch position where terminal 1 = emitter, terminal 2 = base, terminal 3 = collector.
2. Applies to all terminals.

1.7 FUNCTIONAL DIAGRAM



NOTES:

1. For TO-18, the collector is internally connected to the case.
2. For CCP the lid is not connected to any terminal

1.8 MATERIALS AND FINISHES

Materials and finishes shall be as follows:

- a) Case
For the metal can package the case shall be hermetically sealed and have a metal body with hard glass seals.

For the chip carrier package the case shall be hermetically sealed and have a ceramic body with a Kovar lid.
- b) Leads/Terminals
As specified in Component Type Variants.

2. REQUIREMENTS

2.1 GENERAL

The complete requirements for procurement of the components specified herein are as stated in this specification and the ESCC Generic Specification. Permitted deviations from the Generic Specification, applicable to this specification only, are listed below.

Permitted deviations from the Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESCC requirement and do not affect the component's reliability, are listed in the appendices attached to this specification.

2.1.1 Deviations from the Generic Specification

None.

2.2 MARKING

The marking shall be in accordance with the requirements of ESCC Basic Specification No. 21700 and as follows.

The information to be marked on the component shall be:

- (a) The ESCC qualified components symbol (for ESCC qualified components only).
- (b) The ESCC Component Number.
- (c) Traceability information.

2.3 TERMINAL STRENGTH

The test conditions for terminal strength, tested as specified in the ESCC Generic Specification, shall be as follows:

For TO-18, Test Condition: E, lead fatigue.

2.4 ELECTRICAL MEASUREMENTS AT ROOM, HIGH AND LOW TEMPERATURES

Electrical measurements shall be performed at room, high and low temperatures.

2.4.1 Room Temperature Electrical Measurements

The measurements shall be performed at $T_{\text{amb}} = +22 \pm 3^{\circ}\text{C}$.

Characteristics	Symbols	MIL-STD-750 Test Method	Test Conditions	Limits		Units
				Min	Max	
Collector-Base Breakdown Voltage	$V_{(BR)CBO}$	3001	$I_C = -100\mu A$ Bias condition D	-160	-	V
Collector-Emitter Breakdown Voltage	$V_{(BR)CEO}$	3011	$I_C = -1mA$ Bias condition D Note 1	-150	-	V
Emitter-Base Breakdown Voltage	$V_{(BR)EBO}$	3026	$I_E = -10\mu A$ Bias condition D	-5	-	V
Collector-Base Cut-off Current	I_{CBO}	3036	$V_{CB} = -120V$ Bias condition D	-	-50	nA
Emitter-Base Cut-off Current	I_{EBO}	3061	$V_{EB} = -3V$ Bias condition D	-	-50	nA
Collector-Emitter Saturation Voltage	$V_{CE(sat)1}$	3071	$I_C = -10mA$ $I_B = -1mA$ Note 1	-	-200	mV
	$V_{CE(sat)2}$	3071	$I_C = -50mA$ $I_B = -5mA$ Note 1	-	-500	mV
Base-Emitter Saturation Voltage	$V_{BE(sat)1}$	3066	$I_C = -10mA$ $I_B = -1mA$ Test condition A Note 1	-	-1	V
	$V_{BE(sat)2}$	3066	$I_C = -50mA$ $I_B = -5mA$ Test condition A Note 1	-	-1	V
Forward-Current Transfer Ratio	h_{FE1}	3076	$V_{CE} = -5V$; $I_C = -1mA$	50	-	-
	h_{FE2}	3076	$V_{CE} = -5V$; $I_C = -10mA$ Note 1	60	240	-
	h_{FE3}	3076	$V_{CE} = -5V$; $I_C = -50mA$ Note 1	60	-	-
Small-Signal Current Gain	h_{fe}	3206	$V_{CE} = -10V$; $I_C = -10mA$ $f = 10kHz$ Note 2	5	-	-
Output Capacitance	C_{obo}	3236	$V_{CB} = -10V$, $I_E = 0A$ $f = 1MHz$ Note 2	-	6	pF

NOTES:

1. Pulse measurement: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$
2. For AC characteristics read and record measurements shall be performed on a sample of 32

components with 0 failures allowed. Alternatively a 100% inspection may be performed.

2.4.2 High and Low Temperatures Electrical Measurements

Characteristics	Symbols	MIL-STD-750 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Collector-Base Cut-off Current	I_{CBO}	3036	$T_{amb}=+150 (+0 -5)^{\circ}C$ $V_{CB}=-120V$ Bias condition D	-	-50	μA
Forward-Current Transfer Ratio 2	h_{FE2}	3076	$T_{amb}=55(+5-0)^{\circ}C$ $V_{CE}=-5V$; $I_C =-10mA$ Note 2	20	-	-

NOTES:

- Read and record measurements shall be performed on a sample of 5 components with 0 failures allowed. Alternatively a 100% inspection may be performed.
- Pulse measurement: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

2.5 PARAMETER DRIFT VALUES

Unless otherwise specified, the measurements shall be performed at $T_{amb}=+22 \pm 3^{\circ}C$.

The test methods and test conditions shall be as per the corresponding test defined in Room Temperature Electrical Measurements.

The drift values (Δ) shall not be exceeded for each characteristic specified. The corresponding absolute limit values for each characteristic shall not be exceeded.

Characteristics	Symbols	Limits			Units
		Drift Value Δ	Absolute		
			Min	Max	
Collector-Base Cut-off Current	I _{CBO}	±5 or (1) ±100%	-	-50	nA
Collector-Emitter Saturation Voltage 2	V _{CE(sat)2}	±30 or (1) ±15%	-	-500	mV
Forward-Current Transfer Ratio 2	h _{FE2}	±15%	60	240	-

NOTES:

- Whichever is the greater referred to initial value.

2.6 INTERMEDIATE AND END-POINT ELECTRICAL MEASUREMENTS

Unless otherwise specified, the measurements shall be performed at $T_{amb}=+22 \pm 3^{\circ}C$.

The test methods and test conditions shall be as per the corresponding test defined in Room Temperature Electrical Measurements.

The limit values for each characteristic shall not be exceeded.

Characteristics	Symbols	Limits		Units
		Min	Max	
Collector-Base Cut-off Current	I_{CBO}	-	-50	nA
Collector-Emitter Saturation Voltage 2	$V_{CE(sat)2}$	-	-500	mV
Forward-Current Transfer Ratio 2	h_{FE2}	60	240	-

2.7 HIGH TEMPERATURE REVERSE BIAS BURN-IN CONDITIONS

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	T_{amb}	+150 (+0 -5)	°C
Collector-Base Voltage	V_{CB}	-128	V
Duration	t	48 minimum	Hours

2.8 POWER BURN-IN CONDITIONS

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	T_{amb}	+25 to +50	°C
Power Dissipation	P_{tot}	As per Maximum Ratings P_{tot1} derated at the chosen T_{amb}	W
Collector-Base Voltage	V_{CB}	-90	V

2.9 OPERATING LIFE CONDITIONS

The conditions shall be as specified for Power Burn-in.

APPENDIX 'A'**AGREED DEVIATIONS FOR STMICROELECTRONICS (F)**

ITEMS AFFECTED	DESCRIPTION OF DEVIATIONS
Deviations from Production Control-Chart F2	Special In-process Control Internal Visual Inspection. For CCP packages the criteria specified for voids in the fillet and minimum die mounting material around the visible die perimeter for die mounting defects may be omitted providing that a radiographic inspection to verify the die-attach process is performed on a sample basis in accordance with STMicroelectronics procedure 0076637.
Deviations from Room Temperature Electrical Measurements	All AC characteristics (Room Temperature Electrical Measurement Note 2) may be considered guaranteed but not tested if successful pilot lot testing has been performed on the wafer lot which includes AC characteristic measurements per the Detail Specification. A summary of the pilot lot testing shall be provided if required by the Purchase Order.
Deviations from High and Low Temperatures Electrical Measurements	All characteristics specified may be considered guaranteed but not tested if successful pilot lot testing has been performed on the wafer lot which includes characteristic measurements at high and low temperatures per the Detail Specification. A summary of the pilot lot testing shall be provided if required by the Purchase Order.