DOCUMENT CHANGE REQUEST

DCR number 321	Changes required for: N/A	Originator: Christian Ferre
Date: 2007/02/21	Date sent: 2007/02/21	Organisation: CNES
Status: IMPLEMENTED		

Title:	Integrated Circuits Silicon Monolithic CMOS Gate Array/Embedded Array , based on Type MH1RT		
Number:	9202/076	Issue:	1

Other documents affected:

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Original wording:

Proposed wording:

see attached file

Justification:

see attached file

Attachments:

DCR321att2.pdf, modifs_9202076_issue_1.doc, DCR321att9202076.pdf, DCR321att.pdf, null

Modifications:

The following amendments and additional changes shall apply to this DCR:
See attached mark-up for details.

Para 1.8 (ref. "DCR321 Change #1" replaced as follows)
Add note 1 to para 1.8 Functional Diagram:
"1. For all packages the lid is internally connected to the ground terminal as specified in the ASIC Sheet."

Para 1.4.1 (ref. "DCR321 Change #2" replaced as follows)
Amend the Manufacturer Specific ASIC Identification to be a 3 character code where:
"XYZ: Individual 3 character code allocated by the Manufacturer to a specific ASIC design".
(previously the 1st letter of the code was meant to indicate the Manufacturer)

Para 1.5 (ref. "DCR321 Change #3" replaced as follows)
Maximum rating for "Supply Current" shall be "See ASIC Sheet" (was "+/-60mA")
New characteristic "Input current" added with max rating "+/-60mA" and note "Each Input Pin"

Para 1.5 (ref. "DCR321 Change #4" replaced as follows)
Delete the various package references from the Thermal Resistance characteristic column ("MQFP-F196" etc) and replace the max rating values by "See ASIC Sheet". "Note 3" is deleted for Thermal Resistance.
Additional Justification: Thermal Resistance value is variable depending on package and circuit function. Accordingly the value should be specified in the applicable ASIC Sheet.

Para 2.3.1 (ref. "DCR321 Change #6" amended as follows)
Characteristic titles and symbols are amended to be consistent with other ESCC specifications i.e.:
"Positive Trigger Threshold Voltage"; "VTP" (instead of "Threshold Schmitt Trigger Input Voltage"; "VT+")
"Negative Trigger Threshold Voltage"; "VTN" (instead of "Threshold Schmitt Trigger Input Voltage"; "VT-")
"Hysteresis Voltage"; "VH" (instead of "Hysteresis"; "Delta VT")

The limits for para 2.3.1.1 for VIL & VIH are "690mVmax" & "1.89Vmin" respectively (instead of "0.3VDD" & "0.7VDD")

The limit in para 2.3.1.2, 2.3.1.3 & 2.3.1.4 for VIL is "800mVmax" (instead of "0.8Vmax")
Additional Justification: For clarification & consistency purposes.

Para 2.3.2 (ref. "DCR321 Change #7" amended as follows)
Notes "8" & "9" are renumbered as "6" & "7" (also in para 2.3.1.4)

Para 2.3.1 & 2.4 (editorial change only)
Amend "Low Level Output Voltage" value in tables & notes to be "400mVmax" (instead of "0.4Vmax")
Additional Justification: For consistency purposes.

Approval signature:

Date signed:
2007-02-21

Modifications of 9202/076 Issue 1 – DCR # 321

1. Change #1 :

For MH1RT ASIC family, Atmel proposes its packages **with lid connected to ground**.

Reason of change :
The note 'lid is connected to ground' is not specified in the detail specification 9202/076.

Description of change:
In §1.7.1 MQFPF196, §1.7.2 MQFPF256, §1.7.3 MQFPT352, §1.7.4 MCGA349 and §1.7.5 MCGA472, Add note 3. lid is connected to ground.

2. Change #2 :

§1.4.1 ESCC component number
'XYZ' has to stay a code with 3 digits allocated to Atmel.

Reason of change :
In 9202/076, 'X' is a single letter allocated by ESCC executive, and only 2 digits ('YZ') are allocated to Atmel to identify the ASIC.
Atmel needs 3 digits to identify its ASIC : 'X' indicates the country, and 'YZ' is a chrono. For instance 'FPK' is Atmel identification for 'HBRISC2'.

Description of change:
replace

- *Manufacturer Specific ASIC Identification: XYZ (as applicable) where:*

X : Single letter allocated by the ESCC Executive to the manufacturer and each complete code registered with the ESCC Executive Secretariat.
YZ : Individual 2 character code allocated by the Manufacturer to a specific ASIC design.
By:

- Manufacturer Specific ASIC Identification: XYZ.

3. Change #3 :

§1.5. Maximum ratings : Clarification expected

Reason of change :
To avoid confusion between supply pin and other input pins

Description of change:
Add in line 'supply current', row 'remarks': 'Each supply pin'

4. Change #4 :

§1.5. Maximum ratings : Mismatch about notes

Reason of change :
Note 3 is not suitable for 'thermal resistance'

Note 4 is not complete.

Description of change:
- Add note 3
3. Rth(j-c) is given for the smallest available matrix which corresponds to the worst case (highest junction-to-case resistance).

- Rename Note 3 in Note 4 (suitable for 'soldering temperature'), add note 4 is applicable for MQFP packages.

5. Change #5 :

§1.7.4 MCGA349
'A' is missing in bottom view description.

6. Change #6 :

§2.3.1. Room temperature electrical measurements : VIL, VIH, VT

Reason of change :
Information is missing to be homogeneous with Atmel MH1RT datasheet.

Description of change:
§2.3.1.1 (VDD=2.5V)
Add:

Low level input voltage	VIL	-	CMOS buffers VDD=2.3V		0.3 VDD	V
High level input voltage	VIH	-	CMOS buffers VDD=2.7V	0.7 VDD		V
Threshold Schmitt trigger input voltage	VT+	-	Note 5	1.06	1.61	V
Threshold Schmitt trigger input voltage	VT-	-	Note 5	0.78	1.25	V
Hysteresis	Delta VT	-	Note 5	0.25		V

§2.3.1.2 (VDD=3V)
Add:

Low level input voltage	VIL	-	CMOS buffers VDD=2.7V		0.8	V
High level input voltage	VIH	-	CMOS buffers VDD=3.3V	2		V
Threshold Schmitt trigger input voltage	VT+	-	Note 5	1.25	1.93	V
Threshold Schmitt trigger input voltage	VT-	-	Note 5	0.90	1.42	V
Hysteresis	Delta VT	-	Note 5	0.31		V

§2.3.1.3 (VDD=3.3V)
Add:

Low level input voltage	VIL	-	CMOS buffers VDD=3V		0.8	V
High level input voltage	VIH	-	CMOS buffers VDD=3.6V	2		V
Threshold Schmitt trigger input voltage	VT+	-	Note 5	1.40	2.08	V
Threshold Schmitt trigger input voltage	VT-	-	Note 5	0.99	1.51	V
Hysteresis	Delta VT	-	Note 5	0.37		V

§2.3.1.4 (VDD=2.5, 3 or 3.3V VCC=5V)
Add:

Low level input voltage	VIL	-	PICV, PICV5 buffers VDD min		0.8	V
High level input voltage	VIH	-	PICV, PICV5 buffers VDD max	2		V
Threshold Schmitt trigger input voltage	VT+	-	Note 5	1.40	2.08	V
Threshold Schmitt trigger input voltage	VT-	-	Note 5	0.99	1.51	V
Hysteresis	Delta VT	-	Note 5	0.37		V

7. Change #7 :

§2.3.2. Notes to electrical measurements

Reason of change :
Notes 6 and 7 are no more applicable in final version

Description of change:
Remove notes 6 and 7.

MARK-up CONCLUSION
PER DCR 321
S. Thaller.
9/7/7
13/7/7

ESCC
European Space Components Coordination

Pages 1 to 28

INTEGRATED CIRCUITS, SILICON MONOLITHIC, CMOS,

GATE ARRAY/EMBEDDED ARRAY

BASED ON TYPE MH1RT

ESCC Detail Specification No. 9202/076

Issue 1 2 Draft B	~~December 2006~~ July 2007

esa

Document Custodian: European Space Agency - see https://escies.org

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DOCUMENTATION CHANGE NOTICE

(Refer to https://escies.org for ESCC DCR content)

DCR No.	CHANGE DESCRIPTION
321	Specification reissued to incorporate changes per DCR.

TABLE OF CONTENTS

1. GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics and test and inspection data for the component type variants and/or the range of components specified below. It supplements the requirements of, and shall be read in conjunction with, the ESCC Generic Specification listed under Applicable Documents.

1.2 APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:

(a) ESCC Generic Specification No. 9000.
(b) MIL-STD-883, Test Methods and Procedures for Microelectronics.

1.3 TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESCC Basic Specification No. 21300 shall apply.

1.4 THE ESCC COMPONENT NUMBER AND COMPONENT TYPE VARIANTS

1.4.1 The ESCC Component Number

The ESCC Component number shall be constituted as follows:

Example: 920207601RXYZ

- Detail Specification Reference: 9202076
- Component Type Variant Number: 01 (as required)
- Total Dose Radiation Level Letter: R (as required)
- Manufacturer Specific ASIC Identification: XYZ (as applicable) where:

  X: Single letter allocated by the ESCC Executive to the manufacturer and each complete code registered with the ESCC Executive Secretariat.

  XYZ : Individual 2 character code allocated by the Manufacturer to a specific ASIC design.

1.4.2 Component Type Variants

The component type variants applicable to this specification are as follows:

Variant Number	Based on Type	Circuit Function	Supply Voltage	Case	Terminal Material and Finish (Note 5)	Weight max g	Total Dose Radiation Level Letter (Note 6)	Notes
01	TH1099ER	988000 sites	Single Supply (3V)	MQFP-T352	D2	27	R [100kRAD(Si)]	1, 3

Variant Number	Based on Type	Circuit Function	Supply Voltage	Case	Terminal Material and Finish (Note 5)	Weight max g	Total Dose Radiation Level Letter (Note 6)	Notes
02	TH1099ER	988000 sites	Single Supply (3V)	MQFP-F256	D2	14	R [100kRAD(Si)]	1, 3
03	TH1099ER	988000 sites	Single Supply (3V)	MQFP-F196	D2	10	R [100kRAD(Si)]	1, 3
04	TH1099ER	988000 sites	Single Supply (3V)	MCGA-349	R	9	R [100kRAD(Si)]	1, 3
05	TH1156ER	1558000 sites	Single Supply (3V)	MQFP-T352	D2	27	R [100kRAD(Si)]	1, 3
06	TH1156ER	1558000 sites	Single Supply (3V)	MQFP-F256	D2	14	R [100kRAD(Si)]	1, 3
07	TH1156ER	1558000 sites	Single Supply (3V)	MCGA-472	R	12	R [100kRAD(Si)]	1, 3
08	TH1156ER	1558000 sites	Single Supply (3V)	MCGA-349	R	9	R [100kRAD(Si)]	1, 3
09	TH1242ER	2422000 sites	Single Supply (3V)	MQFP-T352	D2	27	R [100kRAD(Si)]	1, 3
10	TH1242ER	2422000 sites	Single Supply (3V)	MQFP-F256	D2	14	R [100kRAD(Si)]	1, 3
11	TH1242ER	2422000 sites	Single Supply (3V)	MCGA-472	R	12	R [100kRAD(Si)]	1, 3
12	TH1242ER	2422000 sites	Single Supply (3V)	MCGA-349	R	9	R [100kRAD(Si)]	1, 3
13	TH1332ER	3319000 sites	Single Supply (3V)	MCGA-472	R	12	R [100kRAD(Si)]	1, 3
14	TH1099ES	988000 sites	Bi-voltage Supply (3V/5V)	MQFP-T352	D2	27	R [100kRAD(Si)]	2, 3
15	TH1099ES	988000 sites	Bi-voltage Supply (3V/5V)	MQFP-F256	D2	14	R [100kRAD(Si)]	2, 3

Variant Number	Based on Type	Circuit Function	Supply Voltage	Case	Terminal Material and Finish (Note 5)	Weight max g	Total Dose Radiation Level Letter (Note 6)	Notes
16	TH1099ES	988000 sites	Bi-voltage Supply (3V/5V)	MQFP-F196	D2	10	R [100kRAD(Si)]	2, 3
17	TH1099ES	988000 sites	Bi-voltage Supply (3V/5V)	MCGA-349	R	9	R [100kRAD(Si)]	2, 3
18	TH1156ES	1558000 sites	Bi-voltage Supply (3V/5V)	MQFP-T352	D2	27	R [100kRAD(Si)]	2, 3
19	TH1156ES	1558000 sites	Bi-voltage Supply (3V/5V)	MQFP-F256	D2	14	R [100kRAD(Si)]	2, 3
20	TH1156ES	1558000 sites	Bi-voltage Supply (3V/5V)	MCGA-472	R	12	R [100kRAD(Si)]	2, 3
21	TH1156ES	1558000 sites	Bi-voltage Supply (3V/5V)	MCGA-349	R	9	R [100kRAD(Si)]	2, 3
22	TH1242ES	2422000 sites	Bi-voltage Supply (3V/5V)	MQFP-T352	D2	27	R [100kRAD(Si)]	2, 3
23	TH1242ES	2422000 sites	Bi-voltage Supply (3V/5V)	MQFP-F256	D2	14	R [100kRAD(Si)]	2, 3
24	TH1242ES	2422000 sites	Bi-voltage Supply (3V/5V)	MCGA-472	R	12	R [100kRAD(Si)]	2, 3
25	TH1242ES	2422000 sites	Bi-voltage Supply (3V/5V)	MCGA-349	R	9	R [100kRAD(Si)]	2, 3
26	TH1332ES	3319000 sites	Bi-voltage Supply (3V/5V)	MCGA-472	R	12	R [100kRAD(Si)]	2, 3
27	TH1M099ER	988000 sites composite	Single Supply (3V)	MQFP-T352	D2	27	R [100kRAD(Si)]	1, 4
28	TH1M099ER	988000 sites composite	Single Supply (3V)	MQFP-F256	D2	14	R [100kRAD(Si)]	1, 4
29	TH1M099ER	988000 sites composite	Single Supply (3V)	MQFP-F196	D2	10	R [100kRAD(Si)]	1, 4

Variant Number	Based on Type	Circuit Function	Supply Voltage	Case	Terminal Material and Finish (Note 5)	Weight max g	Total Dose Radiation Level Letter (Note 6)	Notes
30	TH1M099ER	988000 sites composite	Single Supply (3V)	MCGA-349	R	9	R [100kRAD(Si)]	1, 4
31	TH1M156ER	1558000 sites composite	Single Supply (3V)	MQFP-T352	D2	27	R [100kRAD(Si)]	1, 4
32	TH1M156ER	1558000 sites composite	Single Supply (3V)	MQFP-F256	D2	14	R [100kRAD(Si)]	1, 4
33	TH1M156ER	1558000 sites composite	Single Supply (3V)	MCGA-472	R	12	R [100kRAD(Si)]	1, 4
34	TH1M156ER	1558000 sites composite	Single Supply (3V)	MCGA-349	R	9	R [100kRAD(Si)]	1, 4
35	TH1M242ER	2422000 sites composite	Single Supply (3V)	MQFP-T352	D2	27	R [100kRAD(Si)]	1, 4
36	TH1M242ER	2422000 sites composite	Single Supply (3V)	MQFP-F256	D2	14	R [100kRAD(Si)]	1, 4
37	TH1M242ER	2422000 sites composite	Single Supply (3V)	MCGA-472	R	12	R [100kRAD(Si)]	1, 4
38	TH1M242ER	2422000 sites composite	Single Supply (3V)	MCGA-349	R	9	R [100kRAD(Si)]	1, 4
39	TH1M332ER	3319000 sites composite	Single Supply (3V)	MCGA-472	R	12	R [100kRAD(Si)]	1, 4
40	TH1M099ES	988000 sites composite	Bi-voltage Supply (3V/5V)	MQFP-T352	D2	27	R [100kRAD(Si)]	2, 4
41	TH1M099ES	988000 sites composite	Bi-voltage Supply (3V/5V)	MQFP-F256	D2	14	R [100kRAD(Si)]	2, 4
42	TH1M099ES	988000 sites composite	Bi-voltage Supply (3V/5V)	MQFP-F196	D2	10	R [100kRAD(Si)]	2, 4
43	TH1M099ES	988000 sites composite	Bi-voltage Supply (3V/5V)	MCGA-349	R	9	R [100kRAD(Si)]	2, 4

Variant Number	Based on Type	Circuit Function	Supply Voltage	Case	Terminal Material and Finish (Note 5)	Weight max g	Total Dose Radiation Level Letter (Note 6)	Notes
44	TH1M156ES	1558000 sites composite	Bi-voltage Supply (3V/5V)	MQFP-T352	D2	27	R [100kRAD(Si)]	2, 4
45	TH1M156ES	1558000 sites composite	Bi-voltage Supply (3V/5V)	MQFP-F256	D2	14	R [100kRAD(Si)]	2, 4
46	TH1M156ES	1558000 sites composite	Bi-voltage Supply (3V/5V)	MCGA-472	R	12	R [100kRAD(Si)]	2, 4
47	TH1M156ES	1558000 sites composite	Bi-voltage Supply (3V/5V)	MCGA-349	R	9	R [100kRAD(Si)]	2, 4
48	TH1M242ES	2422000 sites composite	Bi-voltage Supply (3V/5V)	MQFP-T352	D2	27	R [100kRAD(Si)]	2, 4
49	TH1M242ES	2422000 sites composite	Bi-voltage Supply (3V/5V)	MQFP-F256	D2	14	R [100kRAD(Si)]	2, 4
50	TH1M242ES	2422000 sites composite	Bi-voltage Supply (3V/5V)	MCGA-472	R	12	R [100kRAD(Si)]	2, 4
51	TH1M242ES	2422000 sites composite	Bi-voltage Supply (3V/5V)	MCGA-349	R	9	R [100kRAD(Si)]	2, 4
52	TH1M332ES	3319000 sites composite	Bi-voltage Supply (3V/5V)	MCGA-472	R	12	R [100kRAD(Si)]	2, 4

NOTES:

1. The component is specified for operation at a nominal single supply voltage V_{DD} = 2.5V, 3V or 3.3V.
2. The component is specified for bi-voltage operation at V_{DD} = 2.5V, 3V or 3.3V and inputs and/or outputs tolerant or compliant to V_{CC} = 5V.
3. The ASIC design will be customised at metal levels.
4. The ASIC design will be customised at base wafer and metal levels.
5. The terminal material and finish shall be in accordance with the requirements of ESCC Basic Specification No. 23500.
6. The total dose radiation level letter shall be as defined in ESCC Basic Specification No. 22900. If an alternative radiation test level is specified in the Purchase Order the letter shall be changed accordingly.

1.4.3 Manufacturer Specific ASIC Identification

An ASIC Sheet shall be produced by the Manufacturer, after negotiation with the Orderer, that, as a minimum, specifies all the requirements unique to the specific ASIC design that are identified herein as being specified in the ASIC Sheet. The ASIC Sheet shall be held under configuration control by the Manufacturer. For identification and traceability purposes the Manufacturer shall allocate a unique Manufacturer Specific ASIC Identification to the ASIC Sheet and the specific ASIC design as specified in The ESCC Component Number herein.

1.5 MAXIMUM RATINGS

The maximum ratings shall not be exceeded at any time during use or storage.
Maximum ratings shall only be exceeded during testing to the extent specified in this specification and when stipulated in Test Methods and Procedures of the ESCC Generic Specification.

Characteristics	Symbols	Maximum Ratings	Units	Remarks
Supply Voltage	V_{DD} V_{CC}	-0.5 to 4 -0.5 to 6	V	Note 1
Input Voltage 2.5V, 3V, 3.3V Range 5V Compliant 5V Tolerant	V_{IN}	 -0.5 to V_{DD} +0.5 -0.5 to V_{CC} +0.5 -0.5V ≤ V_{CC} ≤ 6	V	Note 1, 2
Device Power Dissipation (Continuous)	P_D	See ASIC Sheet	W	
Supply Current	I_{DDop}	See ~~±60~~ ASIC Sheet	mA	
Operating Temperature Range	T_{op}	-55 to +125	°C	T_{amb}
Storage Temperature Range	T_{stg}	-65 to +150	°C	
Junction Temperature	T_j	+175	°C	
Thermal Resistance Junction to case ~~MQFP-F196~~ ~~MQFP-F256~~ ~~MQFP-T352~~ ~~MCCA-349~~ ~~MCCA-472~~	$R_{th(j-c)}$	See ASIC Sheet 5 4.5 2.5 1.5	°C/W	~~Note 3~~
Soldering Temperature	T_{sol}	+300	°C	Note 3

Conclusion requested from QCT on this point

NOTES:

1. With reference to V_{SS} = 0V.
2. Applicable to all inputs. Input current limited to I_{IC} = ±10mA.
3. Duration 10 seconds maximum at a distance of not less than 1.6mm from the device body and the same terminal shall not be resoldered until 3 minutes have elapsed.

1.6 HANDLING PRECAUTIONS

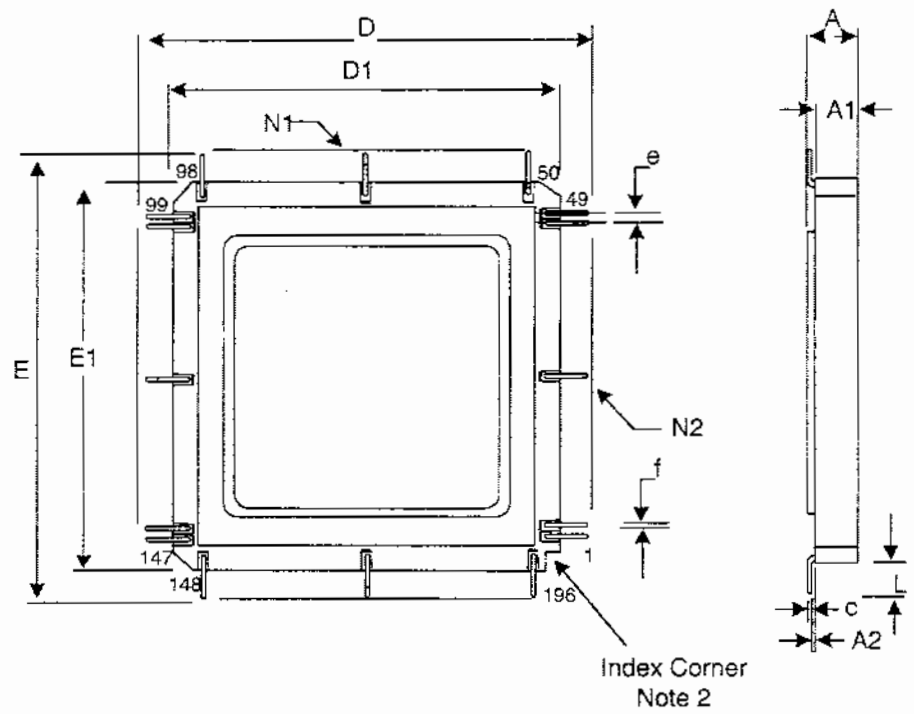
These devices are susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacture, testing, packaging, shipment and any handling.

These components are categorised as Class 3 per ESCC Basic Specification No. 23800 with a Minimum Critical Path Failure Voltage of 4000 Volts.

Input Current	I_{IN}	± 60	mA	Each Input pin

1.7 PHYSICAL DIMENSIONS AND TERMINAL IDENTIFICATION

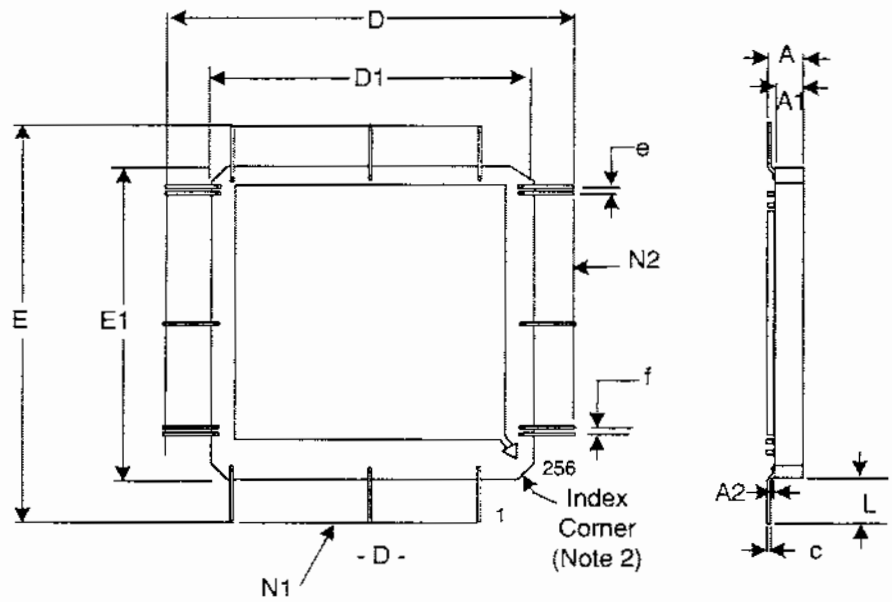
1.7.1 Multilayer Quad Flat Package (MQFP-F196) - 196 Flat Leads



Symbols	Dimensions mm		Notes
	Min	Max	
A	2.13	2.65	
A1	1.83	2.24	
A2	0.202	0.204	
c	0.102	0.203	1
D/E	46.73	47.94	
D1/E1	34.03	34.54	
e	0.635 BSC		1
f	0.15	0.25	1
L	6.35	6.7	1
N1/N2	49		Each side

NOTES:
1. Applies to all leads.
2. Terminal identification is specified by reference to the index corner as shown.

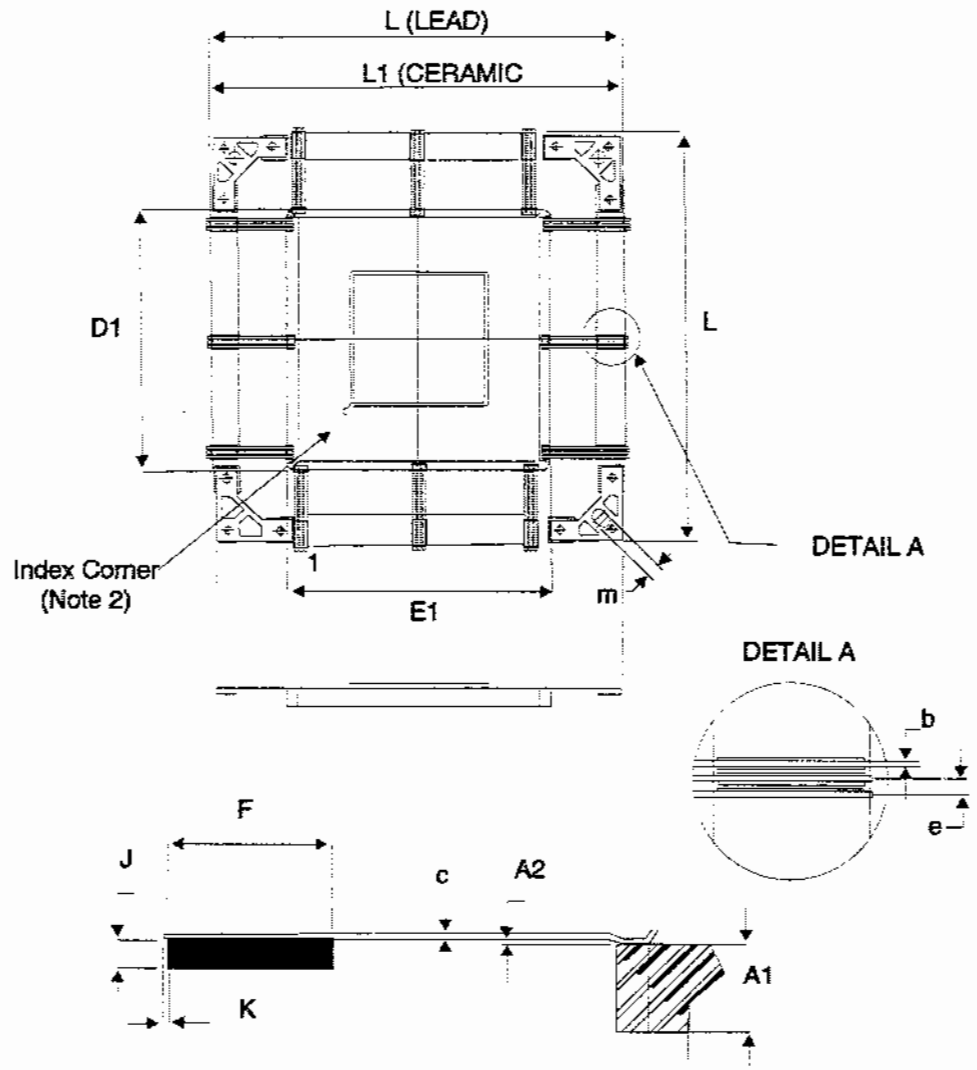
1.7.2 Multilayer Quad Flat Package (MQFP-F256) - 256 Flat Leads



Symbols	Dimensions mm		Notes
	Min	Max	
A	2.41	3.18	
A1	2.06	2.56	
A2	0.05	0.36	
c	0.1	0.2	1
D/E	53.23	55.74	
D1/E1	36.83	37.34	
e	0.508 BSC		1
f	0.15	0.25	1
L	8.2	9.2	1
N1/N2	64		Each side

NOTES:
1. Applies to all leads.
2. Terminal identification is specified by reference to the index corner as shown.

1.7.3 Multilayer Quad Flat Package (MQFP-T352) - 352 Tied Leads



Symbols	Dimensions mm		Notes
	Min	Max	
A1	2.35	3.15	
A2	0.05	0.35	
b	0.19	0.25	1
c	0.11	0.2	1
D1/E1	47.52	48.48	
e	0.50 BSC		1
F	4.5	5.5	
G	2.5	2.6	
J	0.75	1.05	

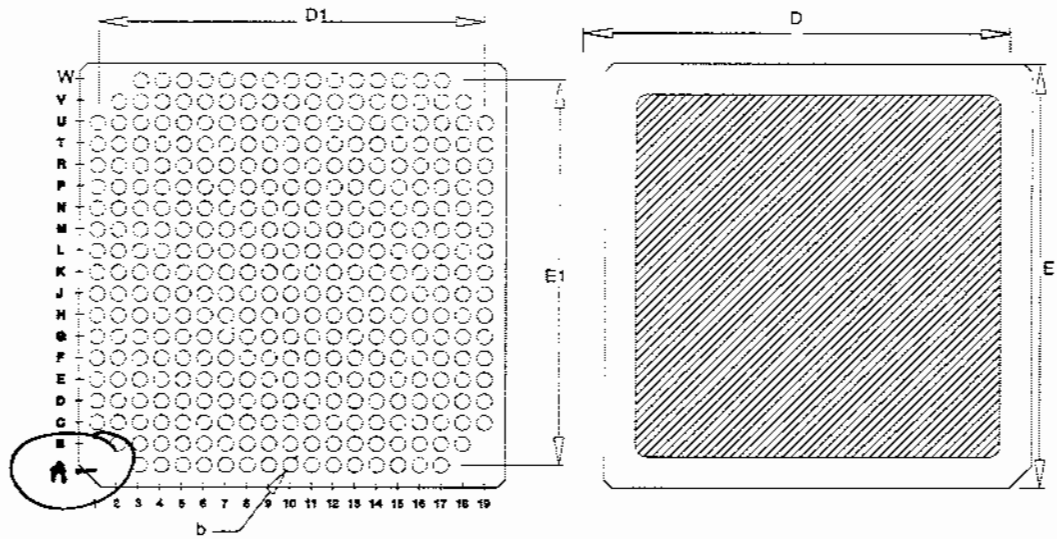
Symbols	Dimensions mm		Notes
	Min	Max	
K	-	0.5	1
L	74.85	76.4	
L1	74.6	75.4	
m	2.5	2.65	
N1/N2	88		Each side

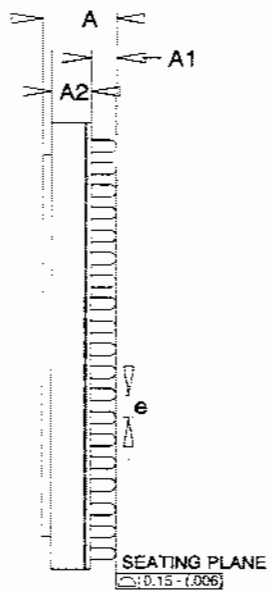
NOTES:
1. Applies to all leads.
2. Terminal identification is specified by reference to the index corner as shown.

1.7.4 Multilayer Column Grid Array (MCGA-349) - 349 Columns

BOTTOM VIEW

TOP VIEW



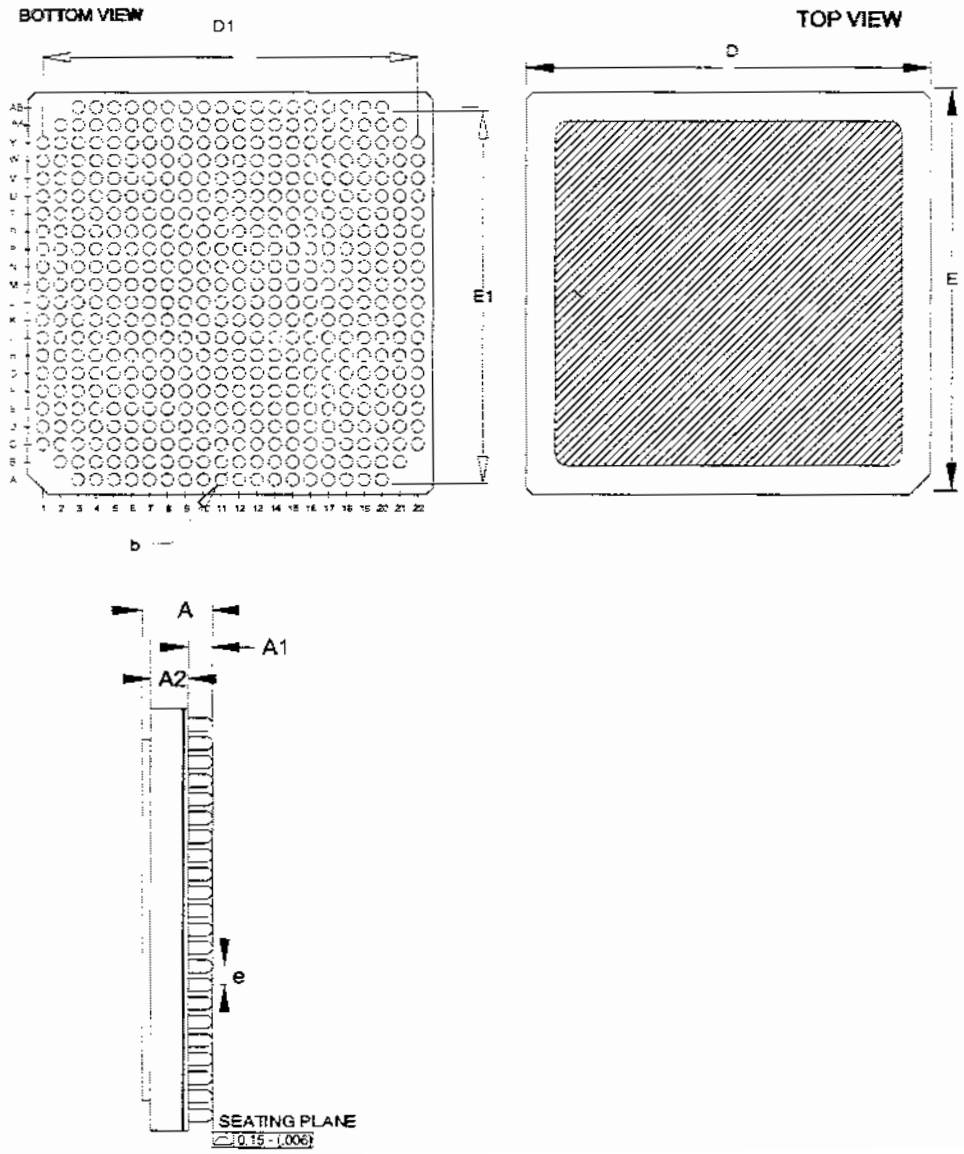


Symbols	Dimensions mm		Notes
	Min	Max	
A	4.3	5.9	
A1	1.4	1.85	
A2	2.4	3.45	
b	0.79	0.99	1

Symbols	Dimensions mm		Notes
	Min	Max	
D/E	24.8	25.2	
D1/E1	22.86		
e	1.27 BSC		1

NOTES:
1. Applies to all columns.
2. Terminal identification is specified by reference to the index corner as shown.

1.7.5 Multilayer Column Grid Array (MCGA-472) - 472 Columns



Symbols	Dimensions mm		Notes
	Min	Max	
A	4.3	5.9	
A1	1.4	1.85	
A2	2.6	3.45	
b	0.79	0.99	1
D/E	28.77	29.23	
D1/E1	26.67		
e	1.27 BSC		1

NOTES:
1. Applies to all columns.
2. Terminal identification is specified by reference to the index corner as shown.

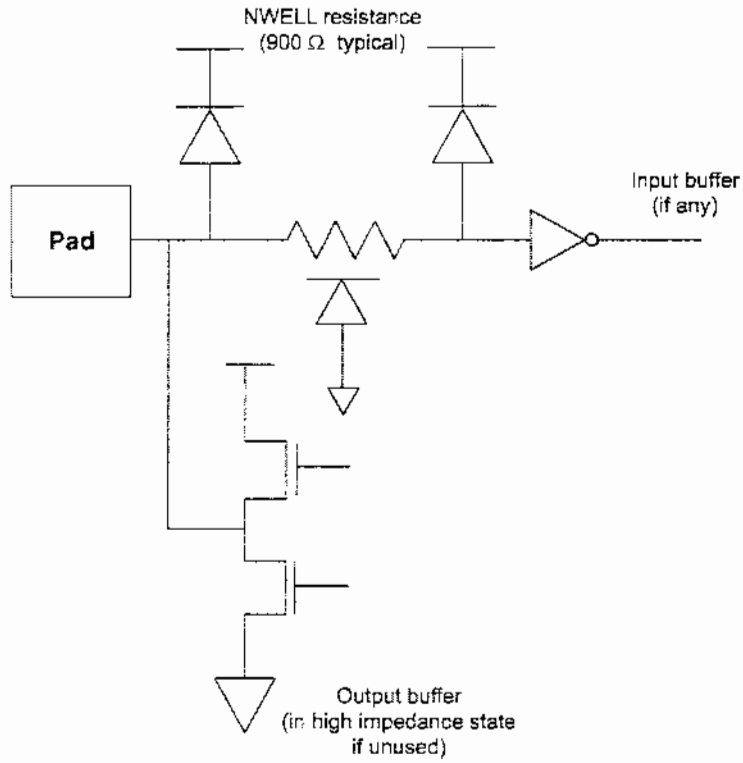
1.8 FUNCTIONAL DIAGRAM
See ASIC Sheet.

NOTES:
1. For all packages the lid is internally connected to the ground terminal as specified in the ASIC Sheet.

1.9 PIN ASSIGNMENT
See ASIC Sheet.

1.10 INSTRUCTION SET AND TIMING DIAGRAMS
See ASIC Sheet.

1.11 PROTECTION NETWORK



2. REQUIREMENTS

2.1 GENERAL

The complete requirements for procurement of the components specified herein are as stated in this specification and the ESCC Generic Specification. Permitted deviations from the Generic Specification, applicable to this specification only, are listed below.

Permitted deviations from the Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESCC requirement and do not affect the component's reliability, are listed in the appendices attached to this specification.

2.1.1 Deviations from the Generic Specification

2.1.1.1 Deviations from Screening Tests

High Temperature Reverse Bias Burn-in shall not be performed.

2.2 MARKING

The marking shall be in accordance with the requirements of ESCC Basic Specification No. 21700 and

as follows.

As a minimum the information to be marked on the component shall be:

(a) The ESCC qualified components symbol (for ESCC qualified components only).
(b) The ESCC Component Number.
(c) Traceability information.

The complete marking shall be as specified in the ASIC Sheet.

2.3 ELECTRICAL MEASUREMENTS AT ROOM, HIGH AND LOW TEMPERATURES

Electrical measurements shall be performed at room, high and low temperatures. Consolidated notes are given after the tables.

2.3.1 Room Temperature Electrical Measurements

The measurements shall be performed at T_{amb} = +22 ± 3°C.

2.3.1.1 Room Temperature Electrical Measurements for Components Specified at Single Supply Voltage V_{DD} = 2.5V

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1 (V_{DD} = 2.5 ± 0.2V)	Limits		Units
				Min	Max	
Functional Test 1	-	3014	See ASIC Sheet V_{DD}=2.3V	-	-	-
Functional Test 2	-	3014	See ASIC Sheet V_{DD}=2.5V	-	-	-
Functional Test 3	-	3014	See ASIC Sheet V_{DD}=2.7V	-	-	-
Supply Current, Stand-by	I_{DDSB}	3005	See ASIC Sheet			mA
Supply Current, Operating	I_{DDOP}	3005	See ASIC Sheet			mA
Low Level Input Current	I_{IL}	3009	V_{IN}=V_{SS}, CMOS Buffers	-	-1	µA
Low Level Input Current, Pull-up Resistor PRU1	I_{ILPU}	3009	V_{IN}=V_{SS}, CMOS Buffers Note 2	70	230	µA
Low Level Input Current, Pull-down Resistor PRD1	I_{ILPD}	3009	V_{IN}=V_{SS}, CMOS Buffers Note 2	-	±5	µA
High Level Input Current	I_{IH}	3010	V_{IN}=V_{DD}, CMOS Buffers	-	1	µA
High Level Input Current, Pull-up Resistor PRU1	I_{IHPU}	3010	V_{IN}=V_{DD}, CMOS Buffers Note 2	-	±5	µA

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1 (V_{DD} = 2.5 ± 0.2V)	Limits		Units
				Min	Max	
High Level Input Current, Pull-down Resistor PRD1	I_{IHPD}	3010	$V_{IN}=V_{DD}$, CMOS Buffers Note 2	70	540	µA
Output Leakage Current Third State, Low Level Applied	I_{OZL}	3020	V_{OUT}=0V, All Buffers V_{DD}=2.7V	-	-1	µA
Output Leakage Current Third State, High Level Applied	I_{OZH}	3021	V_{OUT}=0V, All Buffers V_{DD}=2.7V	-	1	µA
Input Current, Cold Sparing	I_{ICS}	-	V_{IN}=0V to 2.7V, PICZ Buffers $V_{DD}=V_{SS}$=0V	-	±2	µA
Output Current, Cold Sparing	I_{OCS}	-	V_{OUT}=0V to 2.7V, PO11Z Buffers $V_{DD}=V_{SS}$=0V	-	±2	µA
Low Level Output Voltage	V_{OL}	3007	V_{DD}=2.3V, I_{OL}=800µA PO11 Buffers Note 3	-	~~0.4~~ 400	~~V~~ mV
High Level Output Voltage	V_{OH}	3006	V_{DD}=2.3V, I_{OH}=-600µA PO11 Buffers Note 4	2	-	V
Output Short Circuit Current, to V_{DD}	I_{OSN}	-	PO11 output at High Level shorted to V_{DD} Note 5	-	15	mA
Output Short Circuit Current, to V_{SS}	I_{OSP}	-	PO11 output at High Level shorted to V_{SS} Note 5	-	8	mA
Input Capacitance	C_{IN}	3012	Note 5	-	2.4	pF
Output Capacitance	C_{OUT}	3012	Note 5	-	5.6	pF
Input/Output Capacitance	$C_{I/O}$	3012	Note 5	-	6.6	pF
Timings	-	3003	See ASIC Sheet			ns
Low Level Input Voltage	V_{IL}	-	CMOS Buffers V_{DD} = 2.3V	-	690	mV
High Level Input Voltage	V_{IH}	-	CMOS Buffers V_{DD} = 2.7V	1.89	-	V
Positive Trigger Threshold Voltage	V_{TP}	-	Note 5	1.06	1.61	V
Negative Trigger Threshold Voltage	V_{TN}	-	Note 5	0.78	1.25	V
Hysteresis Voltage	V_H	-	Note 5	250	-	mV

2.3.1.2 *Room Temperature Electrical Measurements for Components Specified at Single Supply Voltage V_{DD} = 3V*

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1 (V_{DD} = 3 ± 0.3V)	Limits		Units
				Min	Max	
Functional Test 1	-	3014	See ASIC Sheet V_{DD}=2.7V	-	-	-
Functional Test 2	-	3014	See ASIC Sheet V_{DD}=3V	-	-	-
Functional Test 3	-	3014	See ASIC Sheet V_{DD}=3.3V	-	-	-
Supply Current, Stand-by	I_{DDSB}	3005	See ASIC Sheet			mA
Supply Current, Operating	I_{DDOP}	3005	See ASIC Sheet			mA
Low Level Input Current	I_{IL}	3009	V_{IN}=V_{SS}, CMOS Buffers	-	-1	µA
Low Level Input Current, Pull-up Resistor PRU1	I_{ILPU}	3009	V_{IN}=V_{SS}, CMOS Buffers Note 2	108	330	µA
Low Level Input Current, Pull-down Resistor PRD1	I_{ILPD}	3009	V_{IN}=V_{SS}, CMOS Buffers Note 2	-	±5	µA
High Level Input Current	I_{IH}	3010	V_{IN}=V_{DD}, CMOS Buffers	-	1	µA
High Level Input Current, Pull-up Resistor PRU1	I_{IHPU}	3010	V_{IN}=V_{DD}, CMOS Buffers Note 2	-	±5	µA
High Level Input Current, Pull-down Resistor PRD1	I_{IHPD}	3010	V_{IN}=V_{DD}, CMOS Buffers Note 2	108	825	µA
Output Leakage Current Third State, Low Level Applied	I_{OZL}	3020	V_{OUT}=0V, All Buffers V_{DD}=3.3V	-	-1	µA
Output Leakage Current Third State, High Level Applied	I_{OZH}	3021	V_{OUT}=0V, All Buffers V_{DD}=3.3V	-	1	µA
Input Current, Cold Sparing	I_{ICS}	-	V_{IN}=0V to 3.3V, PICZ Buffers V_{DD}=V_{SS}=0V	-	±2	µA
Output Current, Cold Sparing	I_{OCS}	-	V_{OUT}=0V to 3.3V, PO11X Buffers V_{DD}=V_{SS}=0V	-	±2	µA

* → see attached.

*
Para 2.3.1.2 (P21)

Low Level Input Voltage	V_{IL}	–	CMOS Buffers $V_{DD} = 2.7V$	–	800	mV
High Level Input Voltage	V_{IH}	–	CMOS Buffers $V_{DD} = 3.3V$	2	–	V
Positive Trigger Threshold Voltage	V_{TP}	–	Note 5	1.25	1.93	V
Negative Trigger Threshold Voltage	V_{TN}	–	Note 5	0.9	1.42	V
Hysteresis Voltage	V_H	–	Note 5	0.31	–	mV

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1 (V_{DD} = 3 ± 0.3V)	Limits		Units
				Min	Max	
Low Level Output Voltage	V_{OL}	3007	V_{DD}=2.7V, I_{OL}=1mA PO11 Buffers Note 3	-	~~0.4~~ 400	~~V~~ mV
High Level Output Voltage	V_{OH}	3006	V_{DD}=2.7V, I_{OH}=-800µA PO11 Buffers Note 4	2.4	-	V
Output Short Circuit Current, to V_{DD}	I_{OSN}	-	PO11 output at High Level shorted to V_{DD} Note 5	-	21	mA
Output Short Circuit Current, to V_{SS}	I_{OSP}	-	PO11 output at High Level shorted to V_{SS} Note 5	-	12	mA
Input Capacitance	C_{IN}	3012	Note 5	-	2.4	pF
Output Capacitance	C_{OUT}	3012	Note 5	-	5.6	pF
Input/Output Capacitance	$C_{I/O}$	3012	Note 5	-	6.6	pF
Timings	-	3003	See ASIC Sheet			ns

2.3.1.3 *Room Temperature Electrical Measurements for Components Specified at Single Supply Voltage V_{DD} = 3.3V*

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1 (V_{DD} = 3.3 ± 0.3V)	Limits		Units
				Min	Max	
Functional Test 1	-	3014	See ASIC Sheet V_{DD}=3V	-	-	-
Functional Test 2	-	3014	See ASIC Sheet V_{DD}=3.3V	-	-	-
Functional Test 3	-	3014	See ASIC Sheet V_{DD}=3.6V	-	-	-
Supply Current, Stand-by	I_{DDSB}	3005	See ASIC Sheet			mA
Supply Current, Operating	I_{DDOP}	3005	See ASIC Sheet			mA
Low Level Input Current	I_{IL}	3009	V_{IN}=V_{SS}, CMOS Buffers	-	-1	µA
Low Level Input Current, Pull-up Resistor PRU1	I_{ILPU}	3009	V_{IN}=V_{SS}, CMOS Buffers Note 2	120	400	µA

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1 (V_{DD} = 3.3 ± 0.3V)	Limits		Units
				Min	Max	
Low Level Input Current, Pull-down Resistor PRD1	I_{ILPD}	3009	$V_{IN}=V_{SS}$, CMOS Buffers Note 2	-	±5	µA
High Level Input Current	I_{IH}	3010	$V_{IN}=V_{DD}$, CMOS Buffers	-	1	µA
High Level Input Current, Pull-up Resistor PRU1	I_{IHPU}	3010	$V_{IN}=V_{DD}$, CMOS Buffers Note 2	-	±5	µA
High Level Input Current, Pull-down Resistor PRD1	I_{IHPD}	3010	$V_{IN}=V_{DD}$, CMOS Buffers Note 2	150	900	µA
Output Leakage Current Third State, Low Level Applied	I_{OZL}	3020	V_{OUT}=0V, All Buffers V_{DD}=3.6V	-	-1	µA
Output Leakage Current Third State, High Level Applied	I_{OZH}	3021	V_{OUT}=0V, All Buffers V_{DD}=3.6V	-	1	µA
Input Current, Cold Sparing	I_{ICS}	-	V_{IN}=0V to 3.6V, PICZ Buffers $V_{DD}=V_{SS}$=0V	-	±2	µA
Output Current, Cold Sparing	I_{OCS}	-	V_{OUT}=0V to 3.6V, PO11Z Buffers $V_{DD}=V_{SS}$=0V	-	±2	µA
Low Level Output Voltage	V_{OL}	3007	V_{DD}=3V I_{OL}=2mA PO11 Buffers Note 3	-	~~0.4~~ 400	~~V~~ mV
High Level Output Voltage	V_{OH}	3006	V_{DD}=3V I_{OL}=-1.8mA PO11 Buffers Note 4	2.4	-	V
Output Short Circuit Current, to V_{DD}	I_{OSN}	-	PO11 output at High Level shorted to V_{DD} Note 5	-	23	mA
Output Short Circuit Current, to V_{SS}	I_{OSP}	-	PO11 output at High Level shorted to V_{SS} Note 5	-	13	mA
Input Capacitance	C_{IN}	3012	Note 5	-	2.4	pF
Output Capacitance	C_{OUT}	3012	Note 5	-	5.6	pF
Input/Output Capacitance	$C_{I/O}$	3012	Note 5	-	6.6	pF

see attached →

* P 2.3.1.3 (P23)

Low Level Input Voltage	V_{IL}	–	CMOS Buffers V_{DD} = 3V	–	800	mV
High Level Input Voltage	V_{IH}	–	CMOS Buffers V_{DD} = 3.6V	2	–	V
Positive Trigger Threshold Voltage	V_{TP}	–	Note 5	1.4	2.08	V
Negative Trigger Threshold Voltage	V_{TN}	–	Note 5	0.99	1.51	V
Hysteresis Voltage	V_H	–	Note 5	370	–	mV

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1 (V_{DD} = 3.3 ± 0.3V)	Limits		Units
				Min	Max	
Timings	-	3003	See ASIC Sheet			ns

2.3.1.4 *Room Temperature Electrical Measurements for Components Specified for Bi-voltage Operation at V_{DD} = 2.5V, 3V or 3.3V and V_{CC} = 5V.*

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1 [V_{DD} = 2.5 ± 0.2V, 3 ± 0.3V, 3.3 ± 0.3V (Note ~~8~~ 6) V_{CC}=5 ± 0.5V (Note ~~9~~ 7)]	Limits		Units
				Min	Max	
Functional Test 1	-	3014	See ASIC Sheet V_{CC}=4.5V, V_{DD}=3V	-	-	-
Functional Test 2	-	3014	See ASIC Sheet V_{CC}=5V, V_{DD}=3.3V	-	-	-
Functional Test 3	-	3014	See ASIC Sheet V_{CC}=5.5V, V_{DD}=3.6V	-	-	-
Supply Current, Stand-by	I_{DDSB}	3005	See ASIC Sheet			mA
Supply Current, Operating	I_{DDOP}	3005	See ASIC Sheet			mA
Low Level Input Current	I_{IL}	3009	V_{IN}=V_{SS}, CMOS Buffers	-	-1	µA
Low Level Input Current, Pull-up Resistor PRU1	I_{ILPU}	3009	V_{IN}=V_{SS}, CMOS Buffers Note 2	180	690	µA
Low Level Input Current, Pull-down Resistor PRD1	I_{ILPD}	3009	V_{IN}=V_{SS}, CMOS Buffers Note 2	-	±5	µA
High Level Input Current	I_{IH}	3010	V_{IN}=V_{DD}, CMOS Buffers	-	1	µA
High Level Input Current, Pull-up Resistor PRU1	I_{IHPU}	3010	V_{IN}=V_{DD}, CMOS Buffers Note 2	-	±5	µA
High Level Input Current, Pull-down Resistor PRD1	I_{IHPD}	3010	V_{IN}=V_{DD}, CMOS Buffers Note 2	30	400	µA
Output Leakage Current Third State, Low Level Applied	I_{OZL}	3020	V_{OUT}=0V, All Buffers V_{DD}=3.6V	-	-1	µA

see attached →

P2.3.1.4 (P 24)

Low Level Input Voltage	V_{IL}	–	PICV, PICV5 Buffers $V_{DD} = V_{DD}^{min}$	–	800	mV
High Level Input Voltage	V_{IH}	–	PICV, PICV5 Buffers $V_{DD} = V_{DD}^{max}$	2	–	V
Positive Trigger Threshold Voltage	V_{TP}	–	Note 5	1.4	2.08	V
Negative Trigger Threshold Voltage	V_{TN}	–	Note 5	0.99	1.51	V
Hysteresis Voltage	V_H	–	Note 5	370	–	mV

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1 [V_{DD} = 2.5 ± 0.2V, 3 ± 0.3V, 3.3 ± 0.3V (Note 6) V_{CC}=5 ± 0.5V (Note 7)]	Limits		Units
				Min	Max	
Output Leakage Current Third State, High Level Applied	I_{OZH}	3021	V_{OUT}=0V, All Buffers V_{DD}=3.6V	-	1	µA
Input Current, Cold Sparing	I_{ICS}	-	V_{IN}=0V to 3.6V, PICZ Buffers V_{DD}=V_{SS}=0V	-	±2	µA
Output Current, Cold Sparing	I_{OCS}	-	V_{OUT}=0V to 3.6V, PO11Z Buffers V_{DD}=V_{SS}=0V	-	±2	µA
Low Level Output Voltage	V_{OL}	3007	V_{DD}=V_{DD}min, V_{CC}=4.5V	-	~~0.4~~ 400	~~V~~ mV
High Level Output Voltage	V_{OH}	3006	V_{DD}=V_{DD}min(2.5V), V_{CC}=4.5V	2	-	V
			V_{DD}=V_{DD}min(3V, 3.3V), V_{CC}=4.5V	2.4	-	V
Output Short Circuit Current, to V_{DD}	I_{OSN}	-	PO11 output at High Level shorted to V_{DD} Note 5	-	28	mA
Output Short Circuit Current, to V_{SS}	I_{OSP}	-	PO11 output at High Level shorted to V_{SS} Note 5	-	17	mA
Input Capacitance	C_{IN}	3012	Note 5	-	2.4	pF
Output Capacitance	C_{OUT}	3012	Note 5	-	5.6	pF
Input/Output Capacitance	$C_{I/O}$	3012	Note 5	-	6.6	pF
Timing	-	3003	See ASIC Sheet			ns

2.3.2 Notes to Electrical Measurements Tables

1. Unless otherwise specified: all inputs and outputs shall be tested for each characteristic; Inputs not under test shall be V_{IN} = V_{SS}, V_{CC} or V_{DD} and outputs not under test shall be open; V_{SS} = 0V.

2. Standard pull-ups: PRU# where # = [1-31] index for Ron:
   Ron = # x R0 = 19kΩ typical (12 to 30kΩ) in 2.5V range.
   Ron = # x R0 = 15kΩ typical (10 to 25kΩ) in 3V range.
   Ron = # x R0 = 14kΩ typical (9 to 25kΩ) in 3.3V range.
   5V tolerant/compliant pull-ups: PRU# where # = [1-31] index for Ron:
   Ron = # x R0 = 14kΩ typical (8 to 25kΩ) in each range.

   Standard pull-downs: PRD# where # = [1-31] index for Ron:
   Ron = # x R0 = 11kΩ typical (5 to 30kΩ) in 2.5V range.
   Ron = # x R0 = 9kΩ typical (4 to 25kΩ) in 3V range.

Ron = # x R0 = 8kΩ typical (4 to 20kΩ) in 3.3V range.
5V tolerant/compliant pull-downs: PRD# where # = [1-31] index for Ron:
Ron = # x R0 = 36kΩ typical (17 to 80kΩ) in 2.5V range.
Ron = # x R0 = 23kΩ typical (11 to 55kΩ) in 3V range.
Ron = # x R0 = 19kΩ typical (9 to 45kΩ) in 3.3V range.

3. Output buffers: PO$# where
$ = [1-12] quantity of output driving capability of p-channels.
#=[1-12] quantity of output driving capability of n-channels.
Standard buffers (including cold sparing)
IO = 1.6, 1.8, 2mA measured at V_{OL} = ~~0.4~~, ~~0.4~~, ~~0.4~~V in 2.5, 3, 3.3V range respectively.
Tolerance buffers (including cold sparing)
IO = 1, 1.3, 1.4mA measured at V_{OL} = ~~0.4~~, ~~0.4~~, ~~0.4~~V in 2.5, 3, 3.3V range respectively.
Compliant buffers (V_{CC} = 4.5V)
IO = 1.1, 1.4, 1.6mA measured at V_{OL} = ~~0.4~~, ~~0.4~~, ~~0.4~~V in 2.5, 3, 3.3V range respectively.
400, 400, 400mV

4. Output buffers: PO$# where
$ = [1-12] quantity of output driving capability of p-channels.
#=[1-12] quantity of output driving capability of n-channels.
Standard buffers (including cold sparing)
IO = -1.6, -1.8, -2mA measured at V_{OL} = 2, 2.4, 2.4V in 2.5, 3, 3.3V range respectively.
Tolerance buffers (including cold sparing)
IO = -1, -1.3, -1.4mA measured at V_{OL} = 2, 2.4, 2.4V in 2.5, 3, 3.3V range respectively.
Compliant buffers (V_{CC} = 4.5V)
IO = -1.1, -1.4, -1.6mA measured at V_{OL} = 2, 2.4, 2.4V in 2.5, 3, 3.3V range respectively.

5. Guaranteed but not tested.

~~U. Variants 01 to 13 and 27 to 39.~~

~~V. Variants 14 to 26 and 40 to 52.~~

6 ~~S~~. 5V tolerant buffers.

7 ~~9~~. 5V compliant buffers.

2.3.3 High and Low Temperatures Electrical Measurements

Unless otherwise specified the measurements shall be performed at T_{amb} = +125 (+0 -5)°C and T_{amb} = -55 (+5 - 0)°C. Unless otherwise specified the characteristics, test methods, conditions and limits shall be the same as specified for Room Temperature Electrical Measurements.

2.4 PARAMETER DRIFT VALUES

Unless otherwise specified, the measurements shall be performed at T_{amb} = +22 ± 3°C.

The test methods and test conditions shall be as per the corresponding test defined in Room Temperature Electrical Measurements.

The drift values (Δ) shall not be exceeded for each characteristic specified. The corresponding absolute limit values for each characteristic shall not be exceeded.

Characteristics	Symbols	Limits			Units
		Drift Value Δ	Absolute		
			Min	Max	
Supply Current, Stand-by	I_{DDSB}	See ASIC Sheet			mA
Low Level Input Current	I_{IL}	±0.1	-	-1	µA
High Level Input Current	I_{IH}	±0.1	-	1	µA
Output Leakage Current Third State, Low Level Applied	I_{OZL}	±0.1	-	-1	µA
Output Leakage Current Third State, High Level Applied	I_{OZH}	±0.1	-	1	µA
Low Level Output Voltage	V_{OL}	±0.1	-	400	mV
High Level Output Voltage	V_{OH}	±0.1	2.4 or 2	-	V

NOTES:
1. Unless otherwise specified all inputs and outputs shall be tested for each characteristic.

2.5 INTERMEDIATE AND END-POINT ELECTRICAL MEASUREMENTS

Unless otherwise specified, the measurements shall be performed at T_{amb} = +22 ± 3°C. Unless otherwise specified the characteristics, test methods, conditions and limits shall be the same as specified for Room Temperature Electrical Measurements.

2.6 POWER BURN-IN CONDITIONS

See ASIC Sheet.

2.7 OPERATING LIFE CONDITIONS

Unless otherwise specified the conditions shall be as specified for Power Burn-in.

2.8 TOTAL DOSE RADIATION TESTING

2.8.1 Bias Conditions and Total Dose Level for Total Dose Radiation Testing

Continuous bias shall be applied during irradiation testing as specified in the ASIC Sheet.

The total dose level applied shall be as specified in the component type variant information herein, in the ASIC Sheet or in the Purchase Order.

2.8.2 Electrical Measurements for Total Dose Radiation Testing

Prior to irradiation testing the devices shall have successfully met Room Temperature Electrical Measurements specified herein.

Unless otherwise stated the measurements shall be performed at T_{amb} = +22 ± 3°C.
The test methods and test conditions shall be as per the corresponding test defined in Room Temperature Electrical Measurements.

The parameters to be measured during and on completion of irradiation testing are specified in the ASIC Sheet.

MARK-up CONCLUSION
PER DCR 321
S. Thaller.
9/7/7
13/7/7

ESCC
European Space Components Coordination

Pages 1 to 28

INTEGRATED CIRCUITS, SILICON MONOLITHIC, CMOS,

GATE ARRAY/EMBEDDED ARRAY

BASED ON TYPE MH1RT

ESCC Detail Specification No. 9202/076

Issue 1 2 Draft B	~~December 2006~~ July 2007

esa

Document Custodian: European Space Agency - see https://escies.org

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DOCUMENTATION CHANGE NOTICE

(Refer to https://escies.org for ESCC DCR content)

DCR No.	CHANGE DESCRIPTION
321	Specification reissued to incorporate changes per DCR.

TABLE OF CONTENTS

1. GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics and test and inspection data for the component type variants and/or the range of components specified below. It supplements the requirements of, and shall be read in conjunction with, the ESCC Generic Specification listed under Applicable Documents.

1.2 APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:

(a) ESCC Generic Specification No. 9000.
(b) MIL-STD-883, Test Methods and Procedures for Microelectronics.

1.3 TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESCC Basic Specification No. 21300 shall apply.

1.4 THE ESCC COMPONENT NUMBER AND COMPONENT TYPE VARIANTS

1.4.1 The ESCC Component Number

The ESCC Component number shall be constituted as follows:

Example: 920207601RXYZ

- Detail Specification Reference: 9202076
- Component Type Variant Number: 01 (as required)
- Total Dose Radiation Level Letter: R (as required)
- Manufacturer Specific ASIC Identification: XYZ (as applicable) where:

  X: Single letter allocated by the ESCC Executive to the manufacturer and each complete code registered with the ESCC Executive Secretariat.

  XYZ : Individual 2 character code allocated by the Manufacturer to a specific ASIC design.

1.4.2 Component Type Variants

The component type variants applicable to this specification are as follows:

Variant Number	Based on Type	Circuit Function	Supply Voltage	Case	Terminal Material and Finish (Note 5)	Weight max g	Total Dose Radiation Level Letter (Note 6)	Notes
01	TH1099ER	988000 sites	Single Supply (3V)	MQFP-T352	D2	27	R [100kRAD(Si)]	1, 3

Variant Number	Based on Type	Circuit Function	Supply Voltage	Case	Terminal Material and Finish (Note 5)	Weight max g	Total Dose Radiation Level Letter (Note 6)	Notes
02	TH1099ER	988000 sites	Single Supply (3V)	MQFP-F256	D2	14	R [100kRAD(Si)]	1, 3
03	TH1099ER	988000 sites	Single Supply (3V)	MQFP-F196	D2	10	R [100kRAD(Si)]	1, 3
04	TH1099ER	988000 sites	Single Supply (3V)	MCGA-349	R	9	R [100kRAD(Si)]	1, 3
05	TH1156ER	1558000 sites	Single Supply (3V)	MQFP-T352	D2	27	R [100kRAD(Si)]	1, 3
06	TH1156ER	1558000 sites	Single Supply (3V)	MQFP-F256	D2	14	R [100kRAD(Si)]	1, 3
07	TH1156ER	1558000 sites	Single Supply (3V)	MCGA-472	R	12	R [100kRAD(Si)]	1, 3
08	TH1156ER	1558000 sites	Single Supply (3V)	MCGA-349	R	9	R [100kRAD(Si)]	1, 3
09	TH1242ER	2422000 sites	Single Supply (3V)	MQFP-T352	D2	27	R [100kRAD(Si)]	1, 3
10	TH1242ER	2422000 sites	Single Supply (3V)	MQFP-F256	D2	14	R [100kRAD(Si)]	1, 3
11	TH1242ER	2422000 sites	Single Supply (3V)	MCGA-472	R	12	R [100kRAD(Si)]	1, 3
12	TH1242ER	2422000 sites	Single Supply (3V)	MCGA-349	R	9	R [100kRAD(Si)]	1, 3
13	TH1332ER	3319000 sites	Single Supply (3V)	MCGA-472	R	12	R [100kRAD(Si)]	1, 3
14	TH1099ES	988000 sites	Bi-voltage Supply (3V/5V)	MQFP-T352	D2	27	R [100kRAD(Si)]	2, 3
15	TH1099ES	988000 sites	Bi-voltage Supply (3V/5V)	MQFP-F256	D2	14	R [100kRAD(Si)]	2, 3

Variant Number	Based on Type	Circuit Function	Supply Voltage	Case	Terminal Material and Finish (Note 5)	Weight max g	Total Dose Radiation Level Letter (Note 6)	Notes
16	TH1099ES	988000 sites	Bi-voltage Supply (3V/5V)	MQFP-F196	D2	10	R [100kRAD(Si)]	2, 3
17	TH1099ES	988000 sites	Bi-voltage Supply (3V/5V)	MCGA-349	R	9	R [100kRAD(Si)]	2, 3
18	TH1156ES	1558000 sites	Bi-voltage Supply (3V/5V)	MQFP-T352	D2	27	R [100kRAD(Si)]	2, 3
19	TH1156ES	1558000 sites	Bi-voltage Supply (3V/5V)	MQFP-F256	D2	14	R [100kRAD(Si)]	2, 3
20	TH1156ES	1558000 sites	Bi-voltage Supply (3V/5V)	MCGA-472	R	12	R [100kRAD(Si)]	2, 3
21	TH1156ES	1558000 sites	Bi-voltage Supply (3V/5V)	MCGA-349	R	9	R [100kRAD(Si)]	2, 3
22	TH1242ES	2422000 sites	Bi-voltage Supply (3V/5V)	MQFP-T352	D2	27	R [100kRAD(Si)]	2, 3
23	TH1242ES	2422000 sites	Bi-voltage Supply (3V/5V)	MQFP-F256	D2	14	R [100kRAD(Si)]	2, 3
24	TH1242ES	2422000 sites	Bi-voltage Supply (3V/5V)	MCGA-472	R	12	R [100kRAD(Si)]	2, 3
25	TH1242ES	2422000 sites	Bi-voltage Supply (3V/5V)	MCGA-349	R	9	R [100kRAD(Si)]	2, 3
26	TH1332ES	3319000 sites	Bi-voltage Supply (3V/5V)	MCGA-472	R	12	R [100kRAD(Si)]	2, 3
27	TH1M099ER	988000 sites composite	Single Supply (3V)	MQFP-T352	D2	27	R [100kRAD(Si)]	1, 4
28	TH1M099ER	988000 sites composite	Single Supply (3V)	MQFP-F256	D2	14	R [100kRAD(Si)]	1, 4
29	TH1M099ER	988000 sites composite	Single Supply (3V)	MQFP-F196	D2	10	R [100kRAD(Si)]	1, 4

Variant Number	Based on Type	Circuit Function	Supply Voltage	Case	Terminal Material and Finish (Note 5)	Weight max g	Total Dose Radiation Level Letter (Note 6)	Notes
30	TH1M099ER	988000 sites composite	Single Supply (3V)	MCGA-349	R	9	R [100kRAD(Si)]	1, 4
31	TH1M156ER	1558000 sites composite	Single Supply (3V)	MQFP-T352	D2	27	R [100kRAD(Si)]	1, 4
32	TH1M156ER	1558000 sites composite	Single Supply (3V)	MQFP-F256	D2	14	R [100kRAD(Si)]	1, 4
33	TH1M156ER	1558000 sites composite	Single Supply (3V)	MCGA-472	R	12	R [100kRAD(Si)]	1, 4
34	TH1M156ER	1558000 sites composite	Single Supply (3V)	MCGA-349	R	9	R [100kRAD(Si)]	1, 4
35	TH1M242ER	2422000 sites composite	Single Supply (3V)	MQFP-T352	D2	27	R [100kRAD(Si)]	1, 4
36	TH1M242ER	2422000 sites composite	Single Supply (3V)	MQFP-F256	D2	14	R [100kRAD(Si)]	1, 4
37	TH1M242ER	2422000 sites composite	Single Supply (3V)	MCGA-472	R	12	R [100kRAD(Si)]	1, 4
38	TH1M242ER	2422000 sites composite	Single Supply (3V)	MCGA-349	R	9	R [100kRAD(Si)]	1, 4
39	TH1M332ER	3319000 sites composite	Single Supply (3V)	MCGA-472	R	12	R [100kRAD(Si)]	1, 4
40	TH1M099ES	988000 sites composite	Bi-voltage Supply (3V/5V)	MQFP-T352	D2	27	R [100kRAD(Si)]	2, 4
41	TH1M099ES	988000 sites composite	Bi-voltage Supply (3V/5V)	MQFP-F256	D2	14	R [100kRAD(Si)]	2, 4
42	TH1M099ES	988000 sites composite	Bi-voltage Supply (3V/5V)	MQFP-F196	D2	10	R [100kRAD(Si)]	2, 4
43	TH1M099ES	988000 sites composite	Bi-voltage Supply (3V/5V)	MCGA-349	R	9	R [100kRAD(Si)]	2, 4

Variant Number	Based on Type	Circuit Function	Supply Voltage	Case	Terminal Material and Finish (Note 5)	Weight max g	Total Dose Radiation Level Letter (Note 6)	Notes
44	TH1M156ES	1558000 sites composite	Bi-voltage Supply (3V/5V)	MQFP-T352	D2	27	R [100kRAD(Si)]	2, 4
45	TH1M156ES	1558000 sites composite	Bi-voltage Supply (3V/5V)	MQFP-F256	D2	14	R [100kRAD(Si)]	2, 4
46	TH1M156ES	1558000 sites composite	Bi-voltage Supply (3V/5V)	MCGA-472	R	12	R [100kRAD(Si)]	2, 4
47	TH1M156ES	1558000 sites composite	Bi-voltage Supply (3V/5V)	MCGA-349	R	9	R [100kRAD(Si)]	2, 4
48	TH1M242ES	2422000 sites composite	Bi-voltage Supply (3V/5V)	MQFP-T352	D2	27	R [100kRAD(Si)]	2, 4
49	TH1M242ES	2422000 sites composite	Bi-voltage Supply (3V/5V)	MQFP-F256	D2	14	R [100kRAD(Si)]	2, 4
50	TH1M242ES	2422000 sites composite	Bi-voltage Supply (3V/5V)	MCGA-472	R	12	R [100kRAD(Si)]	2, 4
51	TH1M242ES	2422000 sites composite	Bi-voltage Supply (3V/5V)	MCGA-349	R	9	R [100kRAD(Si)]	2, 4
52	TH1M332ES	3319000 sites composite	Bi-voltage Supply (3V/5V)	MCGA-472	R	12	R [100kRAD(Si)]	2, 4

NOTES:

1. The component is specified for operation at a nominal single supply voltage V_{DD} = 2.5V, 3V or 3.3V.
2. The component is specified for bi-voltage operation at V_{DD} = 2.5V, 3V or 3.3V and inputs and/or outputs tolerant or compliant to V_{CC} = 5V.
3. The ASIC design will be customised at metal levels.
4. The ASIC design will be customised at base wafer and metal levels.
5. The terminal material and finish shall be in accordance with the requirements of ESCC Basic Specification No. 23500.
6. The total dose radiation level letter shall be as defined in ESCC Basic Specification No. 22900. If an alternative radiation test level is specified in the Purchase Order the letter shall be changed accordingly.

1.4.3 Manufacturer Specific ASIC Identification

An ASIC Sheet shall be produced by the Manufacturer, after negotiation with the Orderer, that, as a minimum, specifies all the requirements unique to the specific ASIC design that are identified herein as being specified in the ASIC Sheet. The ASIC Sheet shall be held under configuration control by the Manufacturer. For identification and traceability purposes the Manufacturer shall allocate a unique Manufacturer Specific ASIC Identification to the ASIC Sheet and the specific ASIC design as specified in The ESCC Component Number herein.

1.5 MAXIMUM RATINGS

The maximum ratings shall not be exceeded at any time during use or storage.
Maximum ratings shall only be exceeded during testing to the extent specified in this specification and when stipulated in Test Methods and Procedures of the ESCC Generic Specification.

Characteristics	Symbols	Maximum Ratings	Units	Remarks
Supply Voltage	V_{DD} V_{CC}	-0.5 to 4 -0.5 to 6	V	Note 1
Input Voltage 2.5V, 3V, 3.3V Range 5V Compliant 5V Tolerant	V_{IN}	 -0.5 to V_{DD} +0.5 -0.5 to V_{CC} +0.5 -0.5V ≤ V_{CC} ≤ 6	V	Note 1, 2
Device Power Dissipation (Continuous)	P_D	See ASIC Sheet	W	
Supply Current	I_{DDop}	See ~~±60~~ ASIC Sheet	mA	
Operating Temperature Range	T_{op}	-55 to +125	°C	T_{amb}
Storage Temperature Range	T_{stg}	-65 to +150	°C	
Junction Temperature	T_j	+175	°C	
Thermal Resistance Junction to case ~~MQFP-F196~~ ~~MQFP-F256~~ ~~MQFP-T352~~ ~~MCCA-349~~ ~~MCCA-472~~	$R_{th(j-c)}$	See ASIC Sheet 5 4.5 2.5 1.5	°C/W	~~Note 3~~
Soldering Temperature	T_{sol}	+300	°C	Note 3

Conclusion requested from QCT on this point

NOTES:

1. With reference to V_{SS} = 0V.
2. Applicable to all inputs. Input current limited to I_{IC} = ±10mA.
3. Duration 10 seconds maximum at a distance of not less than 1.6mm from the device body and the same terminal shall not be resoldered until 3 minutes have elapsed.

1.6 HANDLING PRECAUTIONS

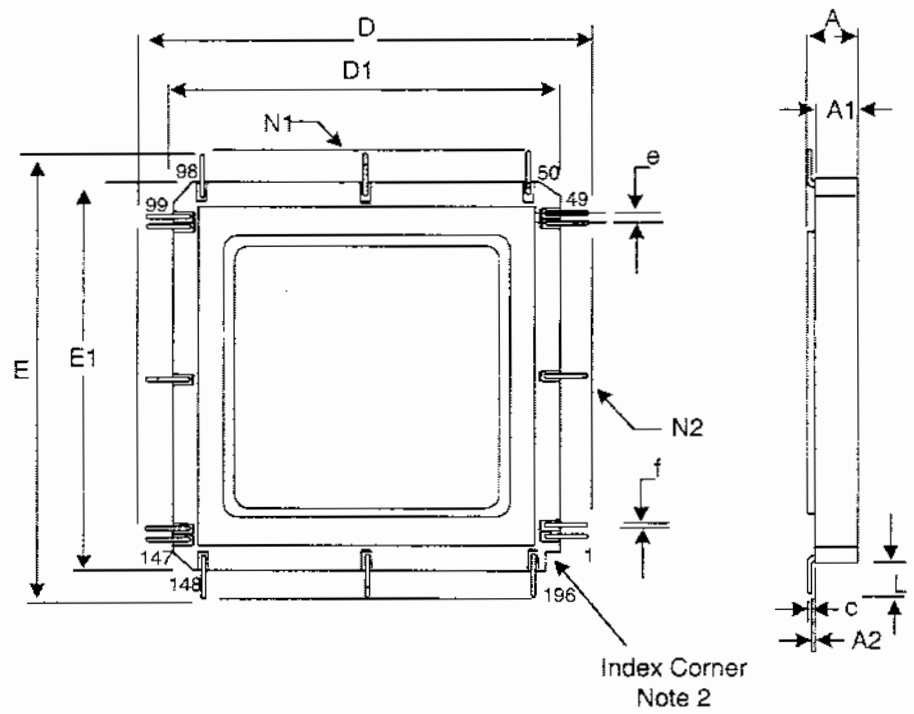
These devices are susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacture, testing, packaging, shipment and any handling.

These components are categorised as Class 3 per ESCC Basic Specification No. 23800 with a Minimum Critical Path Failure Voltage of 4000 Volts.

Input Current	I_{IN}	± 60	mA	Each Input pin

1.7 PHYSICAL DIMENSIONS AND TERMINAL IDENTIFICATION

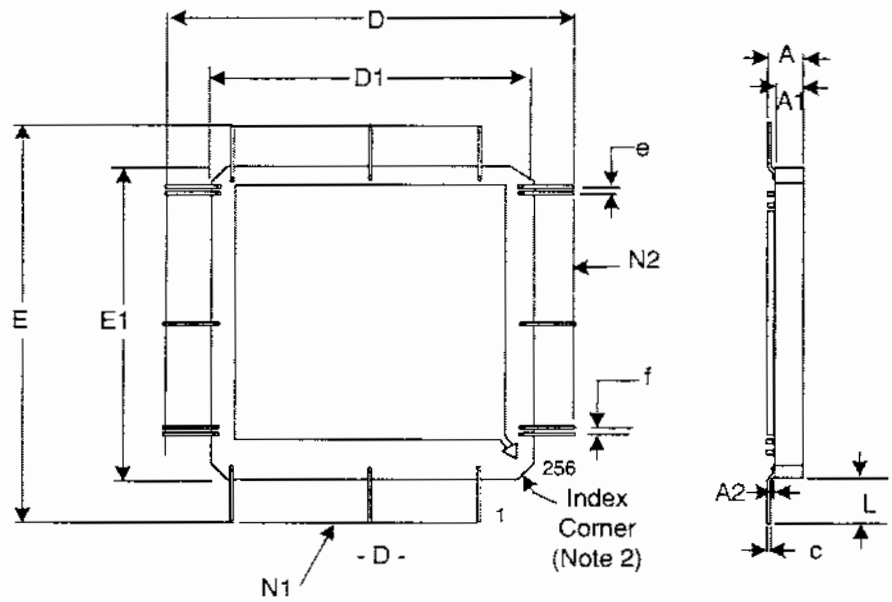
1.7.1 Multilayer Quad Flat Package (MQFP-F196) - 196 Flat Leads



Symbols	Dimensions mm		Notes
	Min	Max	
A	2.13	2.65	
A1	1.83	2.24	
A2	0.202	0.204	
c	0.102	0.203	1
D/E	46.73	47.94	
D1/E1	34.03	34.54	
e	0.635 BSC		1
f	0.15	0.25	1
L	6.35	6.7	1
N1/N2	49		Each side

NOTES:
1. Applies to all leads.
2. Terminal identification is specified by reference to the index corner as shown.

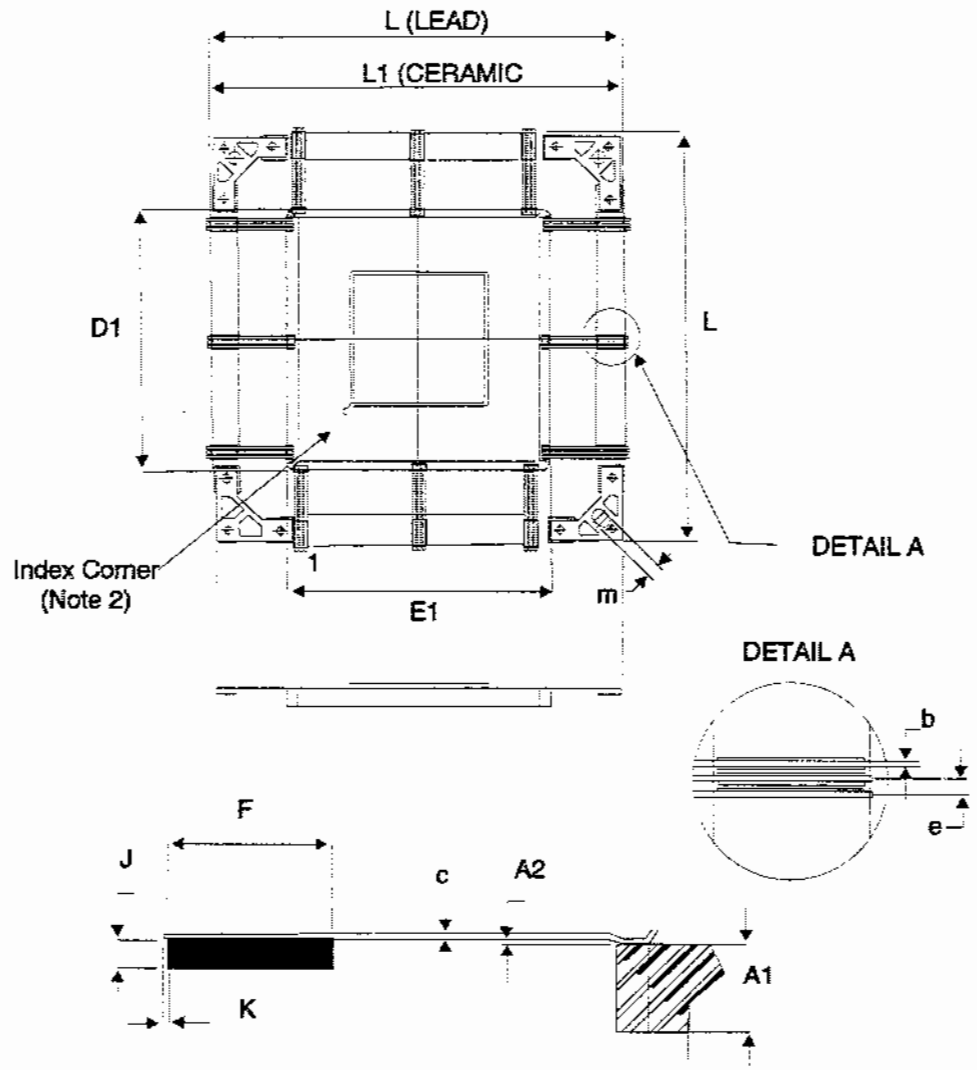
1.7.2 Multilayer Quad Flat Package (MQFP-F256) - 256 Flat Leads



Symbols	Dimensions mm		Notes
	Min	Max	
A	2.41	3.18	
A1	2.06	2.56	
A2	0.05	0.36	
c	0.1	0.2	1
D/E	53.23	55.74	
D1/E1	36.83	37.34	
e	0.508 BSC		1
f	0.15	0.25	1
L	8.2	9.2	1
N1/N2	64		Each side

NOTES:
1. Applies to all leads.
2. Terminal identification is specified by reference to the index corner as shown.

1.7.3 Multilayer Quad Flat Package (MQFP-T352) - 352 Tied Leads



Symbols	Dimensions mm		Notes
	Min	Max	
A1	2.35	3.15	
A2	0.05	0.35	
b	0.19	0.25	1
c	0.11	0.2	1
D1/E1	47.52	48.48	
e	0.50 BSC		1
F	4.5	5.5	
G	2.5	2.6	
J	0.75	1.05	

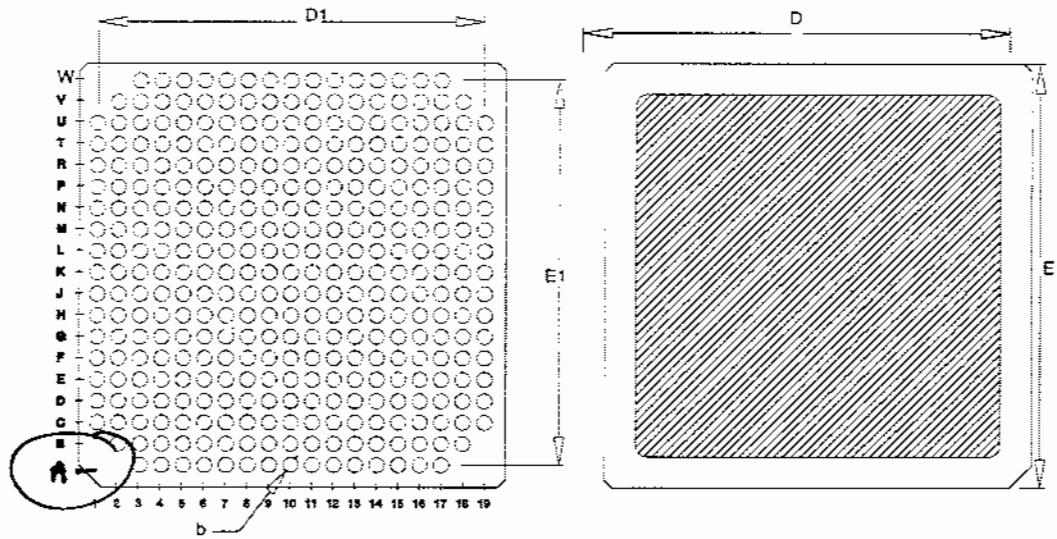
Symbols	Dimensions mm		Notes
	Min	Max	
K	-	0.5	1
L	74.85	76.4	
L1	74.6	75.4	
m	2.5	2.65	
N1/N2	88		Each side

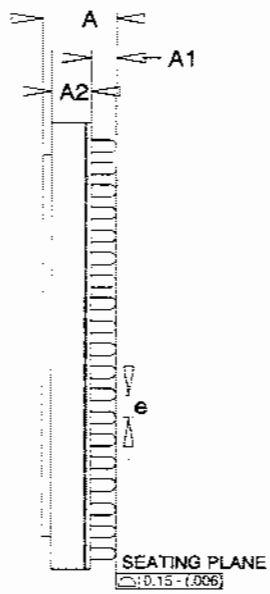
NOTES:
1. Applies to all leads.
2. Terminal identification is specified by reference to the index corner as shown.

1.7.4 Multilayer Column Grid Array (MCGA-349) - 349 Columns

BOTTOM VIEW

TOP VIEW



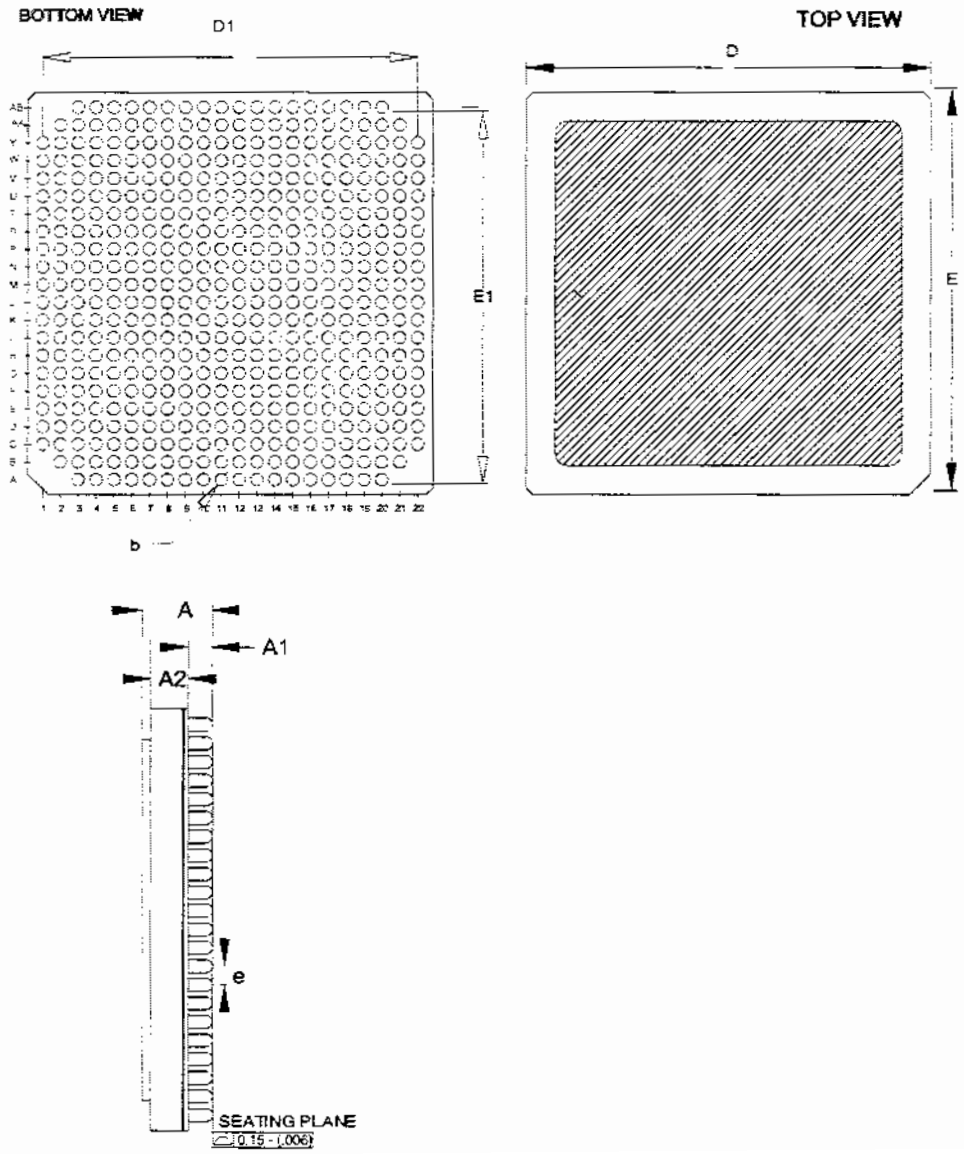


Symbols	Dimensions mm		Notes
	Min	Max	
A	4.3	5.9	
A1	1.4	1.85	
A2	2.4	3.45	
b	0.79	0.99	1

Symbols	Dimensions mm		Notes
	Min	Max	
D/E	24.8	25.2	
D1/E1	22.86		
e	1.27 BSC		1

NOTES:
1. Applies to all columns.
2. Terminal identification is specified by reference to the index corner as shown.

1.7.5 Multilayer Column Grid Array (MCGA-472) - 472 Columns



Symbols	Dimensions mm		Notes
	Min	Max	
A	4.3	5.9	
A1	1.4	1.85	
A2	2.6	3.45	
b	0.79	0.99	1
D/E	28.77	29.23	
D1/E1	26.67		
e	1.27 BSC		1

NOTES:
1. Applies to all columns.
2. Terminal identification is specified by reference to the index corner as shown.

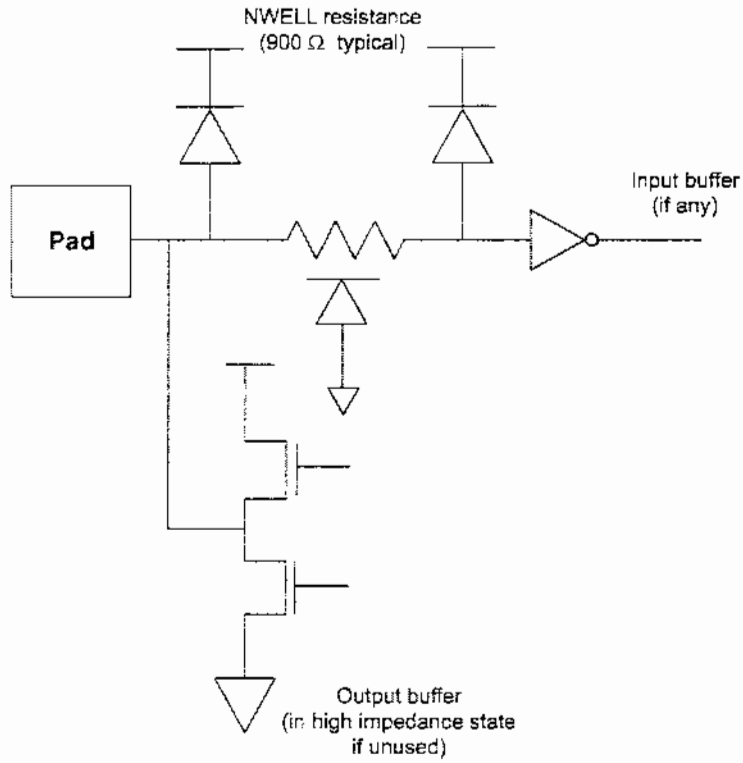
1.8 FUNCTIONAL DIAGRAM
See ASIC Sheet.

NOTES:
1. For all packages the lid is internally connected to the ground terminal as specified in the ASIC Sheet.

1.9 PIN ASSIGNMENT
See ASIC Sheet.

1.10 INSTRUCTION SET AND TIMING DIAGRAMS
See ASIC Sheet.

1.11 PROTECTION NETWORK



2. REQUIREMENTS

2.1 GENERAL

The complete requirements for procurement of the components specified herein are as stated in this specification and the ESCC Generic Specification. Permitted deviations from the Generic Specification, applicable to this specification only, are listed below.

Permitted deviations from the Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESCC requirement and do not affect the component's reliability, are listed in the appendices attached to this specification.

2.1.1 Deviations from the Generic Specification

2.1.1.1 Deviations from Screening Tests

High Temperature Reverse Bias Burn-in shall not be performed.

2.2 MARKING

The marking shall be in accordance with the requirements of ESCC Basic Specification No. 21700 and

as follows.

As a minimum the information to be marked on the component shall be:

(a) The ESCC qualified components symbol (for ESCC qualified components only).
(b) The ESCC Component Number.
(c) Traceability information.

The complete marking shall be as specified in the ASIC Sheet.

2.3 ELECTRICAL MEASUREMENTS AT ROOM, HIGH AND LOW TEMPERATURES

Electrical measurements shall be performed at room, high and low temperatures. Consolidated notes are given after the tables.

2.3.1 Room Temperature Electrical Measurements

The measurements shall be performed at T_{amb} = +22 ± 3°C.

2.3.1.1 Room Temperature Electrical Measurements for Components Specified at Single Supply Voltage V_{DD} = 2.5V

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1 (V_{DD} = 2.5 ± 0.2V)	Limits		Units
				Min	Max	
Functional Test 1	-	3014	See ASIC Sheet V_{DD}=2.3V	-	-	-
Functional Test 2	-	3014	See ASIC Sheet V_{DD}=2.5V	-	-	-
Functional Test 3	-	3014	See ASIC Sheet V_{DD}=2.7V	-	-	-
Supply Current, Stand-by	I_{DDSB}	3005	See ASIC Sheet			mA
Supply Current, Operating	I_{DDOP}	3005	See ASIC Sheet			mA
Low Level Input Current	I_{IL}	3009	V_{IN}=V_{SS}, CMOS Buffers	-	-1	µA
Low Level Input Current, Pull-up Resistor PRU1	I_{ILPU}	3009	V_{IN}=V_{SS}, CMOS Buffers Note 2	70	230	µA
Low Level Input Current, Pull-down Resistor PRD1	I_{ILPD}	3009	V_{IN}=V_{SS}, CMOS Buffers Note 2	-	±5	µA
High Level Input Current	I_{IH}	3010	V_{IN}=V_{DD}, CMOS Buffers	-	1	µA
High Level Input Current, Pull-up Resistor PRU1	I_{IHPU}	3010	V_{IN}=V_{DD}, CMOS Buffers Note 2	-	±5	µA

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1 (V_{DD} = 2.5 ± 0.2V)	Limits		Units
				Min	Max	
High Level Input Current, Pull-down Resistor PRD1	I_{IHPD}	3010	$V_{IN}=V_{DD}$, CMOS Buffers Note 2	70	540	µA
Output Leakage Current Third State, Low Level Applied	I_{OZL}	3020	V_{OUT}=0V, All Buffers V_{DD}=2.7V	-	-1	µA
Output Leakage Current Third State, High Level Applied	I_{OZH}	3021	V_{OUT}=0V, All Buffers V_{DD}=2.7V	-	1	µA
Input Current, Cold Sparing	I_{ICS}	-	V_{IN}=0V to 2.7V, PICZ Buffers $V_{DD}=V_{SS}$=0V	-	±2	µA
Output Current, Cold Sparing	I_{OCS}	-	V_{OUT}=0V to 2.7V, PO11Z Buffers $V_{DD}=V_{SS}$=0V	-	±2	µA
Low Level Output Voltage	V_{OL}	3007	V_{DD}=2.3V, I_{OL}=800µA PO11 Buffers Note 3	-	~~0.4~~ 400	~~V~~ mV
High Level Output Voltage	V_{OH}	3006	V_{DD}=2.3V, I_{OH}=-600µA PO11 Buffers Note 4	2	-	V
Output Short Circuit Current, to V_{DD}	I_{OSN}	-	PO11 output at High Level shorted to V_{DD} Note 5	-	15	mA
Output Short Circuit Current, to V_{SS}	I_{OSP}	-	PO11 output at High Level shorted to V_{SS} Note 5	-	8	mA
Input Capacitance	C_{IN}	3012	Note 5	-	2.4	pF
Output Capacitance	C_{OUT}	3012	Note 5	-	5.6	pF
Input/Output Capacitance	$C_{I/O}$	3012	Note 5	-	6.6	pF
Timings	-	3003	See ASIC Sheet			ns
Low Level Input Voltage	V_{IL}	-	CMOS Buffers V_{DD} = 2.3V	-	690	mV
High Level Input Voltage	V_{IH}	-	CMOS Buffers V_{DD} = 2.7V	1.89	-	V
Positive Trigger Threshold Voltage	V_{TP}	-	Note 5	1.06	1.61	V
Negative Trigger Threshold Voltage	V_{TN}	-	Note 5	0.78	1.25	V
Hysteresis Voltage	V_H	-	Note 5	250	-	mV

2.3.1.2 *Room Temperature Electrical Measurements for Components Specified at Single Supply Voltage V_{DD} = 3V*

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1 (V_{DD} = 3 ± 0.3V)	Limits		Units
				Min	Max	
Functional Test 1	-	3014	See ASIC Sheet V_{DD}=2.7V	-	-	-
Functional Test 2	-	3014	See ASIC Sheet V_{DD}=3V	-	-	-
Functional Test 3	-	3014	See ASIC Sheet V_{DD}=3.3V	-	-	-
Supply Current, Stand-by	I_{DDSB}	3005	See ASIC Sheet			mA
Supply Current, Operating	I_{DDOP}	3005	See ASIC Sheet			mA
Low Level Input Current	I_{IL}	3009	V_{IN}=V_{SS}, CMOS Buffers	-	-1	µA
Low Level Input Current, Pull-up Resistor PRU1	I_{ILPU}	3009	V_{IN}=V_{SS}, CMOS Buffers Note 2	108	330	µA
Low Level Input Current, Pull-down Resistor PRD1	I_{ILPD}	3009	V_{IN}=V_{SS}, CMOS Buffers Note 2	-	±5	µA
High Level Input Current	I_{IH}	3010	V_{IN}=V_{DD}, CMOS Buffers	-	1	µA
High Level Input Current, Pull-up Resistor PRU1	I_{IHPU}	3010	V_{IN}=V_{DD}, CMOS Buffers Note 2	-	±5	µA
High Level Input Current, Pull-down Resistor PRD1	I_{IHPD}	3010	V_{IN}=V_{DD}, CMOS Buffers Note 2	108	825	µA
Output Leakage Current Third State, Low Level Applied	I_{OZL}	3020	V_{OUT}=0V, All Buffers V_{DD}=3.3V	-	-1	µA
Output Leakage Current Third State, High Level Applied	I_{OZH}	3021	V_{OUT}=0V, All Buffers V_{DD}=3.3V	-	1	µA
Input Current, Cold Sparing	I_{ICS}	-	V_{IN}=0V to 3.3V, PICZ Buffers V_{DD}=V_{SS}=0V	-	±2	µA
Output Current, Cold Sparing	I_{OCS}	-	V_{OUT}=0V to 3.3V, PO11X Buffers V_{DD}=V_{SS}=0V	-	±2	µA

* → see attached.

*
Para 2.3.1.2 (P21)

Low Level Input Voltage	V_{IL}	–	CMOS Buffers $V_{DD} = 2.7V$	–	800	mV
High Level Input Voltage	V_{IH}	–	CMOS Buffers $V_{DD} = 3.3V$	2	–	V
Positive Trigger Threshold Voltage	V_{TP}	–	Note 5	1.25	1.93	V
Negative Trigger Threshold Voltage	V_{TN}	–	Note 5	0.9	1.42	V
Hysteresis Voltage	V_H	–	Note 5	0.31	–	mV

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1 (V_{DD} = 3 ± 0.3V)	Limits		Units
				Min	Max	
Low Level Output Voltage	V_{OL}	3007	V_{DD}=2.7V, I_{OL}=1mA PO11 Buffers Note 3	-	~~0.4~~ 400	~~V~~ mV
High Level Output Voltage	V_{OH}	3006	V_{DD}=2.7V, I_{OH}=-800µA PO11 Buffers Note 4	2.4	-	V
Output Short Circuit Current, to V_{DD}	I_{OSN}	-	PO11 output at High Level shorted to V_{DD} Note 5	-	21	mA
Output Short Circuit Current, to V_{SS}	I_{OSP}	-	PO11 output at High Level shorted to V_{SS} Note 5	-	12	mA
Input Capacitance	C_{IN}	3012	Note 5	-	2.4	pF
Output Capacitance	C_{OUT}	3012	Note 5	-	5.6	pF
Input/Output Capacitance	$C_{I/O}$	3012	Note 5	-	6.6	pF
Timings	-	3003	See ASIC Sheet			ns

2.3.1.3 *Room Temperature Electrical Measurements for Components Specified at Single Supply Voltage V_{DD} = 3.3V*

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1 (V_{DD} = 3.3 ± 0.3V)	Limits		Units
				Min	Max	
Functional Test 1	-	3014	See ASIC Sheet V_{DD}=3V	-	-	-
Functional Test 2	-	3014	See ASIC Sheet V_{DD}=3.3V	-	-	-
Functional Test 3	-	3014	See ASIC Sheet V_{DD}=3.6V	-	-	-
Supply Current, Stand-by	I_{DDSB}	3005	See ASIC Sheet			mA
Supply Current, Operating	I_{DDOP}	3005	See ASIC Sheet			mA
Low Level Input Current	I_{IL}	3009	V_{IN}=V_{SS}, CMOS Buffers	-	-1	µA
Low Level Input Current, Pull-up Resistor PRU1	I_{ILPU}	3009	V_{IN}=V_{SS}, CMOS Buffers Note 2	120	400	µA

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1 (V_{DD} = 3.3 ± 0.3V)	Limits		Units
				Min	Max	
Low Level Input Current, Pull-down Resistor PRD1	I_{ILPD}	3009	$V_{IN}=V_{SS}$, CMOS Buffers Note 2	-	±5	µA
High Level Input Current	I_{IH}	3010	$V_{IN}=V_{DD}$, CMOS Buffers	-	1	µA
High Level Input Current, Pull-up Resistor PRU1	I_{IHPU}	3010	$V_{IN}=V_{DD}$, CMOS Buffers Note 2	-	±5	µA
High Level Input Current, Pull-down Resistor PRD1	I_{IHPD}	3010	$V_{IN}=V_{DD}$, CMOS Buffers Note 2	150	900	µA
Output Leakage Current Third State, Low Level Applied	I_{OZL}	3020	V_{OUT}=0V, All Buffers V_{DD}=3.6V	-	-1	µA
Output Leakage Current Third State, High Level Applied	I_{OZH}	3021	V_{OUT}=0V, All Buffers V_{DD}=3.6V	-	1	µA
Input Current, Cold Sparing	I_{ICS}	-	V_{IN}=0V to 3.6V, PICZ Buffers $V_{DD}=V_{SS}$=0V	-	±2	µA
Output Current, Cold Sparing	I_{OCS}	-	V_{OUT}=0V to 3.6V, PO11Z Buffers $V_{DD}=V_{SS}$=0V	-	±2	µA
Low Level Output Voltage	V_{OL}	3007	V_{DD}=3V I_{OL}=2mA PO11 Buffers Note 3	-	~~0.4~~ 400	~~V~~ mV
High Level Output Voltage	V_{OH}	3006	V_{DD}=3V I_{OL}=-1.8mA PO11 Buffers Note 4	2.4	-	V
Output Short Circuit Current, to V_{DD}	I_{OSN}	-	PO11 output at High Level shorted to V_{DD} Note 5	-	23	mA
Output Short Circuit Current, to V_{SS}	I_{OSP}	-	PO11 output at High Level shorted to V_{SS} Note 5	-	13	mA
Input Capacitance	C_{IN}	3012	Note 5	-	2.4	pF
Output Capacitance	C_{OUT}	3012	Note 5	-	5.6	pF
Input/Output Capacitance	$C_{I/O}$	3012	Note 5	-	6.6	pF

see attached →

* P 2.3.1.3 (P23)

Low Level Input Voltage	V_{IL}	–	CMOS Buffers V_{DD} = 3V	–	800	mV
High Level Input Voltage	V_{IH}	–	CMOS Buffers V_{DD} = 3.6V	2	–	V
Positive Trigger Threshold Voltage	V_{TP}	–	Note 5	1.4	2.08	V
Negative Trigger Threshold Voltage	V_{TN}	–	Note 5	0.99	1.51	V
Hysteresis Voltage	V_H	–	Note 5	370	–	mV

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1 (V_{DD} = 3.3 ± 0.3V)	Limits		Units
				Min	Max	
Timings	-	3003	See ASIC Sheet			ns

2.3.1.4 *Room Temperature Electrical Measurements for Components Specified for Bi-voltage Operation at V_{DD} = 2.5V, 3V or 3.3V and V_{CC} = 5V.*

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1 [V_{DD} = 2.5 ± 0.2V, 3 ± 0.3V, 3.3 ± 0.3V (Note ~~8~~ 6) V_{CC}=5 ± 0.5V (Note ~~9~~ 7)]	Limits		Units
				Min	Max	
Functional Test 1	-	3014	See ASIC Sheet V_{CC}=4.5V, V_{DD}=3V	-	-	-
Functional Test 2	-	3014	See ASIC Sheet V_{CC}=5V, V_{DD}=3.3V	-	-	-
Functional Test 3	-	3014	See ASIC Sheet V_{CC}=5.5V, V_{DD}=3.6V	-	-	-
Supply Current, Stand-by	I_{DDSB}	3005	See ASIC Sheet			mA
Supply Current, Operating	I_{DDOP}	3005	See ASIC Sheet			mA
Low Level Input Current	I_{IL}	3009	V_{IN}=V_{SS}, CMOS Buffers	-	-1	µA
Low Level Input Current, Pull-up Resistor PRU1	I_{ILPU}	3009	V_{IN}=V_{SS}, CMOS Buffers Note 2	180	690	µA
Low Level Input Current, Pull-down Resistor PRD1	I_{ILPD}	3009	V_{IN}=V_{SS}, CMOS Buffers Note 2	-	±5	µA
High Level Input Current	I_{IH}	3010	V_{IN}=V_{DD}, CMOS Buffers	-	1	µA
High Level Input Current, Pull-up Resistor PRU1	I_{IHPU}	3010	V_{IN}=V_{DD}, CMOS Buffers Note 2	-	±5	µA
High Level Input Current, Pull-down Resistor PRD1	I_{IHPD}	3010	V_{IN}=V_{DD}, CMOS Buffers Note 2	30	400	µA
Output Leakage Current Third State, Low Level Applied	I_{OZL}	3020	V_{OUT}=0V, All Buffers V_{DD}=3.6V	-	-1	µA

see attached →

P2.3.1.4 (P 24)

Low Level Input Voltage	V_{IL}	–	PICV, PICV5 Buffers $V_{DD} = V_{DD}^{min}$	–	800	mV
High Level Input Voltage	V_{IH}	–	PICV, PICV5 Buffers $V_{DD} = V_{DD}^{max}$	2	–	V
Positive Trigger Threshold Voltage	V_{TP}	–	Note 5	1.4	2.08	V
Negative Trigger Threshold Voltage	V_{TN}	–	Note 5	0.99	1.51	V
Hysteresis Voltage	V_H	–	Note 5	370	–	mV

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1 [V_{DD} = 2.5 ± 0.2V, 3 ± 0.3V, 3.3 ± 0.3V (Note 6) V_{CC}=5 ± 0.5V (Note 7)]	Limits		Units
				Min	Max	
Output Leakage Current Third State, High Level Applied	I_{OZH}	3021	V_{OUT}=0V, All Buffers V_{DD}=3.6V	-	1	µA
Input Current, Cold Sparing	I_{ICS}	-	V_{IN}=0V to 3.6V, PICZ Buffers V_{DD}=V_{SS}=0V	-	±2	µA
Output Current, Cold Sparing	I_{OCS}	-	V_{OUT}=0V to 3.6V, PO11Z Buffers V_{DD}=V_{SS}=0V	-	±2	µA
Low Level Output Voltage	V_{OL}	3007	V_{DD}=V_{DD}min, V_{CC}=4.5V	-	~~0.4~~ 400	~~V~~ mV
High Level Output Voltage	V_{OH}	3006	V_{DD}=V_{DD}min(2.5V), V_{CC}=4.5V	2	-	V
			V_{DD}=V_{DD}min(3V, 3.3V), V_{CC}=4.5V	2.4	-	V
Output Short Circuit Current, to V_{DD}	I_{OSN}	-	PO11 output at High Level shorted to V_{DD} Note 5	-	28	mA
Output Short Circuit Current, to V_{SS}	I_{OSP}	-	PO11 output at High Level shorted to V_{SS} Note 5	-	17	mA
Input Capacitance	C_{IN}	3012	Note 5	-	2.4	pF
Output Capacitance	C_{OUT}	3012	Note 5	-	5.6	pF
Input/Output Capacitance	$C_{I/O}$	3012	Note 5	-	6.6	pF
Timing	-	3003	See ASIC Sheet			ns

2.3.2 Notes to Electrical Measurements Tables

1. Unless otherwise specified: all inputs and outputs shall be tested for each characteristic; Inputs not under test shall be V_{IN} = V_{SS}, V_{CC} or V_{DD} and outputs not under test shall be open; V_{SS} = 0V.

2. Standard pull-ups: PRU# where # = [1-31] index for Ron:
   Ron = # x R0 = 19kΩ typical (12 to 30kΩ) in 2.5V range.
   Ron = # x R0 = 15kΩ typical (10 to 25kΩ) in 3V range.
   Ron = # x R0 = 14kΩ typical (9 to 25kΩ) in 3.3V range.
   5V tolerant/compliant pull-ups: PRU# where # = [1-31] index for Ron:
   Ron = # x R0 = 14kΩ typical (8 to 25kΩ) in each range.

   Standard pull-downs: PRD# where # = [1-31] index for Ron:
   Ron = # x R0 = 11kΩ typical (5 to 30kΩ) in 2.5V range.
   Ron = # x R0 = 9kΩ typical (4 to 25kΩ) in 3V range.

Ron = # x R0 = 8kΩ typical (4 to 20kΩ) in 3.3V range.
5V tolerant/compliant pull-downs: PRD# where # = [1-31] index for Ron:
Ron = # x R0 = 36kΩ typical (17 to 80kΩ) in 2.5V range.
Ron = # x R0 = 23kΩ typical (11 to 55kΩ) in 3V range.
Ron = # x R0 = 19kΩ typical (9 to 45kΩ) in 3.3V range.

3. Output buffers: PO$# where
$ = [1-12] quantity of output driving capability of p-channels.
#=[1-12] quantity of output driving capability of n-channels.
Standard buffers (including cold sparing)
IO = 1.6, 1.8, 2mA measured at V_{OL} = ~~0.4~~, ~~0.4~~, ~~0.4~~V in 2.5, 3, 3.3V range respectively.
Tolerance buffers (including cold sparing)
IO = 1, 1.3, 1.4mA measured at V_{OL} = ~~0.4~~, ~~0.4~~, ~~0.4~~V in 2.5, 3, 3.3V range respectively.
Compliant buffers (V_{CC} = 4.5V)
IO = 1.1, 1.4, 1.6mA measured at V_{OL} = ~~0.4~~, ~~0.4~~, ~~0.4~~V in 2.5, 3, 3.3V range respectively.
400, 400, 400mV

4. Output buffers: PO$# where
$ = [1-12] quantity of output driving capability of p-channels.
#=[1-12] quantity of output driving capability of n-channels.
Standard buffers (including cold sparing)
IO = -1.6, -1.8, -2mA measured at V_{OL} = 2, 2.4, 2.4V in 2.5, 3, 3.3V range respectively.
Tolerance buffers (including cold sparing)
IO = -1, -1.3, -1.4mA measured at V_{OL} = 2, 2.4, 2.4V in 2.5, 3, 3.3V range respectively.
Compliant buffers (V_{CC} = 4.5V)
IO = -1.1, -1.4, -1.6mA measured at V_{OL} = 2, 2.4, 2.4V in 2.5, 3, 3.3V range respectively.

5. Guaranteed but not tested.

~~U. Variants 01 to 13 and 27 to 39.~~

~~V. Variants 14 to 26 and 40 to 52.~~

6 ~~S~~. 5V tolerant buffers.

7 ~~9~~. 5V compliant buffers.

2.3.3 High and Low Temperatures Electrical Measurements

Unless otherwise specified the measurements shall be performed at T_{amb} = +125 (+0 -5)°C and T_{amb} = -55 (+5 - 0)°C. Unless otherwise specified the characteristics, test methods, conditions and limits shall be the same as specified for Room Temperature Electrical Measurements.

2.4 PARAMETER DRIFT VALUES

Unless otherwise specified, the measurements shall be performed at T_{amb} = +22 ± 3°C.

The test methods and test conditions shall be as per the corresponding test defined in Room Temperature Electrical Measurements.

The drift values (Δ) shall not be exceeded for each characteristic specified. The corresponding absolute limit values for each characteristic shall not be exceeded.

Characteristics	Symbols	Limits			Units
		Drift Value Δ	Absolute		
			Min	Max	
Supply Current, Stand-by	I_{DDSB}	See ASIC Sheet			mA
Low Level Input Current	I_{IL}	±0.1	-	-1	µA
High Level Input Current	I_{IH}	±0.1	-	1	µA
Output Leakage Current Third State, Low Level Applied	I_{OZL}	±0.1	-	-1	µA
Output Leakage Current Third State, High Level Applied	I_{OZH}	±0.1	-	1	µA
Low Level Output Voltage	V_{OL}	±0.1	-	400	mV
High Level Output Voltage	V_{OH}	±0.1	2.4 or 2	-	V

NOTES:
1. Unless otherwise specified all inputs and outputs shall be tested for each characteristic.

2.5 INTERMEDIATE AND END-POINT ELECTRICAL MEASUREMENTS

Unless otherwise specified, the measurements shall be performed at T_{amb} = +22 ± 3°C. Unless otherwise specified the characteristics, test methods, conditions and limits shall be the same as specified for Room Temperature Electrical Measurements.

2.6 POWER BURN-IN CONDITIONS

See ASIC Sheet.

2.7 OPERATING LIFE CONDITIONS

Unless otherwise specified the conditions shall be as specified for Power Burn-in.

2.8 TOTAL DOSE RADIATION TESTING

2.8.1 Bias Conditions and Total Dose Level for Total Dose Radiation Testing

Continuous bias shall be applied during irradiation testing as specified in the ASIC Sheet.

The total dose level applied shall be as specified in the component type variant information herein, in the ASIC Sheet or in the Purchase Order.

2.8.2 Electrical Measurements for Total Dose Radiation Testing

Prior to irradiation testing the devices shall have successfully met Room Temperature Electrical Measurements specified herein.

Unless otherwise stated the measurements shall be performed at T_{amb} = +22 ± 3°C.
The test methods and test conditions shall be as per the corresponding test defined in Room Temperature Electrical Measurements.

The parameters to be measured during and on completion of irradiation testing are specified in the ASIC Sheet.