DOCUMENT CHANGE REQUEST

DCR number 371	Changes required for: N/A	Originator: andre UGUEN
Date: 2007/07/25	Date sent: 2007/07/25	Organisation:
Status: IMPLEMENTED		

Title:	CMOS 8-Stage Shift and Store Bus Register with Synchronous Serial Outputs and 3-State Parallel		
Number:	9306/026	Issue:	2

Other documents affected:

Page:

1.10 TRUTH TABLE AND TIMING DIAGRAM
page 14

Paragraph:

1.10 TRUTH TABLE AND TIMING DIAGRAM
page 14

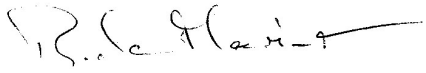
Original wording:

Proposed wording:

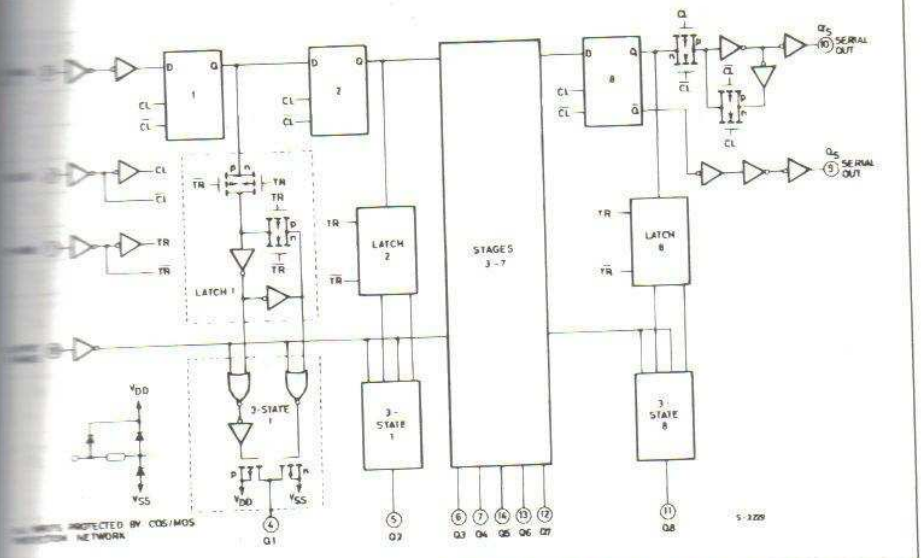
timing diagram is wrong.

Justification:

during migration from old ESA/SCC form to ESCC form, the diagram was copied and an error was introduiced: the second negative pulse of STR shall start at the next falling front of CLK (in the same time as OE).
Good diagram is proposed in attached file

Attachments:
diagram_HCC4094.pdf, null
Modifications:
N/A
Approval signature:

Date signed:
2007-07-25

DIAGRAMS



G DIAGRAM