DOCUMENT CHANGE REQUEST

DCR number 490	Changes required for: General	Originator: S Jeffery - ESCC
Date: 2009/04/14	Date sent: 2009/04/14	Organisation: ESA/ESTEC
Status: IMPLEMENTED		

Title:	Transistors Low Power NPN, based on type 2N2484		
Number:	5201/001	Issue:	4

Other documents affected:

Page:

See attachment

Paragraph:

See attachment

Original wording:

Proposed wording:

Various editorial and technical changes as detailed in the attachment, which are required to make this detail spec clear, complete and consistent with the standard format and content of specifications for similar Part Types. Note that this DCR replaces the withdrawn DCR 458.

Justification:

Improve the appearance, content and clarity of the spec.

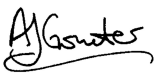
Attachments:

5201001_Issue_5_-_Draft_B.pdf, null

Modifications:

N/A

Approval signature:



Date signed:

2009-04-14

TRANSISTORS, LOW POWER, NPN

BASED ON TYPE 2N2484

ESCC Detail Specification No. 5201/001

as applicable

Issue ~~4~~ 5 - Draft B	~~December 2008~~

Document Custodian: European Space Agency - see https://escies.org

as applicable

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DOCUMENTATION CHANGE NOTICE

(Refer to https://escies.org for ESCC DCR content)

DCR No.	CHANGE DESCRIPTION
~~428, 447~~ tbd	Specification up issued to incorporate editorial and technical changes per DCR.

1.5 MAXIMUM RATINGS

The maximum ratings shall not be exceeded at any time during use or storage.

Maximum ratings shall only be exceeded during testing to the extent specified in this specification and when stipulated in Test Methods and Procedures of the ESCC Generic Specification.

Characteristics	Symbols	Maximum Ratings	Unit	Remarks
Collector-Base Voltage	V_{CBO}	60	V	Over entire operating temperature range
Collector-Emitter Voltage	V_{CEO}	60	V	
Emitter-Base Voltage	V_{EBO}	6	V	
Collector Current	I_C	50	mA	Continuous
Power Dissipation For TO-18 and CCP	P_{tot1}	0.36	W	At $T_{amb} \leq +25^{\circ}C$ ~~Note 1~~
~~For CCP~~	~~P_{tot2}~~	~~0.73 (Note 2)~~	~~W~~	
For TO-18	P_{tot2}	1.2	W	At $T_{case} \leq +25^{\circ}C$ ~~Note 1~~
Operating Temperature Range	T_{op}	-65 to +200	°C	Note 2
Storage Temperature Range	T_{stg}	-65 to +200	°C	Note 2
Soldering Temperature For TO-18 For CCP	T_{sol}	 +260 +245	°C	 Note 3 Note 4

See attached

o Symbol - make bigger

NOTES:

~~1. For T_{amb} or $T_{case} \geq +25^{\circ}C$, derate linearly to 0W at +200°C.~~

~~2. When mounted on a 15 x 15 x 0.6mm ceramic substrate.~~

, and any handling,

2. For Variants with tin-lead plating or hot solder dip lead finish all testing performed at $T_{amb} > +125^{\circ}C$ shall be carried out in a 100% inert atmosphere.

3. Duration 10 seconds maximum at a distance of not less than 1.5mm from the device body and the same lead shall not be resoldered until 3 minutes have elapsed.

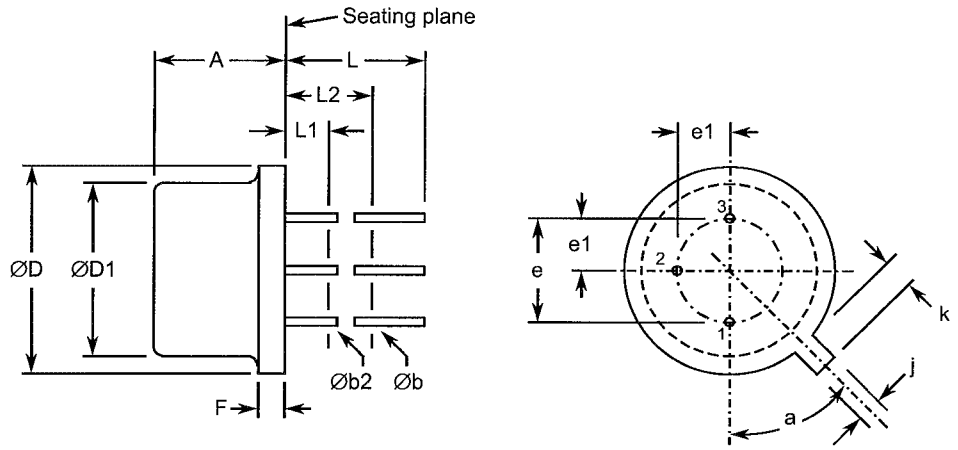
4. Duration 5 seconds maximum and the same terminal shall not be resoldered until 3 minutes have elapsed.

1. Thermal Resistance, Junction-to-Case only applies to TO-18 packaged Variants.

Thermal Resistance, Junction-to-Ambient	$R_{th(j-a)}$	486	°C/W	
Thermal Resistance, Junction-to-Case	$R_{th(j-c)}$	145.8	°C/W	Note 1

1.6 PHYSICAL DIMENSIONS AND TERMINAL IDENTIFICATION

1.6.1 Metal Can Package (TO-18) - 3 lead



note addition of horizontal lines

Symbols	Dimensions mm		Notes
	Min	Max	
A	4.32	5.33	
Øb	0.406	0.533	2, 3
Øb2	0.406	0.483	2, 3
ØD	5.31	5.84	
ØD1	4.52	4.95	
e	2.54 BSC		4
e1	1.27 BSC		4
F	-	0.762	
j	0.914	1.17	
k	0.711	1.22	5
L	12.7	-	2
L1	-	1.27	3
L2	6.35	-	3
a	45° BSC		1, 4, 6

NOTES:

1. Terminal identification is specified by reference to the tab position where lead 1 = emitter, lead 2 = base, lead 3 = collector.
2. Applies to all leads.
3. Øb2 applies between L1 and L2. Øb applies between L2 and 12.7mm from the seating plane. Diameter is uncontrolled within L1 and beyond12.7mm from the seating plane.
4. Leads having maximum diameter 0.483mm measured in the gauging plane 1.37(+0.025,-0)mm

2.4.2 High and Low Temperatures Electrical Measurements

Characteristics	Symbols	MIL-STD-750 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Collector-Base Cut-off Current	I_{CBO}	3036	T_{amb}=+150(+0-5)°C V_{CB}=45V, Bias Condition D	-	10	µA
Forward-Current Transfer Ratio 2	h_{FE2}	3076	T_{amb}=-55(+5-0)°C V_{CE}=5V I_C=10µA	20	-	-

NOTES:
1. Read and record measurements shall be performed on a sample of 5 components with 0 failures allowed. Alternatively a 100% inspection may be performed.

2.5 PARAMETER DRIFT VALUES

Unless otherwise specified, the measurements shall be performed at T_{amb}=+22 ±3°C.

The test methods and test conditions shall be as per the corresponding test defined in Room Temperature Electrical Measurements.

The drift values (Δ) shall not be exceeded for each characteristic specified. The corresponding absolute limit values for each characteristic shall not be exceeded.

Characteristics	Symbols	Limits			Units
		Drift Value Δ	Absolute		
			Min	Max	
Collector-Base Cut-off Current	I_{CBO}	±5 or (1) ±100%	-	10	nA
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$	±30 or (1) ±15%	-	350	mV
Forward-Current Transfer Ratio 4	h_{FE4}	±15%	250	650	-

NOTES:
1. Whichever is the greater referred to the initial value.

2.6 INTERMEDIATE AND END-POINT ELECTRICAL MEASUREMENTS

Unless otherwise specified, the measurements shall be performed at T_{amb}=+22 ±3°C.

The test methods and test conditions shall be as per the corresponding test defined in Room Temperature Electrical Measurements.

The limit values for each characteristic shall not be exceeded.

Characteristics	Symbols	Limits		Units
		Min	Max	
Collector-Base Cut-off Current	I_{CBO}	-	10	nA
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$	-	350	mV
Forward-Current Transfer Ratio 4	h_{FE4}	250	650	-

2.7 POWER BURN-IN CONDITIONS

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	T_{amb}	+20 to +50	°C
Power Dissipation	P_{tot}	As per Maximum Ratings. P_{tot} derated at the chosen T_{amb}	W
Collector-Base Voltage	V_{CB}	27	V

Derate P_{tot1}

using the specified $R_{th(j-a)}$.

2.8 OPERATING LIFE CONDITIONS

The conditions shall be as specified for Power Burn-in.

APPENDIX 'A'

AGREED DEVIATIONS FOR STMICROELECTRONICS (F)

<table>
<tr><th>ITEMS AFFECTED</th><th>DESCRIPTION OF DEVIATIONS</th></tr>
<tr><td>Deviations from Production Control-Chart F2</td><td>Special In-Process Control Internal Visual Inspection.
For CCP packages the criteria specified for voids in the fillet and minimum die mounting material around the visible die perimeter for die mounting defects may be omitted providing that a radiographic inspection to verify the die-attach process is performed on a sample basis in accordance with STMicroelectronics procedure 0076637.</td></tr>
<tr><td>Deviations from Room Temperature Electrical Measurements</td><td>All AC characteristics (Room Temperature Electrical Measurement Note 2) may be considered guaranteed but not tested if successful pilot lot testing has been performed on the wafer lot which includes AC characteristic measurements per the Detail Specification.

A summary of the pilot lot testing shall be provided if required by the Purchase Order.

Characteristics h_{fe1}, and C_{ibo}, shall be as follows:
<table>
<tr><th rowspan="2">Characteristics</th><th rowspan="2">Symbols</th><th rowspan="2">MIL-STD-750 Test Method</th><th rowspan="2">Test Conditions</th><th colspan="2">Limits</th><th rowspan="2">Units</th></tr>
<tr><th>Min.</th><th>Max.</th></tr>
<tr><td>High Frequency Small Signal Current Gain 1</td><td>h_{fe1}</td><td>3306</td><td>V_{CE}=5V
I_C=50µA
f=5MHz
Note 2</td><td>1</td><td>-</td><td>-</td></tr>
<tr><td>Input Capacitance</td><td>C_{ibo}</td><td>3240</td><td>V_{EB}=500mV
I_C=0A
f=1MHz
Note 2</td><td>-</td><td>15</td><td>pF</td></tr>
</table></td></tr>
<tr><td>Deviations from High and Low Temperatures Electrical Measurements</td><td>All characteristics specified may be considered guaranteed but not tested if successful pilot lot testing has been performed on the wafer lot which includes characteristic measurements at high and low temperatures per the Detail Specification. A summary of the pilot lot testing shall be provided if required by the Purchase Order.</td></tr>
<tr><td>Deviations from Screening Tests - Chart F3</td><td>Solderability is not applicable unless specifically stipulated in the Purchase Order.</td></tr>
</table>