DOCUMENT CHANGE REQUEST

DCR number 491	Changes required for: General	Originator: S Jeffery - ESCC
Date: 2009/04/14	Date sent: 2009/04/14	Organisation: ESA/ESTEC
Status: IMPLEMENTED		

Title:	Transistors Low Power PNP, based on type 2N2907A		
Number:	5202/001	Issue:	4

Other documents affected:

Page:

See attachment

Paragraph:

See attachment

Original wording:

Proposed wording:

Various editorial and technical changes as detailed in the attachment, which are required to make this detail spec clear, complete and consistent with the standard format and content of specifications for similar Part Types. Note that this DCR replaces the withdrawn DCR 460.

Justification:

Improve the appearance, content and clarity of the spec.

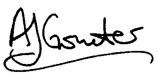
Attachments:

5202001_Issue_5_-_Draft_B.pdf, null

Modifications:

N/A

Approval signature:



Date signed:

2009-04-14

European Space Components Coordination

Pages 1 to 16

TRANSISTORS, LOW POWER, PNP

BASED ON TYPE 2N2907A

ESCC Detail Specification No. 5202/001

as applicable

Issue ~~4~~ 5 - Draft B	~~December 2008~~

esa

Document Custodian: European Space Agency - see https://escies.org

as applicable

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DOCUMENTATION CHANGE NOTICE

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DCR No.	CHANGE DESCRIPTION
~~423, 447~~ tbd	Specification up issued to incorporate editorial and technical changes per DCR.

1.5 MAXIMUM RATINGS

The maximum ratings shall not be exceeded at any time during use or storage.

Maximum ratings shall only be exceeded during testing to the extent specified in this specification and when stipulated in Test Methods and Procedures of the ESCC Generic Specification.

Characteristics	Symbols	Maximum Ratings	Unit	Remarks
Collector-Base Voltage	V_{CBO}	-60	V	Over entire operating temperature range
Collector-Emitter Voltage	V_{CEO}	-60	V	
Emitter-Base Voltage	V_{EBO}	-5	V	
Collector Current For TO-18 For CCP	I_C	 -600 -500	mA	Continuous
Power Dissipation For TO-18 and CCP	P_{tot1}	0.4	W	At $T_{amb} \leq +25^{\circ}C$ ~~Note 1~~
~~For CCP~~	P_{tot2}	0.73 (Note 2)	W	
For TO-18	P_{tot} 2.	1.8	W	At $T_{case} \leq +25^{\circ}C$ ~~Note 1~~
Operating Temperature Range	T_{op}	-65 to +200	°C	Note ~~3~~ 2
Storage Temperature Range	T_{stg}	-65 to +200	°C	Note ~~3~~ 2
Soldering Temperature For TO-18 For CCP	T_{sol}	 +260 +245	°C	 Note ~~4~~ 3 Note ~~5~~ 4

See attached

Symbol - make bigger

NOTES:

~~1. For T_{amb} or T_{case} > +25°C, derate linearly to 0W at +200°C.~~

~~2. When mounted on a 15 x 15 x 0.6mm ceramic substrate.~~

, and any handling,

2. ~~3.~~ For Variants with tin-lead plating or hot solder dip lead finish all testing performed at T_{amb} > +125°C shall be carried out in a 100% inert atmosphere.

3. ~~4.~~ Duration 10 seconds maximum at a distance of not less than 1.5mm from the device body and the same lead shall not be resoldered until 3 minutes have elapsed.

4. ~~5.~~ Duration 5 seconds maximum and the same terminal shall not be resoldered until 3 minutes have elapsed.

[1. Thermal Resistance, Junction-to-Case only applies to TO-18 packaged Variants.

Thermal Resistance, Junction-to-Ambient	$R_{th(j-a)}$	437.5	°C/W	
Thermal Resistance, Junction-to-Case	$R_{th(j-c)}$	97.2	°C/W	Note 1

Characteristics	Symbols	Limits		Units
		Min	Max	
Collector-Base Cut-off Current	I_{CBO}	-	-10	nA
Forward-Current Transfer Ratio 3	h_{FE3}	100	300	-
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$	-	-400	mV

2.7 HIGH TEMPERATURE REVERSE BIAS BURN-IN CONDITIONS

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	T_{amb}	+150 (+0 -5)	°C
Collector-Base Voltage	V_{CB}	-50	V
Duration	t	48 minimum	Hours

2.8 POWER BURN-IN CONDITIONS

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	T_{amb}	+20 to +50	°C
Power Dissipation	P_{tot}	As per Maximum Ratings, ~~P_{tot} derated~~ at the chosen T_{amb} using the specified $R_{th(j-a)}$.	W
Collector-Base Voltage	V_{CB}	40	V

Derate P_{tot}

2.9 OPERATING LIFE CONDITIONS

The conditions shall be as specified for Power Burn-in.

APPENDIX 'A'

AGREED DEVIATIONS FOR STMICROELECTRONICS (F)

ITEMS AFFECTED	DESCRIPTION OF DEVIATIONS
Deviations from Production Control-Chart F2	Special In-process Control Internal Visual Inspection. For CCP packages the criteria specified for voids in the fillet and minimum die mounting material around the visible die perimeter for die mounting defects may be omitted providing that a radiographic inspection to verify the die-attach process is performed on a sample basis in accordance with STMicroelectronics procedure 0076637.
Deviations from Room Temperature Electrical Measurements	All AC characteristics (Room Temperature Electrical Measurement Note 2) may be considered guaranteed but not tested if successful pilot lot testing has been performed on the wafer lot which includes AC characteristic measurements per the Detail Specification. A summary of the pilot lot testing shall be provided if required by the Purchase Order.
Deviations from High and Low Temperatures Electrical Measurements	All characteristics specified may be considered guaranteed but not tested if successful pilot lot testing has been performed on the wafer lot which includes characteristic measurements at high and low temperatures per the Detail Specification. A summary of the pilot lot testing shall be provided if required by the Purchase Order.
Deviations from Screening Tests - Chart F3	Solderability is not applicable unless specifically stipulated in the Purchase Order.