

## DOCUMENT CHANGE REQUEST

492 DCR number Changes required for: General Originator: S Jeffery - ESCC Date: 2009/04/14 Organisation: ESA/ESTEC Date sent: 2009/04/14 Status: IMPLEMENTED Title: Transistors Low Power PNP, based on type 2N5401 Number: 5202/014 Issue: 3 Other documents affected: Page: See attachment Paragraph: See attachment Original wording: Proposed wording: Various editorial and technical changes as detailed in the attachment, which are required to make this detail spec clear, complete and consistent with the standard format and content of specifications for similar Part Types. Note that this DCR replaces the withdrawn DCR 461. Justification: Improve the appearance, content and clarity of the spec. Attachments: 5202014\_Issue\_4\_-\_Draft\_B.pdf, null Modifications: N/A Approval signature: surtes Date signed: 2009-04-14

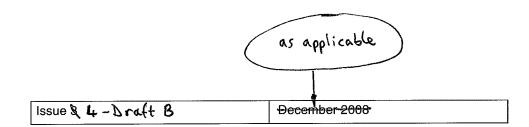


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# TRANSISTORS, LOW POWER, PNP

## **BASED ON TYPE 2N5401**

# **ESCC Detail Specification No. 5202/014**







as applicable

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## **DOCUMENTATION CHANGE NOTICE**

(Refer to https://escies.org for ESCC DCR content)

DCR No.	CHANGE DESCRIPTION
428 44	Specification up issued to incorporate editorial and technical changes per DCR.
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#### 1.5 MAXIMUM RATINGS

The maximum ratings shall not be exceeded at any time during use or storage.

Maximum ratings shall only be exceeded during testing to the extent specified in this specification and when stipulated in Test Methods and Procedures of the ESCC Generic Specification.

Characteristics	Symbols	Maximum Ratings	Unit	Remarks	
Collector-Base Voltage	V <sub>CBO</sub>	-160	V	Over entire	
Collector-Emitter Voltage	V <sub>CEO</sub>	-150	V	operating temperature	
Emitter-Base Voltage	V <sub>EBO</sub>	-5	V	range	
Collector Current For TO-18 For CCP	I <sub>C</sub>	-600 -500	mA	Continuous	
Power Dissipation For TO-18 and CCP	P <sub>tot1</sub>	0.36	» (	At T <sub>amb</sub> ≤ +25°C	
FOUCEBUSIN	ノダゲノ	) 0.58 (Note 2)	) W)	2000	
For TO-18	P <sub>tot</sub> s, 2.	1.2	W	At T <sub>case</sub> ≤ +25°C	
Operating Temperature Range	T <sub>op</sub>	-65 to +200	°C	Note 🖏 2	
Storage Temperature Range	T <sub>stg</sub>	-65 to +200	°C	Note & 2	
Soldering Temperature For TO-18 For CCP	T <sub>sol</sub>	+260 +245	°C	Note & 3 Note & 4	

See attached

**NOTES:** 

1. For T<sub>amb</sub> or T<sub>case</sub> > ±25°C, derate linearly to 0W-at +200°C.

-2. When mounted on an 8 x 10 x 0.6mm ceramic substrate.

2. So For Variants with tin-lead plating or hot solder dip lead finish all testing performed at T<sub>amb</sub> > +125°C shall be carried out in a 100% inert atmosphere.

Duration 10 seconds maximum at a distance of not less than 1.5mm from the device body and the same lead shall not be resoldered until 3 minutes have elapsed.

4 5 Duration 5 seconds maximum and the same terminal shall not be resoldered until 3 minutes have elapsed.

1. Thermall Resistance, Junction-to-Case only applies to TO-18 packaged Variants.

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Thermal Resistance,				
Junction-to-Ambient	$R_{th(j-a)}$	486	°C/W	
Thermal Resistance,				
Junction-to-Case	$R_{th(j-c)}$	145.8	°C/W	Note 1



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The test methods and test conditions shall be as per the corresponding test defined in Room Temperature Electrical Measurements.

The limit values for each characteristic shall not be exceeded.

Characteristics	Symbols	Lin	Units	
		Min	Max	
Collector-Base Cut-off Current	I <sub>CBO</sub>	-	-50	nA
Collector-Emitter Saturation Voltage 2	V <sub>CE(sat)2</sub>	-	-500	mV
Forward-Current Transfer Ratio 2	h <sub>FE2</sub>	60	240	-

#### 2.7 <u>HIGH TEMPERATURE REVERSE BIAS BURN-IN CONDITIONS</u>

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	T <sub>amb</sub>	+150 (+0 -5)	°C
Collector-Base Voltage	V <sub>CB</sub>	-128	V
Duration	t	48 minimum	Hours

#### 2.8 POWER BURN-IN CONDITIONS

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	T <sub>amb</sub>	+25 to +50	°C
Power Dissipation	P <sub>tot</sub>	As per Maximum Ratings.  Ptoti detailed at the chosen  Tamb using the	W
Collector-Base Voltage	V <sub>CB</sub>	90	V

2.9 <u>OPERATING LIFE CONDITIONS</u>

The conditions shall be as specified for Power Burn-in.



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# APPENDIX 'A'



# AGREED DEWATIONS FOR STMICEOELECTRONICS (F)

ITEMA AFFECTED			
ITEMS AFFECTED	DESCRIPTION OF DEVIATIONS		
Deviations from Production Control- Chart F2	Special In-process Control Internal Visual Inspection. For CCP packages the criteria specified for voids in the fillet and minimum die mounting material around the visible die perimeter for die mounting defects may be omitted providing that a radiographic inspection to verify the die-attach process is performed on a sample basis in accordance with STMicroelectronics procedure 0076637.		
Deviations from Room Temperature Electrical Measurements	All AC characteristics (Room Temperature Electrical Measurement Note 2) may be considered guaranteed but not tested if successful pilot lot testing has been performed on the wafer lot which includes AC characteristic measurements per the Detail Specification.  A summary of the pilot lot testing shall be provided if required by the Purchase Order.		
Deviations from High and Low Temperatures Electrical Measurements	All characteristics specified may be considered guaranteed but not teste if successful pilot lot testing has been performed on the wafer lot which includes characteristic measurements at high and low temperatures per the Detail Specification. A summary of the pilot lot testing shall be provided if required by the Purchase Order.		
Deviations from Screening Tests - Chart F3	Solderability is not applicable unless specifically stipulated in the Purchase Order.		