DOCUMENT CHANGE REQUEST

DCR number 496	Changes required for: General	Originator: S Jeffery - ESCC
Date: 2009/04/14	Date sent: 2009/04/14	Organisation: ESA/ESTEC
Status: IMPLEMENTED		

Title:	Transistors High Voltage NPN, based on type 2N5551		
Number:	5201/019	Issue:	4

Other documents affected:

Page:

See attachment

Paragraph:

See attachment

Original wording:

Proposed wording:

Various editorial and technical changes as detailed in the attachment, which are required to make this detail spec clear, complete and consistent with the standard format and content of specifications for similar Part Types. Note that this DCR replaces the withdrawn DCR 465.

Justification:

Improve the appearance, content and clarity of the spec.

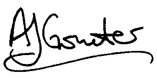
Attachments:

5201019_Issue_5_-_Draft_B.pdf, null

Modifications:

N/A

Approval signature:



Date signed:

2009-04-14

European Space Components Coordination

TRANSISTORS, HIGH VOLTAGE, NPN

BASED ON TYPE 2N5551

ESCC Detail Specification No. 5201/019

as applicable

Issue 4 5 - Draft B	~~December 2008~~

Document Custodian: European Space Agency - see https://escies.org

as applicable

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DOCUMENTATION CHANGE NOTICE

(Refer to https://escies.org for ESCC DCR content)

DCR No.	CHANGE DESCRIPTION
~~413, 423~~ ~~427~~ tbd	Specification up issued to incorporate editorial and technical changes per DCRs.

1. GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics and test and inspection data for the component type variants and/or the range of components specified below. It supplements the requirements of, and shall be read in conjunction with, the ESCC Generic Specification listed under Applicable Documents.

1.2 APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:

(a) ESCC Generic Specification No. 5000
(b) MIL-STD-750, Test Methods and Procedures for Semiconductor Devices

1.3 TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESCC Basic Specification No. 21300 shall apply.

1.4 THE ESCC COMPONENT NUMBER AND COMPONENT TYPE VARIANTS

1.4.1 The ESCC Component Number

The ESCC Component Number shall be constituted as follows:

Example: 520101901

- Detail Specification Reference: 5201019
- Component Type Variant Number: 01 (as required)

1.4.2 Component Type Variants

The component type variants applicable to this specification are as follows:

Variant Number	Based on Type	Case	Lead/Terminal Material and/or Finish	Weight max g
01	2N5551	TO-18	D2	0.4
02	2N5551	TO-18	D3 or D4	0.4
04	2N5551	CCP (3 Terminal)	2	0.06
05	2N5551	CCP (3 Terminal)	4	0.06
06	2N5551	TO-39	D2	1.5
07	2N5551	TO-39	D3 or D4	1.5
08	2N5551	CCP (4 Terminal)	2	0.06
09	2N5551	CCP (4 Terminal)	4	0.06

The lead/terminal material and/or finish shall be in accordance with the requirements of ESCC Basic

Specification No. 23500.

1.5 MAXIMUM RATINGS

The maximum ratings shall not be exceeded at any time during use or storage.

Maximum ratings shall only be exceeded during testing to the extent specified in this specification and when stipulated in Test Methods and Procedures of the ESCC Generic Specification.

Characteristics	Symbols	Maximum Ratings	Unit	Remarks
Collector-Base Voltage	V_{CBO}	180	V	Over entire operating temperature range
Collector-Emitter Voltage	V_{CEO}	160	V	
Emitter-Base Voltage	V_{EBO}	6	V	
Collector Current For TO-18 and TO-39 For CCP	I_C	 600 500	mA	Continuous
Power Dissipation For TO-18, TO-39 and CCP	P_{tot1}	0.36	W	At $T_{amb} \leq +25^{\circ}C$ Note 1
For CCP	P_{tot2}	0.58 (Note 2)	W	
For TO-18 and TO-39	P_{tot2}	1.2	W	At $T_{case} \leq +25^{\circ}C$ Note 1
Operating Temperature Range	T_{op}	-65 to +200	°C	Note 2
Storage Temperature Range	T_{stg}	-65 to +200	°C	Note 2
Soldering Temperature For TO-18 and TO-39 For CCP	T_{sol}	 +260 +245	°C	 Note 3 Note 4

see attached

make o bigger

NOTES:

1. ~~For T_{amb} or $T_{case} > +25^{\circ}C$, derate linearly to 0W at $+200^{\circ}C$.~~
2. ~~When mounted on an 8 x 10 x 0.6mm ceramic substrate.~~
2. For Variants with tin-lead plating or hot solder dip lead finish all testing, and any handling, performed at $T_{amb} > +125^{\circ}C$ shall be carried out in a 100% inert atmosphere.
3. Duration 10 seconds maximum at a distance of not less than 1.5mm from the device body and the same lead shall not be resoldered until 3 minutes have elapsed.
4. Duration 5 seconds maximum and the same terminal shall not be resoldered until 3 minutes have elapsed.

1. Thermal Resistance, Junction-to-Case applies to all TO-18 and TO-39 packaged Variants.

Thermal Resistance, Junction-to-Ambient	$R_{th(j-a)}$	486	°C/W	
Thermal Resistance, Junction-to-Case	$R_{th(j-c)}$	145.8	°C/W	Note 1

Characteristics	Symbols	Limits			Units
		Drift Value Δ	Absolute		
			Min	Max	
Collector-Base Cut-off Current	I_{CBO}	±5 or (1) ±100%	-	50	nA
Collector-Emitter Saturation Voltage 2	$V_{CE(sat)2}$	±30 or (1) ±15%	-	200	mV
Forward-Current Transfer Ratio 2	h_{FE2}	±15%	80	250	-

NOTES:
1. Whichever is the greater referred to the initial value.

2.6 INTERMEDIATE AND END-POINT ELECTRICAL MEASUREMENTS

Unless otherwise specified, the measurements shall be performed at T_{amb}=+22 ±3°C.

The test methods and test conditions shall be as per the corresponding test defined in Room Temperature Electrical Measurements.

The limit values for each characteristic shall not be exceeded.

Characteristics	Symbols	Limits		Units
		Min	Max	
Collector-Base Cut-off Current	I_{CBO}	-	50	nA
Collector-Emitter Saturation Voltage 2	$V_{CE(sat)2}$	-	200	mV
Forward-Current Transfer Ratio 2	h_{FE2}	80	250	-

2.7 POWER BURN-IN CONDITIONS

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	T_{amb}	+25 to +50	°C
Power Dissipation	P_{tot}	As per Maximum Ratings. P_{tot1} ~~derated~~ at the chosen T_{amb} using the	W
Collector-Base Voltage	V_{CB}	90	V

Derate

specified $R_{th(j-a)}$.

2.8 OPERATING LIFE CONDITIONS

The conditions shall be as specified for Power Burn-in.

P

S -

APPENDIX 'A'

AGREED DEVIATIONS FOR STMICROELECTRONICS (F)

<table>
<tr><th>ITEMS AFFECTED</th><th>DESCRIPTION OF DEVIATIONS</th></tr>
<tr><td>Deviations from Production Control-Chart F2</td><td>Special In-process Control Internal Visual Inspection.
For CCP packages the criteria specified for voids in the fillet and minimum die mounting material around the visible die perimeter for die mounting defects may be omitted providing that a radiographic inspection to verify the die-attach process is performed on a sample basis in accordance with STMicroelectronics procedure 0076637.</td></tr>
<tr><td>Deviations from Room Temperature Electrical Measurements</td><td>All AC characteristics (Room Temperature Electrical Measurement Note 2) may be considered guaranteed but not tested if successful pilot lot testing has been performed on the wafer lot which includes AC characteristic measurements per the Detail Specification.

A summary of the pilot lot testing shall be provided if required by the Purchase Order.

Characteristics h_{fe2}, and C_{ebo}, shall be as follows:
<table>
<tr><th rowspan="2">Characteristics</th><th rowspan="2">Symbols</th><th rowspan="2">MIL-STD-750 Test Method</th><th rowspan="2">Test Conditions</th><th colspan="2">Limits</th><th rowspan="2">Units</th></tr>
<tr><th>Min.</th><th>Max.</th></tr>
<tr><td>High Frequency Small-Signal Short-Circuit Forward-Current Transfer Ratio</td><td>h_{fe2}</td><td>3306</td><td>V_{CE}=10V
I_C=10mA
f=20MHz
Note 2</td><td>2.5</td><td>-</td><td>-</td></tr>
<tr><td>Emitter-Base Capacitance</td><td>C_{ebo}</td><td>3240</td><td>V_{EB}=500mV
I_C=0A
f=1MHz
Note 2</td><td>-</td><td>45</td><td>pF</td></tr>
</table></td></tr>
<tr><td>Deviations from High and Low Temperatures Electrical Measurements</td><td>All characteristics specified may be considered guaranteed but not tested if successful pilot lot testing has been performed on the wafer lot which includes characteristic measurements at high and low temperatures per the Detail Specification. A summary of the pilot lot testing shall be provided if required by the Purchase Order.</td></tr>
<tr><td>Deviations from Screening Tests - Chart F3</td><td>Solderability is not applicable unless specifically stipulated in the Purchase Order.</td></tr>
</table>