



DOCUMENT CHANGE REQUEST

DCR number	509	Changes required for:	General	Originator:	S Jeffery - ESCC
Date:	2009/05/06	Date sent:	2009/05/06	Organisation:	ESA/ESTEC
Status: IMPLEMENTED					

Title:	Transistors Field-Effect N-Channel, based on types 2N4391/2N4392 and 2N4393				
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Number:	5205/003	Issue:	2		
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Other documents affected:

Page:

See attachment

Paragraph:

See attachment

Original wording:

Proposed wording:

Update the Maximum Ratings table (see the attachment for details) so that this detail spec is clear, complete and the content and format is in-line with other detail specifications for similar Part Types.

Justification:

Improve the content and clarity of the spec.

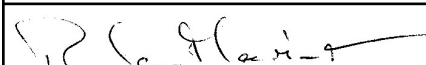
Attachments:

5205003\_Issue\_3\_-\_Draft\_A.pdf, null

Modifications:

Page 6: original Note 2 to Maximum Ratings, add ", and any handling,"between "testing" and "performed".

Approval signature:



Date signed:

2009-05-06



Pages 1 to 13

## TRANSISTORS, FIELD-EFFECT, N-CHANNEL

BASED ON TYPE 2N4391, 2N4392 AND 2N4393

ESCC Detail Specification No. 5205/003

as applicable

Issue 3 - Draft A	May 2008
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Document Custodian: European Space Agency - see <https://escies.org>



as applicable

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**DOCUMENTATION CHANGE NOTICE**

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DCR No.	CHANGE DESCRIPTION
<del>381</del>	Specification up issued to incorporate editorial and technical changes per DCR.

tbd

when stipulated in Test Methods and Procedures of the ESCC Generic Specification.

At  $T_{case} \leq +25^{\circ}C$

Characteristics	Symbols	Maximum Ratings	Unit	Remarks
Drain-Source Voltage	$V_{DS}$	40	V	Over entire operating temperature range
Gate-Source Voltage	$V_{GS}$	-40	V	
Gate-Drain Voltage	$V_{GD}$	-40	V	
Gate Current	$I_G$	50	mA	
Power Dissipation	$P_{tot1}$	0.300	W	At $T_{amb} \leq +25^{\circ}C$
	$P_{tot2}$	1.8	W	Notes 1
Operating Temperature Range	$T_{op}$	-55 to +175	$^{\circ}C$	Note 1
Storage Temperature Range	$T_{stg}$	-65 to +200	$^{\circ}C$	Note 1
Soldering Temperature	$T_{sol}$	+235	$^{\circ}C$	Note 2

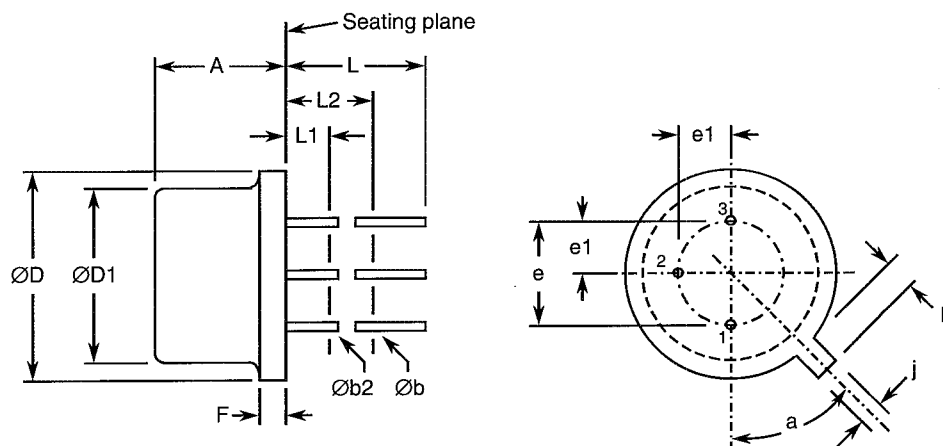
see attached

#### NOTES:

- For  $T_{amb} > +25^{\circ}C$ , derate linearly to 0W at  $+175^{\circ}C$ .
- For Variants with tin-lead plating or hot solder dip lead finish all testing performed at  $T_{amb} > +125^{\circ}C$  shall be carried out in a 100% inert atmosphere.
- Duration 10 seconds maximum at a distance of not less than 1.5mm from the device body and the same lead shall not be resoldered until 3 minutes have elapsed.

## 1.6 PHYSICAL DIMENSIONS AND TERMINAL IDENTIFICATION

### 1.6.1 Metal Can Package (TO-18) - 3 lead



Symbols	Dimensions mm		Notes
	Min	Max	
A	4.32	5.33	
Øb	0.406	0.533	2, 3

Thermal Resistance, Junction-to-Ambient	$R_{th(j-a)}$	500	°C/W	
Thermal Resistance, Junction-to-Case	$R_{th(j-c)}$	83.3	°C/W	