	ES(<u>.C</u>	D	OCUMENT	CHANGE REQUEST					
DCR number	634	Changes red	quired for: N/	4	Originator: Samuel SAVIN					
Date: 2011/06	6/16	Date sent: 2	2010/11/23		Organisation: CNES					
Status: IMPLE	EMENTED									
Title:	Diodes Silicon Sv	vitching, based o	on types 1N66	39, 1N6640 and 1I	N6641					
Number:	5101/027		Issue:	1						
Other documen	ts affected:									
Page:										
See attached document										
Paragraph:	Paragraph:									
See attached d	See attached document									
Original wording	g:									
Proposed wordi	ng:									
See attached d	ocument									
Justification:										
Variant 07: new Variant 08: new	/ ST variant introdu / ST variant introdu	uction with LCC2 uction with LCC2	D package D package							
Attachments:										
DCR634att.pdf,	, DCR_1N6640.pd	f, null								
Modifications:										
The original atta	achment to this DC	CR, provided by	STMicroelectr	onics, is replaced b	by the attached 5101/027 issue 2 Draft B.					
This change wo of this Detail Sp formatted speci Specification.	This change wording serves to implement the new STM Variants 07 and 08 and at the same time perform a total reformat of this Detail Specification (under Generic Specification No. 5000) as part of the ongoing conversion of legacy ESA/SCC formatted specifications to the ESCC format. See below for summary of changes and attached Issue 2 Draft B of the Specification.									
Note: known support for active procurement against this specification includes the following manufacturers: STMICROELECTRONICS/F are currently willing to support the procurement of new Variants 07 and 08.										

MICROSEMI/I have indicated some interest in supporting some types covered by this specification. Full details are not currently available but it is expected that types 1N66XX, MIL qualified per MIL-PRF-19500/609 in various packages, may be considered. However is has been confirmed by MICROSEMI/I that existing Variants 01 to 06 are not supported in their currently specified form. It is intended to proceed with a new update of this specification in order to implement additional Variants for MICROSEMI/I once this DCR has been approved and implemented.

Summary of changes to the current format, layout and content is as follows:

a) Rewording and restructure of various sections and paragraphs of the specification plus other editorial changes based on the layout and editorial content of other Detail Specifications already converted to ESCC format, as well as changes to make the Detail specification consistent with the current ESCC Generic Specification No. 5000.

b) Removal of any redundant paragraphs and information,

e.g.: Figure 1; mechanical paragraph; Figures 4, 5(a), 5(b); Appendix A for MICROSEMI/I

c) Removal of all requirements specifically applicable to obsolete types & Variants 01 to 06, plus addition and amendment of requirements as apply to the new 1N6640U Variants 07 & 08 and for STM. This impacts the following locations in the specification:

Title page: remove reference to 1N6639, 1N6641. Only type 1N6640U now applies to this spec issue 2.

Para 1.7: delete reference to tin-lead plated lead finish

Table 1(a): delete obsolete Variants 01 to 06 and add 07 & 08 for type 1N6640U in LCC2D package

Table 1(b): Soldering Temperature, Junction Temperature, Thermal Resistance

Figure 2

Figure 3

Para 4.2 & 4.2.1 to 4.2.5: all deviations from Generic Spec are deleted.

Para 4.3.2 Para 4.3.3 Para 4.4.1, 4.4.2 Table 2 Table 3(a) & 3(b) Table 4 Table 5(a) & 5(b) Table 6

Details of specific technical changes are as follows (See attached 5101/027 Issue 2 Draft B for full details):

1) Table 1(b) (now Para 1.5): Forward Surge Current rating is changed to be 2A maximum (was 2.5A) based on STM characterisation data.

2) Para 4.2.2(g) additional Surge Current Test is not required (this is justified based on use of STM's internal Pilot Lot procedure N° 7188211)

3) Table 2 Breakdown Voltage test V(BR) (now Para 2.3.1): Test is replaced by equivalent Reverse Current test (IR2)

4) Table 2 Reverse Recovery Time 1 trr1 (now Para 2.3.1): Test is considered guaranteed but not tested based on testing of added parameter Reverse Recovery Time 2 trr2.

5) Table 3(b) (now Para 2.3.2 & Appendix A):

Reverse Current (IR2 for Breakdown Voltage) is added (but is considered guaranteed but not tested based on STMs pilot lot testing).

6) Table 4 Breakdown Voltage test V(BR) (now Para 2.4): Test is deleted as the specified Breakdown Voltage test does not produce a result that can be used for delta calculations (i.e. The test per MIL-STD-750 Method 4021 is effectively a go-no-go test) 7) Table 5(a) (now Para 2.6): Duration is changed to be >=48h (was 72h) for clarification purposes. 8) Table 5(b) (now Para 2.7): Power Burn-in conditions are amended to reflect a test operating the components at junction temperature. 9) Table 6 (now Para 2.5): Change/delta Limits for parameters are not included; only absolute limits apply. Reverse Current (IR2 for Breakdown Voltage) is added. 10) General deviations to the ESCC Generic & Detail Specs, as already agreed in other ESCC published Detail Specs for STM, are included as Appendix A for STM. Justification: as above Approval signature: c flaring Date signed: 2011-06-16

TABLE 1(a)- Type Variants

Variant	Based on Type	Case	Figure	Breakdown Voltage V(BR) (V)	Repetitive peak reverse voltage VRRM (V)	Working Peak Reverse Voltage VRWM (V)	Lead/Terminal Material and Finish
<mark>07</mark>	<mark>1N6640U</mark>	LCC2D	2(c)	<mark>75</mark>	<mark>75</mark>	-	2
<mark>08</mark>	1N6640U	LCC2D	2(c)	<mark>75</mark>	<mark>75</mark>	-	<mark>4</mark>

Justification .

Variant 07: new ST variant introduction with LCC2D package Variant 08: new ST variant introduction with LCC2D package

TABLE 1(b)- MAXIMUM RATINGS

N°	Characteristics	Symbols	Maximum Ratings	Unit	Remarks
1	Forward Surge Current (per Diode)				At Tamb $\leq +25^{\circ}C$
	Variants 01 to 06	IFSM	2.5	A(pk)	Note 1
	Variants 07 to 08		<mark>2</mark>	A	
3	Average Output Rectified Current				
	Variants 01 to 06	IO	300	mA	Note 3 and 4
	Variants 07 to 08		<mark>300</mark>	m <mark>A</mark>	Note 7
4	Operating Temperature Range				
	Variants 01 to 06	Тор	-65 to +175	°C	Tamb
	Variants 07 to 08 (Case Temperature)	<mark>Top</mark>	<mark>-65 to +175</mark>	°C	Note 8
added	Junction Temperature	<mark>Tj</mark>	<mark>+175</mark>	°C	
	Variants 07 to 08				
5	Storage Temperature Range	Tstg	-65 to +175	°C	
	Variants 01 to 06				
	Variants 07 to 08				Note 8
6	Soldering Temperature	Tsol		°C	
	Variant 01 to 03		+260		Note 5
	Variant 04 to 06		+245		Note 6
	Variants 07 to 08		+245		Note 9
added	Thermal Resistance, Junction to Case	Rth(j-c)	<mark>60</mark>	°C/W	Note 10
	Variants 07 to 08				
added	Thermal Resistance, Junction to Ambient	Rth(j-a)	<mark>280</mark>	°C/W	
	Variants 07 to 08				

NOTES:

7. For Variants 07 to 08 at Tcase \geq +155°C per Diode, derate linearly to 0A at +175°C.

8. For Variants with hot solder dip lead finish all testing performed at Tamb>+125°C shall be carried out in a 100% inert atmosphere.

9. Duration 5 seconds maximum. The same package must not be resoldered until 3 minutes have elapsed. 10. Package mounted on infinite heatsink.

Justification .

Variant 07: new ST variant introduction with LCC2D package Variant 08: new ST variant introduction with LCC2D package

FIGURE 1 – PARAMETER DERATING INFORMATION (Not Applicable for the variants 07 to 08)



Justification .

Variant 07: new ST variant introduction with LCC2D package Variant 08: new ST variant introduction with LCC2D package

Figure 2(c)- Variant 07 to 08 - Leadless Chip Carrier 2 (LCC2D) – 2 Terminal



Notes:

The anode is identified by a metallization in 2 top angle castellations and by the index mark on the bottom metallization n° 1.
 Measurement prior to solder coating the mounting pads on bottom of package.

Justification .

Variant 07: new ST variant introduction with LCC2D package Variant 08: new ST variant introduction with LCC2D package

FIGURE 3 - FUNCTIONAL DIAGRAM

Variants 07 to 08 Terminal 1: Anode Terminal 2: Cathode



Notes:

For LCC2, the lid is not connected to any lead.

Justification .

Variant 07: new ST variant introduction with LCC2D package Variant 08: new ST variant introduction with LCC2D package

4.2.2 Deviations from Final Production Tests (Chart II)

(a) Para. 9.2.1, Bond Strenght Test: Not applicable. Excepted for the variants 07 to 08 (Applicable in the Chart F2 of the ESCC N°5000 Issue 6).

(b) Para. 9.2.2, Die Shear Test: Not applicable. Excepted for the variants 07 to 08 (Applicable in the Chart F2 of the ESCC N°5000 Issue 6).

(c) At any time following Para. 9.5.1, Thermal Shock Test, Thermal impedance measurements shall be performed in accordance with MIL-STD-750, TEST Method 3101 as specified in Table 2, item 11.
For the variants 07 to 08 (the thermal impedance is applicable in the Chart F3 of the ESCC N°5000 Issue 6).
For the variants 07 to 08 (the thermal shock is applicable in the Chart F4 Environmental Subgroup of the ESCC N°5000 Issue 6).

(d) Para. 9.6, Constant Acceleration: Not applicable. Excepted for the variants 07 to 08 (Applicable in the Chart F4 Mechanical Subgroup of the ESCC N°5000 Issue 6).

(e) Para. 9.7 Particle Impact Noise Detection (PIND) test: Not applicable Excepted for the variants 07 to 08 (Applicable in the Chart F3 of the ESCC N°5000 Issue 6).

(f) Para. 9.8.1, Seal Test Fine Leak: Not applicable Excepted for the variants 07 to 08 (Applicable in the Chart F3 of the ESCC N°5000 Issue 6).

(g)Excepted for the variants 07 to 08: N/A.

Justification .

Variant 07: new ST variant introduction with LCC2D package Variant 08: new ST variant introduction with LCC2D package

4.2.3 Deviations from Burn-In and Electrical Measurements (Chart III)

(b) Para. 9.8.1 Seal Test Fine Leak: Not applicable
Excepted for the variants 07 to 08 (Applicable in the Chart F3 of the ESCC N°5000 Issue 6).
(c) Para. 9.12, Radiographic Inspection: Not applicable
Excepted for the variants 07 to 08 (Applicable in the Chart F3 of the ESCC N°5000 Issue 6).

Justification .

Variant 07: new ST variant introduction with LCC2D package Variant 08: new ST variant introduction with LCC2D package

4.2.4 Deviations from Qualification Tests (Chart IV)

(a) Para. 9.2.3, Bond Strenght Test: Not applicable Excepted for the variants 07 to 0 (Applicable in the Chart F4 Assembly Capability Subgroup of the ESCC N°5000 Issue 6).

(b) Para. 9.2.4, Die Shear Test: Not applicable

Excepted for the variants 07 to 08 (Applicable in the Chart F4 Assembly Capability Subgroup of the ESCC N°5000 Issue 6).

(c) Para. 9.8.1, Seal Test Fine Leak: Not applicable

Excepted for the variants 07 to 08 (Applicable in the Chart F4 Environmental and Mechanical Subgroup of the ESCC N°5000 Issue 6).

(d) Para. 9.15, Constant Acceleration: Not applicable

Excepted for the variants 07 to 08 (Applicable in the Chart F4 Mechanical Subgroup of the ESCC N°5000 Issue 6). Justification.

Variant 07: new ST variant introduction with LCC2D package Variant 08: new ST variant introduction with LCC2D package

4.2.5 Deviations from Lot Acceptance Tests (Chart V)

(a) Para. 9.8.1, Seal Test Fine Leak: Not applicable Excepted for the variants 07 to 08 (Applicable in the Chart F4 F4 Environmental and Mechanical Subgroup of the ESCC N°5000 Issue 6).

(b) Para. 9.15, Constant Acceleration: Not applicable

Excepted for the variants 13 to 14 (Applicable in the Chart F4 Mechanical Subgroup of the ESCC N°5000 Issue 6). Justification.

Variant 07: new ST variant introduction with LCC2D package Variant 08: new ST variant introduction with LCC2D package

4.3.2 Weight

The maximum weight of the diodes specified herein shall be 0.2 grammes for the variants 01 to 03 and 0.13 grammes for variant 04 to 06 and 0.12 grammes for the variants 07 to 08.

Justification .

Variant 07: new ST variant introduction with LCC2D package Variant 08: new ST variant introduction with LCC2D package

4.3.3 Terminal Strength

For the variants 07 to 08 as specified in the ESCC Generic Specification (Applicable in the Chart F4 Assembly Capability Subgroup of the ESCC N°5000 Issue 6).

Justification .

Variant 07: new ST variant introduction with LCC2D package Variant 08: new ST variant introduction with LCC2D package

4.4.1 Case

The case shall be hermetically sealed and have an Aln body with kovar lid for the variants 07 to 08.

Justification .

Variant 07: new ST variant introduction with LCC2D package Variant 08: new ST variant introduction with LCC2D package

4.4.2 Lead Material and Finish

For the variants 07 to 08 leads/terminals as specified in the Table 1a. Justification.

Variant 07: new ST variant introduction with LCC2D package Variant 08: new ST variant introduction with LCC2D package

4.5.1 General

For the variants 07 to 08 the marking shall be in accordance with the requirements of ESCC Basic Specification No. 21700 and as follows. The information to be marked on the component shall be: (a) Polarity. (a) The ESCC qualified components symbol (for ESCC qualified components only). (b) The ESCC Component Number.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE D.C.PARAMETERS

	Chamastaristics	Symbols	MIL-STD-750	Test Conditions	Limits		Unite
N°	Characteristics	Symbols	Test Method	Test Conditions	Min	Max	Units
1	Breakdown	V _(BR)	4021	$I_R = -10 \mu A$			
	Voltage			Variants 01 to 06 only	Note1	-	V
2	Forward	V _{F1}	4011	Pulse Method			
	Voltage			I _F =200mA,			
				Variants 07 to 8 (Note 2)	-	<mark>1.1</mark>	V
3	Forward	V _{F2}	4011	Pulse Method			
	Voltage			I _F =100mA,			
				Variants 07 to 8 (Note 2)	-	<mark>0.98</mark>	V
4	Forward	V _{F3}	4011	Pulse Method			
	Voltage			$I_F = 50 \text{mA},$			
				Variants 07 to 8 (Note 2)	-	<mark>0.89</mark>	V
5	Forward	V _{F4}	4011	Pulse Method			
	Voltage			$I_F=1mA$,			
	-			Variants 07 to 8 (Note 2)	-	<mark>0.63</mark>	V
6	Reverse Current	I _{R1}	4016	DC Method			
				$V_R=50V$			
				Variant 07 to 08	-	<mark>40</mark>	nA

<u>Notes</u>

- 1. See Colum 5 of Table 1(a).
- 2. For variant 01 to 06 pulsed measurement: tp = 300μ s maximum For variant 07 t o 08 Pulse Width $\leq 680\mu$ s; Duty Cycle $\leq 2\%$
- 3. See Colum 6 of Table 1(a).

Justification .

Variant 07: new ST variant introduction with LCC2D package Variant 08: new ST variant introduction with LCC2D package

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - A.C. PARAMETERS

N°	Characteristics	Symbols	MIL-STD-750	Test Conditions	Limits		Unite
	Characteristics	Symbols	Test Method	Test Conditions	Min	Max	Units
added	Junction Capacitance	C,		V _R =0Vdc Vsig=50mV(p-p)max f=1MHz (Note 4) Variants 07 to 08	-	<mark>3</mark>	pF
8	Reverse Recovery Time	Trr <mark>1</mark>	4031 Cond. 'A'	$I_{F}=I_{RM}=10$ to 100mA $I_{RR}=10\%$ of I_{RM} (Note 1) Variants 01, 02, 04, 05 Variants 03, 06 (Note 4 and 5)		4.0 5.0	nS
		Trr2	4031 Cond. 'A'	Variants 07 to 08 $I_F = 1A; V_R = 30V$ $DI/dt = -15A/\mu S$ (Note 4) Variants 07 to 08	-	9 20	nS
9	Forward Recovery Time	T _{FR}	4026	$I_F = 200mA$ (Note 1 and 2) Variants 01 to 06 (Note 4) Variants 07 to 08	-	10 20	nS
10	Forward Recovery Voltage	V _{FR}	4026	$I_F = 200 \text{mA}$ (Note 1 and 2) Variants 01 to 06 (Note 4) Variants 07 to 08	-	5	V
11	Thermal	Z _{TH(J-C)}	3101	Variants 01 to 06 only			

	Impedance						
added	Thermal Impedance	Z _{TH(J-C)}	3101	Variants 07 to 08 $I_H=0.1$ to 0.3A $t_H=50ms$ to 10s $I_M=10mA$ $t_{md}=100\mu s$	Calculate (see Note	ΔVF, 7)	°C/W

NOTES

4) See appendix A [Agreed Deviations for STMicroelectronics (F)]

5) Test parameter trr1 is not tested but guaranteed by trr2.

6) Performed only during Screening Tests Parameter Drift Values (Initial Measurements), go-no-go.

7) The limits for ΔVF shall be defined by the Manufacturer on every lot in accordance with MIL-STD-750 Method 3101

and shall guarantee the Rth(j-a) limits specified in Maximum Ratings.

Justification .

Variant 07: new ST variant introduction with LCC2D package Variant 08: new ST variant introduction with LCC2D package

TABLE 3(a) - ELECTRICAL MEASUREMENTS AT HIGH TEMPERATURES

N°	Characteristics	Sumbola	MIL-STD-750	Test Conditions	Limits		Units
	Characteristics	Symbols	Test Method	Test Conditions	Min	Max	
3	Reverse Current	I _{R1}	4016	DC Method			μA
				$V_R = Note1$			
				Variants 01 to 06	-	100	
				Tamb=+150(+0-5)°C			
				Variants 07 to 08 (Note 2)			
				$V_{R} = 50V$	-	<mark>30</mark>	

NOTES

2. Read and record measurements shall be performed on a sample of 5 components with 0 failures allowed. Alternatively a 100% inspection may be performed.

Justification .

Variant 07: new ST variant introduction with LCC2D package Variant 08: new ST variant introduction with LCC2D package

TABLE 3(b) - ELECTRICAL MEASUREMENTS AT LOW TEMPERATURES

N°	Characteristics	Symbols	MIL-STD-750	Test Conditions	Limits		Units
	Characteristics	Symbols	Test Method	Test Conditions	Min	Max	Units
1	Forward	V _{F1}	4011	$I_F = 500 \text{mA} \text{ (Note 1)}$			
	Voltage			Variants 01, 04	-	1.3	
				$I_F=200 \text{mA} \text{ (Note 1)}$			V
				Variants 02, 05	-	1.1	
				Variants 03, 06	-	1.2	
				Tamb=-55(+5-0)°C			
				Pulse Method			
				I _F =200mA			
				Variants 07 to 08 (Note 2 and 3)	-	<mark>1.2</mark>	

NOTES

2. Pulse Width $\leq 680 \mu s$; Duty Cycle $\leq 2\%$

3. Read and record measurements shall be performed on a sample of 5 components with 0 failures allowed. Alternatively a 100% inspection may be performed.

TABLE 4 PARAMETER DRIFT VALUES FOR VARIANTS 07 T08

	Limits						
Characteristics	Symbols	Drift Value	Abs	olute	Units		
		Δ	Min	Max			
Reverse Current 1	I _{R1}	<mark>+/-10</mark>	-	<mark>40</mark>	nA		
		<mark>or</mark>					
		<mark>+/-100%</mark>					
Forward Voltage 1	V _{F1}	+/-50	_	<mark>1100</mark>	mV		

Note:

 Whichever is the greater referred to the initial value. Justification.

Variant 07: new ST variant introduction with LCC2D package Variant 08: new ST variant introduction with LCC2D package

TABLE 5(a) CONDITION FOR HIGH TEMPERATURE REVERSE BIAS BURN-IN

N°	Characteristics	Symbols	Conditions	Units
2	Reverse Voltage	V		
	Variants 07 to 08	V _R	<mark>60 (80% of V_{RRM})</mark>	V
3	Duration			
	Variants 01 to 06	t	72	Hours
	Variants 07 to 08	t	<mark>≥48</mark>	Hours 1

Justification .

Variant 07: new ST variant introduction with LCC2D package Variant 08: new ST variant introduction with LCC2D package

TABLE 5(c) - CONDITIONS FOR POWER BURN-IN AND OPERATING LIFE TESTS

For the variants 07 to 08

N°	Characteristics	Symbols	Test Conditions	Units
1	Ambient Temperature	<mark>Tamb</mark>	+125 (+0/-5)	°C
2	Junction Temperature	Tj	+175 (+0 -5)	°C
<mark>3</mark>	Average Output Rectified Current	IO	Note 2	A

NOTES:

2. The output current may be adjusted, within their given limit ranges, to attain the specified junction temperature. *Justification*.

Variant 07: new ST variant introduction with LCC2D package Variant 08: new ST variant introduction with LCC2D package

TABLE 6 - ELECTRICAL MEASUREMENTS AT INTERMEDIATE POINTS AND ONCOMPLETION OF ENDURANCE TESTING

		SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	CHANGE	ABSOLUTE		
No.	CHARACTERISTICS			(Note1 and 2)	LIMITS (Δ)	MIN.	MAX.	UNIT
	D.C Forward Voltage 1		As per Table 2	As per Table 2				
2		VF1		Variants 01, 04	+/- 0.03V	-	1.2	
				Variants 02, 05	+/- 0.03V	0.87	1	V
				Variants 03, 06	+/- 0.03V	-	1.1	
				Variant 07 to 08	-	-	<mark>1.1</mark>	
				As per Table 2	+/- 20nA			
4	Pavarsa Current	ID	As per Table 2	Variant 01 to 06	Or (1)	-	100	nΛ
7	Reverse Current	IK	As per Table 2		+/-100%			шл
				Variant 07 to 08	-	-	<mark>40</mark>	

NOTES

2. Changes limits are not applicable for the variants 07 to 08.

Justification .

Variant 07: new ST variant introduction with LCC2D package Variant 08: new ST variant introduction with LCC2D package

APPENDIX 'B'

AGREED DEVIATIONS FOR STN	MICROELECTRONICS (F)
ITEMS AFFECTED	DESCRIPTION OF DEVIATIONS
Deviations from	Internal Visual Inspection: Wedge bonds equal to 1.1 wire diameter are acceptable for
Production Control-Chart F2	bonding with a V-Groove tool.
Deviations from Production	Special In-process Control Internal Visual Inspection.
Control-Chart F2	For CCP packages the criteria specified for voids in the filet and minimum die mounting
	material around the visible die perimeter for die mounting defects may be omitted
	providing that a radiographic inspection to verify the die-attach process is performed on a
	sample basis in accordance with STMicroelectronics procedure 7050651.
Deviations from Screening	Solderability is not applicable unless otherwise stipulated in the Purchase Order.
Tests- Chart F3	
Deviations from Room	Test parameter the reverse recovery time trr1 is not tested but guaranteed by trr2.
Temperature Electrical	AC characteristics (t_{rr2} , C, t_{fr} , V_{fr}), may be considered guaranteed but not tested if

Measurements	successful pilot lot testing has been performed in accordance with STMicroelectronics procedure 7188211 on the wafer lot, which includes AC characteristic measurements per the Detail Specification.
	A summary of the pilot lot testing shall be provided if required by the Purchase Order.
Deviations from High and Low	Low temperature characteristic I _{R2} may be considered guaranteed but not tested if
Temperature Electrical	successful pilot lot testing has been performed in accordance with STMicroelectronics
Measurements	procedure 7188211 on the wafer lot, which includes low temperature characteristic
	measurements per the Detail Specification.
	A summary of the pilot lot testing shall be provided if required by the Purchase Order.

Justification. Variant 07: new ST variant introduction with LCC2D package Variant 08: new ST variant introduction with LCC2D package



Pages 1 to 12

DIODE, SILICON, SWITCHING

BASED ON TYPE 1N6640U

ESCC Detail Specification No. 5101/027

Issue 2 Draft C	March 2011



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DOCUMENTATION CHANGE NOTICE

(Refer to https://escies.org for ESCC DCR content)

DCR No.	CHANGE DESCRIPTION
DCR634	Specification up issued to incorporate editorial and technical changes per DCR.



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ISSUE 2 Draft C

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APPENDIX 'A'



1. <u>GENERAL</u>

1.1 <u>SCOPE</u>

This specification details the ratings, physical and electrical characteristics and test and inspection data for the component type variants and/or the range of components specified below. It supplements the requirements of, and shall be read in conjunction with, the ESCC Generic Specification listed under Applicable Documents.

1.2 <u>APPLICABLE DOCUMENTS</u>

The following documents form part of this specification and shall be read in conjunction with it:

- (a) ESCC Generic Specification No. 5000
- (b) MIL-STD-750, Test Methods and Procedures for Semiconductor Devices

1.3 TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESCC Basic Specification No. 21300 shall apply.

1.4 THE ESCC COMPONENT NUMBER AND COMPONENT TYPE VARIANTS

1.4.1 <u>The ESCC Component Number</u> The ESCC Component Number shall be constituted as follows:

Example: 510102707

- Detail Specification Reference: 5101027
- Component Type Variant Number: 07

1.4.2 <u>Component Type Variants</u>

The component type variants applicable to this specification are as follows:

Variant Number	Based on Type	Case	Breakdown Voltage V _(BR) (V)	Working Peak Reverse Voltage V _{RWM} (V)	Terminal Finish	Weight max g
07	1N6640U	LCC2D	75	50	2 (Note 1)	0.12
08	1N6640U	LCC2D	75	50	4	0.12

NOTES:

1. With electrolytic nickel underplating.

The terminal finish shall be in accordance with the requirements of ESCC Basic Specification No. 23500



1.5 MAXIMUM RATINGS

The maximum ratings shall not be exceeded at any time during use or storage.

Maximum ratings shall only be exceeded during testing to the extent specified in this specification and when stipulated in Test Methods and Procedures of the ESCC Generic Specification.

Characteristics	Symbols	Maximum Ratings	Unit	Remarks
Forward Surge Current	I _{FSM}	2	A	Notes 1, 2
Working Peak Reverse Volt- age	V _{RWM}	Note 3	V	
Average Output Rectified Cur- rent	۱ ₀	300	mA	Note 4
Operating Temperature Range (Case Temperature)	Т _{ор}	-65 to +175	°C	Note 5
Junction Temperature	Тj	+175	°C	
Storage Temperature Range	T _{stg}	-65 to +175	°C	Note 5
Soldering Temperature	T _{sol}	+245	°C	Note 6
Thermal Resistance, Junction to Case	R _{th(j-c)}	60	°C/W	Note 7
Thermal Resistance, Junction to Ambient	R _{th(j-a)}	280	°C/W	

NOTES:

- 1. Sinusoidal pulse of 8.3ms duration.
- 2. At $T_{amb} \leq +25^{\circ}C$.
- 3. See Component Type Variants for V_{RWM} value.
- 4. At $T_{case} \ge +155^{\circ}C$, derate linearly to 0A at +175°C.
- 5. For Variants with hot solder dip lead finish all testing and any handling performed at $T_{amb} > +125^{\circ}C$ shall be carried out in a 100% inert atmosphere.
- 6. Duration 5s maximum and the same package shall not be resoldered until 3 minutes have elapsed.
- 7. Package mounted on an infinite heat sink.

1.6 HANDLING PRECAUTIONS

These devices are susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacture, testing, packaging, shipment and any handling.

These components are categorised as Class 3 per ESCC Basic Specification No. 23800 with a Minimum Critical Path Failure Voltage of 5800 Volts.



1.7 PHYSICAL DIMENSIONS AND TERMINAL IDENTIFICATION

1.7.1 Leadless Chip Carrier Package (LCC2D) - 2 Terminal





Symbols	Dimensio	Notes	
Symbols	Min	Мах	
A	1.86	2.2	2
В	4.44	4.77	
С	1.84	2.1	
D	1.53	1.87	
E	0.48	0.71	

NOTES:

- 1. Terminal identification: The anode is identified by metallisation in the two castellations and by the index mark on the bottom metallisation.
- 2. For Variant 08 dimension limits apply prior to solder coating of terminals.

1.8 FUNCTIONAL DIAGRAM

Terminal 1: Anode Terminal 2: Cathode





NOTES:

1. For LCC2D the lid is not connected to any terminal.

1.9 <u>MATERIALS AND FINISHES</u>

Materials and finishes shall be as follows:

- a) Case
 - The case shall be hermetically sealed and have an Aluminium Nitride body with a Kovar lid.
- b) Terminal Finish
 As specified in Component Type Variants.

2. <u>REQUIREMENTS</u>

2.1 <u>GENERAL</u>

The complete requirements for procurement of the components specified herein are as stated in this specification and the ESCC Generic Specification. Permitted deviations from the Generic Specification, applicable to this specification only, are listed below.

Permitted deviations from the Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESCC requirement and do not affect the component's reliability, are listed in the appendices attached to this specification.

2.1.1 Deviations from the Generic Specification None

2.2 <u>MARKING</u>

The marking shall be in accordance with the requirements of ESCC Basic Specification No. 21700 and as follows.

The information to be marked on the component shall be:

- (a) Terminal Identification.
- (b) The ESCC qualified components symbol (for ESCC qualified components only).
- (c) The ESCC Component Number.
- (d) Traceability information.
- 2.3 <u>ELECTRICAL MEASUREMENTS AT ROOM, HIGH AND LOW TEMPERATURES</u> Electrical measurements shall be performed at room, high and low temperatures. Consolidated notes are given after the tables.
- 2.3.1 Room Temperature Electrical Measurements The measurements shall be performed at T_{amb} =+22 ±3°C.



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Characteristics	Symbols	MIL-STD-750	Test Conditions	Lin	Limits	
		Test Method		Min	Max	
Forward Voltage 1	V _{F1}	4011	Pulse Method I _F =1mA, Note 1	0.54	0.63	V
Forward Voltage 2	V _{F2}	4011	Pulse Method I _F =50mA, Note 1	0.76	0.89	V
Forward Voltage 3	V _{F3}	4011	Pulse Method I _F =100mA, Note 1	0.82	0.98	V
Forward Voltage 4	V _{F4}	4011	Pulse Method I _F =200mA, Note 1	0.87	1.1	V
Reverse Current 1	I _{R1}	4016	DC Method V _R =V _{RWM} , Note 2	-	40	nA
Reverse Current 2 (Breakdown Volt- age)	I _{R2}	4016	DC Method V _R =V _(BR) , Note 2	-	50	nA
Capacitance	С	4001	V _R = 0V V _{sig} =50mV (p-p)max f = 1MHz Note 3	-	3	pF
Reverse Recovery Time 1	t _{rr1}	4031	Test Condition A I _F = I _R = 10mA I _{rr} =1mA Note 4	-	9	ns
Reverse Recovery Time 2	t _{rr2}	4031	Test Condition A I _F = 1A, V _R = 30V dl/dt= -15A/ μ s Note 3	-	20	ns
Forward Recovery Time	t _{fr}	4026	I _F =200mA V _{fr} =1.1V _F Note 3	-	20	ns
Forward Recovery Voltage	V _{fr}	4026	I _F =200mA V _{fr} =1.1V _F Note 3	-	5	V
Thermal Impedance, Junction to Ambient	Z _{th(j-a)}	3101	$I_{H}=0.1A \text{ to } 0.3A$ $t_{H}=50\text{ms to } 10\text{s}$ $I_{M}=10\text{mA}$ $t_{MD}=100\mu\text{s}$ Note 5	Calcula see N	ate ∆V _F lote 6	°C/W

2.3.2 High and Low Temperatures Electrical Measurements

Characteristics	Symbols	ymbols MIL-STD-750 Test Conditions		Limits		Units	
		Test Method	Test Method Note 7	Note /	Min	Max	
Forward Voltage 4	V _{F4}	4011	T _{amb} =-55(+5 -0) ^o C Pulse Method I _F =200mA, Note 1	-	1.2	V	



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Characteristics	Symbols	MIL-STD-750	Test Conditions	Limits		Units
		lest Method	Note /	Min	Max	
Reverse Current 1	I _{R1}	4016	T _{amb} =+150(+0 -5) ^o C DC Method V _R =V _{RWM} , Note 2	-	30	μΑ
Reverse Current 2 (Breakdown Volt- age)	I _{R2}	4016	T_{amb} =-55(+5 -0) ^o C DC Method V _R =V _(BR) , Note 2	-	40	μA

2.3.3 <u>Notes to Electrical Measurement Tables</u>

- 1. Pulse Width \leq 680 μ s, Duty Cycle \leq 2%.
- 2. See Component Type Variants for V_{RWM} and $V_{(BR)}$ values.
- 3. Read and record measurements shall be performed on a sample of 32 components with 0 failures allowed. Alternatively a 100% inspection may be performed.
- 4. Guaranteed by t_{rr2} but not tested.
- 5. Performed only during Screening Tests Parameter Drift Values (Initial Measurements), go-no-go.
- 6. The limits for ΔVF shall be defined by the Manufacturer on every lot in accordance with MIL-STD-750 Method 3101 and shall guarantee the Rth limits specified in Maximum Ratings.
- 7. Read and record measurements shall be performed on a sample of 5 components with 0 failures allowed. Alternatively a 100% inspection may be performed.

2.4 PARAMETER DRIFT VALUES

Unless otherwise specified, the measurements shall be performed at T_{amb} =+22 ±3°C.

The test methods and test conditions shall be as per the corresponding test defined in Room Temperature Electrical Measurements.

The drift values (Δ) shall not be exceeded for each characteristic specified. The corresponding absolute limit values for each characteristic shall not be exceeded.

Characteristics	Symbols		Units		
		Drift	Abso	olute	
		Value A	Min	Max	
Forward Voltage 4	V _{F4}	±0.03	0.87	1.1	V
Reverse Current 1	I _{R1}	±10 or (1) ±100%	-	40	nA

NOTES:

1. Whichever is the greater referred to the initial value.

2.5 INTERMEDIATE AND END-POINT ELECTRICAL MEASUREMENTS Unless otherwise specified, the measurements shall be performed at T_{amb} =+22 ±3°C.



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The test methods and test conditions shall be as per the corresponding test defined in Room Temperature Electrical Measurements.

Characteristics	Symbols	Limits		Units
		Min	Max	
Forward Voltage 4	V _{F4}	0.87	1.1	V
Reverse Current 1	I _{R1}	-	40	nA
Reverse Current 2 (Breakdown Voltage)	I _{R2}	-	50	nA

2.6 HIGH TEMPERATURE REVERSE BIAS BURN-IN CONDITIONS

Characteristics	Symbols	Limits	Units
Ambient Temperature	T _{amb}	+150 (+0 -5)	°C
Reverse Voltage	V _R	0.8 x V _(BR) (Note 1)	V
Duration	t	≥ 48	hours

NOTES:

1. See Component Type Variants for $V_{(BR)}$ value.

2.7 POWER BURN-IN CONDITIONS

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	T _{amb}	+125 (+0 -5)	°C
Junction Temperature	Т _Ј	+175 (+0 -5)	°C
Average Output Rectified Current	۱ ₀	Note 1	mA

NOTES:

1. The output current may be adjusted, within the given limit range, to attain the specified junction temperature.

2.8 OPERATING LIFE CONDITIONS

The conditions shall be as specified for Power Burn-in.



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APPENDIX 'A'

AGREED DEVIATIONS FOR STMICROELECTRONICS (F)

ITEMS AFFECTED	DESCRIPTION OF DEVIATIONS
Deviations from the Generic Specification: Production Control- Chart F2	Special In-process Control Internal Visual Inspection. Wedge bonds equal to 1.1 wire diameters are acceptable for bonding with a V-Groove tool.
	Special In-process Control Internal Visual Inspection. For CCP packages the criteria specified for voids in the fillet and minimum die mounting material around the visible die perimeter for die mounting defects may be omitted providing that a radiographic inspection to verify the die-attach process is performed on a sample basis in accordance with STMicroelectronics procedure 7050651.
Deviations from the Generic Specification: Screening Tests - Chart F3	Solderability is not applicable unless otherwise stipulated in the Purchase Order.
Room Temperature Electrical Measurements	All AC characteristics (C, t_{rr2} , t_{fr} , V_{fr}) may be considered guaranteed but not tested if successful pilot lot testing has been performed in accordance with STMicroelectronics procedure 7188211 on the wafer lot, which includes AC characteristic measurements per the Detail Specification. A summary of the pilot lot testing shall be provided if required by the Purchase Order.
High and Low Temperatures Electrical Measurements	Low temperature characteristic I_{R2} may be considered guaranteed but not tested if successful pilot lot testing has been performed in accordance with STMicroelectronics procedure 7188211 on the wafer lot, which includes low temperature characteristic measurements per the Detail Specification. A summary of the pilot lot testing shall be provided if required by the Purchase Order.