DOCUMENT CHANGE REQUEST

DCR number 639	Changes required for: N/A	Originator: Samuel SAVIN
Date: 2011/06/16	Date sent: 2010/12/17	Organisation: CNES
Status: IMPLEMENTED		

Title:	Diodes Silicon Switching, based on types 1N6638, 1N6642 and 1N6643		
Number:	5101/026	Issue:	1

Other documents affected:

Page:

See attached document

Paragraph:

See attached document

Original wording:

Proposed wording:

See attached document

Justification:

Variant 07: new ST variant introduction with LCC2D package
Variant 08: new ST variant introduction with LCC2D package

Attachments:

DCR_1N6642.pdf, DCR639att.pdf, null

Modifications:

1N6642U DCR639
Approved wording if different from 'Proposed Wording' above or reason for rejection

The original attachment to this DCR, provided by STMicroelectronics, is replaced by the attached 5101/026 issue 2 Draft B.

This change wording serves to implement the new STM Variants 07 and 08 and at the same time perform a total reformat of this Detail Specification (under Generic Specification No. 5000) as part of the ongoing conversion of legacy ESA/SCC formatted specifications to the ESCC format. See below for summary of changes and attached Issue 2 Draft B of the Specification.

Note: known support for active procurement against this specification includes the following manufacturers: STMICROELECTRONICS/F are currently willing to support the procurement of new Variants 07 and 08.

MICROSEMI/I have indicated some interest in supporting some types covered by this specification. Full details are not currently available but it is expected that types 1N66XX, MIL qualified per MIL-PRF-19500/578 in various packages, may be considered. However is has been confirmed by MICROSEMI/I that existing Variants 01 to 06 are not supported in their currently specified form. It is intended to proceed with a new update of this specification in order to implement additional Variants for MICROSEMI/I once this DCR has been approved and implemented.

Summary of changes to the current format, layout and content is as follows:

a) Rewording and restructure of various sections and paragraphs of the specification plus other editorial changes based on the layout and editorial content of other Detail Specifications already converted to ESCC format, as well as changes to make the Detail specification consistent with the current ESCC Generic Specification No. 5000.

b) Removal of any redundant paragraphs and information,
e.g.: Figure 1; mechanical paragraph; Figures 4, 5(a), 5(b); Appendix A for MICROSEMI/I

c) Removal of all requirements specifically applicable to obsolete types & Variants 01 to 06, plus addition and amendment of requirements as apply to the new 1N6642U Variants 07 & 08 and for STM. This impacts the following locations in the specification:
Title page: remove reference to 1N6638, 1N6643. Only type 1N6642U now applies to this spec issue 2.
Para 1.7: delete reference to tin-lead plated lead finish
Table 1(a): delete obsolete Variants 01 to 06 and add 07 & 08 for type 1N6642U in LCC2D package
Table 1(b): Soldering Temperature, Junction Temperature, Thermal Resistance
Figure 2
Figure 3
Para 4.2 & 4.2.1 to 4.2.5: all deviations from Generic Spec are deleted.
Para 4.3.2
Para 4.3.3
Para 4.4.1, 4.4.2
Table 2
Table 3(a) & 3(b)
Table 4
Table 5(a) & 5(b)
Table 6

Details of specific technical changes are as follows (See attached 5101/026 Issue 2 Draft B for full details):

1) Table 1(b) (now Para 1.5): Forward Surge Current rating is changed to be 2A maximum (was 2.5A) based on STM characterisation data.

2) Para 4.2.2(g) additional Surge Current Test is not required (this is justified based on use of STM’s internal Pilot Lot procedure N° 7188211)

3) Table 2 Breakdown Voltage test V(BR) (now Para 2.3.1):
Test is replaced by equivalent Reverse Current test (IR3)

4) Table 2 Reverse Recovery Time 1 trr1 (now Para 2.3.1):
Test is considered guaranteed but not tested based on testing of added parameter Reverse Recovery Time 2 trr2.

5) Table 3(b) (now Para 2.3.2 & Appendix A):

Reverse Current (IR3 for Breakdown Voltage) is added (but is considered guaranteed but not tested based on STM's pilot lot testing).

6) Table 4 Breakdown Voltage test V(BR) (now Para 2.4):
Test is deleted as the specified Breakdown Voltage test does not produce a result that can be used for delta calculations (i.e. The test per MIL-STD-750 Method 4021 is effectively a go-no-go test)

7) Table 5(a) (now Para 2.6):
Duration is changed to be >=48h (was 72h) for clarification purposes.

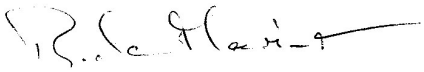
8) Table 5(b) (now Para 2.7):
Power Burn-in conditions are amended to reflect a test operating the components at junction temperature.

9) Table 6 (now Para 2.5):
Change/delta Limits for parameters are not included; only absolute limits apply.
Reverse Current (IR3 for Breakdown Voltage) is added.

10) General deviations to the ESCC Generic & Detail Specs, as already agreed in other ESCC published Detail Specs for STM, are included as Appendix A for STM.

Justification:
as above

Approval signature:



Date signed:

2011-06-16

TABLE 1(a)- Type Variants

Variant	Based on Type	Case	Figure	Breakdown Voltage $V_{(BR)}$ (V)	Repetitive peak reverse voltage V_{RRM} (V)	Working Peak Reverse Voltage V_{RWM} (V)	Lead/Terminal Material and Finish
07	1N6642U	LCC2D	2(c)	100	100	-	2
08	1N6642U	LCC2D	2(c)	100	100	-	4

Justification .

Variant 07: new ST variant introduction with LCC2D package
Variant 08: new ST variant introduction with LCC2D package

TABLE 1(b)- MAXIMUM RATINGS

N°	Characteristics	Symbols	Maximum Ratings	Unit	Remarks
1	Forward Surge Current (per Diode) Variants 01 to 06 Variants 07 to 08	IFSM	2.5 2	A(pk) A	At Tamb ≤ +25°C Note 1
3	Average Output Rectified Current Variants 01 to 06 Variants 07 to 08	IO	300 300	mA mA	Note 3 and 4 Note 7
4	Operating Temperature Range Variants 01 to 06 Variants 07 to 08 (Case Temperature)	Top Top	-65 to +175 -65 to +175	°C °C	Tamb Note 8
added	Junction Temperature Variants 07 to 08	Tj	+175	°C	
5	Storage Temperature Range Variants 01 to 06 Variants 07 to 08	Tstg	-65 to +175	°C	 Note 8
6	Soldering Temperature Variant 01 to 03 Variant 04 to 06 Variants 07 to 08	Tsol	 +260 +245 +245	°C	 Note 5 Note 6 Note 9
added	Thermal Resistance, Junction to Case Variants 07 to 08	Rth(j-c)	60	°C/W	Note 10
added	Thermal Resistance, Junction to Ambient Variants 07 to 08	Rth(j-a)	280	°C/W	

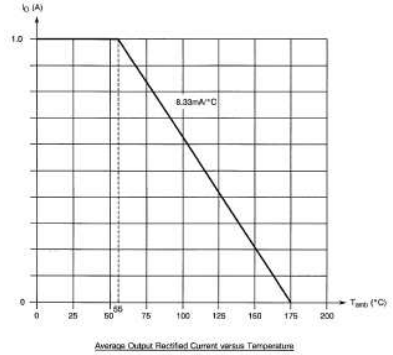
NOTES:

7. For Variants 07 to 08 at Tcase ≥ +155°C per Diode, derate linearly to 0A at +175°C.
8. For Variants with hot solder dip lead finish all testing performed at Tamb>+125°C shall be carried out in a 100% inert atmosphere.
9. Duration 5 seconds maximum. The same package must not be resoldered until 3 minutes have elapsed.
10. Package mounted on infinite heatsink.

Justification .

Variant 07: new ST variant introduction with LCC2D package
Variant 08: new ST variant introduction with LCC2D package

FIGURE 1 – PARAMETER DERATING INFORMATION (Not Applicable for the variants 07 to 08)

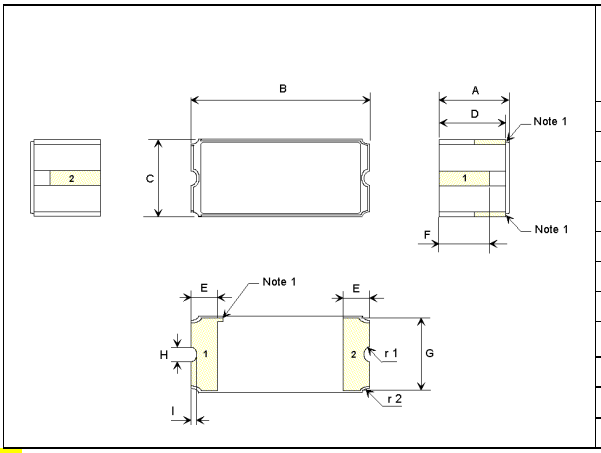


Average Output Rectified Current versus Temperature

Justification .

Variant 07: new ST variant introduction with LCC2D package
Variant 08: new ST variant introduction with LCC2D package

Figure 2(c)- Variant 07 to 08 - Leadless Chip Carrier 2 (LCC2D) – 2 Terminal

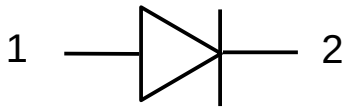


Ref	Dimensions					
	Millimeters			Inches		
	Min	Typ	Max	Min	Typ	Max
A	1.86	2.03	2.20	.073	.080	.087
B	4.44	4.57	4.77	.175	.180	.188
C	1.84	1.97	2.10	.072	.078	.083
D	1.53	1.7	1.87	.060	.067	.074
E	0.48		0.71	.019		.028
F	1.3			.051		
G	1.67			.066		
H	0.37			.015		
I	0.15			.006		
r1	0.15			.006		
r2	0.20			.008		

Notes:
1- The anode is identified by a metallization in 2 top angle castellations and by the index mark on the bottom metallization n° 1.
2- Measurement prior to solder coating the mounting pads on bottom of package.

Justification .
Variant 07: new ST variant introduction with LCC2D package
Variant 08: new ST variant introduction with LCC2D package

FIGURE 3 - FUNCTIONAL DIAGRAM
Variants 07 to 08
Terminal 1: Anode
Terminal 2: Cathode



Notes:
For LCC2, the lid is not connected to any lead.

Justification .
Variant 07: new ST variant introduction with LCC2D package
Variant 08: new ST variant introduction with LCC2D package

4.2.2 Deviations from Final Production Tests (Chart II)
(a) Para. 9.2.1, Bond Strenght Test: Not applicable.
Excepted for the variants 07 to 08 (Applicable in the Chart F2 of the ESCC N°5000 Issue 6).

(b) Para. 9.2.2, Die Shear Test: Not applicable.
Excepted for the variants 07 to 08 (Applicable in the Chart F2 of the ESCC N°5000 Issue 6).

(c) At any time following Para. 9.5.1, Thermal Shock Test, Thermal impedance measurements shall be performed in accordance with MIL-STD-750, TEST Method 3101 as specified in Table 2, item 11.
For the variants 07 to 08 (the thermal impedance is applicable in the Chart F3 of the ESCC N°5000 Issue 6).
For the variants 07 to 08 (the thermal shock is applicable in the Chart F4 Environmental Subgroup of the ESCC N°5000 Issue 6).

(d) Para. 9.6, Constant Acceleration: Not applicable.
Excepted for the variants 07 to 08 (Applicable in the Chart F4 Mechanical Subgroup of the ESCC N°5000 Issue 6).

(e) Para. 9.7 Particle Impact Noise Detection (PIND) test: Not applicable
Excepted for the variants 07 to 08 (Applicable in the Chart F3 of the ESCC N°5000 Issue 6).

(f) Para. 9.8.1, Seal Test Fine Leak: Not applicable
Excepted for the variants 07 to 08 (Applicable in the Chart F3 of the ESCC N°5000 Issue 6).

(g) ……..Excepted for the variants 07 to 08: N/A.

Justification .
Variant 07: new ST variant introduction with LCC2D package
Variant 08: new ST variant introduction with LCC2D package

4.2.3 Deviations from Burn-In and Electrical Measurements (Chart III)
(b) Para. 9.8.1 Seal Test Fine Leak: Not applicable
Excepted for the variants 07 to 08 (Applicable in the Chart F3 of the ESCC N°5000 Issue 6).

(c) Para. 9.12, Radiographic Inspection: Not applicable
Excepted for the variants 07 to 08 (Applicable in the Chart F3 of the ESCC N°5000 Issue 6).

Justification .
Variant 07: new ST variant introduction with LCC2D package
Variant 08: new ST variant introduction with LCC2D package

4.2.4 Deviations from Qualification Tests (Chart IV)
(a) Para. 9.2.3, Bond Strenght Test: Not applicable
Excepted for the variants 07 to 0 (Applicable in the Chart F4 Assembly Capability Subgroup of the ESCC N°5000 Issue 6).

(b) Para. 9.2.4, Die Shear Test: Not applicable
Excepted for the variants 07 to 08 (Applicable in the Chart F4 Assembly Capability Subgroup of the ESCC N°5000 Issue 6).

(c) Para. 9.8.1, Seal Test Fine Leak: Not applicable
Excepted for the variants 07 to 08 (Applicable in the Chart F4 Environmental and Mechanical Subgroup of the ESCC N°5000 Issue 6).

(d) Para. 9.15, Constant Acceleration: Not applicable
Excepted for the variants 07 to 08 (Applicable in the Chart F4 Mechanical Subgroup of the ESCC N°5000 Issue 6).
Justification .
Variant 07: new ST variant introduction with LCC2D package
Variant 08: new ST variant introduction with LCC2D package

4.2.5 Deviations from Lot Acceptance Tests (Chart V)
(a) Para. 9.8.1, Seal Test Fine Leak: Not applicable
Excepted for the variants 07 to 08 (Applicable in the Chart F4 F4 Environmental and Mechanical Subgroup of the ESCC N°5000 Issue 6).

(b) Para. 9.15, Constant Acceleration: Not applicable
Excepted for the variants 13 to 14 (Applicable in the Chart F4 Mechanical Subgroup of the ESCC N°5000 Issue 6).
Justification .
Variant 07: new ST variant introduction with LCC2D package
Variant 08: new ST variant introduction with LCC2D package

4.3.2 Weight
The maximum weight of the diodes specified herein shall be 0.2 grammes for the variants 01 to 03 and 0.13 grammes for variant 04 to 06 and 0.12 grammes for the variants 07 to 08.
Justification .
Variant 07: new ST variant introduction with LCC2D package
Variant 08: new ST variant introduction with LCC2D package

4.3.3 Terminal Strength
For the variants 07 to 08 as specified in the ESCC Generic Specification (Applicable in the Chart F4 Assembly Capability Subgroup of the ESCC N°5000 Issue 6).
Justification .
Variant 07: new ST variant introduction with LCC2D package
Variant 08: new ST variant introduction with LCC2D package

4.4.1 Case
The case shall be hermetically sealed and have an Aln body with kovar lid for the variants 07 to 08.
Justification .
Variant 07: new ST variant introduction with LCC2D package
Variant 08: new ST variant introduction with LCC2D package

4.4.2 Lead Material and Finish
For the variants 07 to 08 leads/terminals as specified in the Table 1a.
Justification .
Variant 07: new ST variant introduction with LCC2D package
Variant 08: new ST variant introduction with LCC2D package

4.5.1 General
For the variants 07 to 08 the marking shall be in accordance with the requirements of ESCC Basic Specification No. 21700 and as follows.
The information to be marked on the component shall be:
(a) Polarity.
(a) The ESCC qualified components symbol (for ESCC qualified components only).
(b) The ESCC Component Number.

(c) Traceability information.

Justification .

Variant 07: new ST variant introduction with LCC2D package
Variant 08: new ST variant introduction with LCC2D package

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE D.C.PARAMETERS

N°	Characteristics	Symbols	MIL-STD-750 Test Method	Test Conditions	Limits		Units
					Min	Max	
1	Breakdown Voltage	$V_{(BR)}$	4021	I_R=-100µA Variants 01 to 06 Variants 07 to 08	 Note1 100	 - -	 V V
2	Forward Voltage	V_{F1}	4011	Pulse Method I_F=10mA, Variants 07 to 08 (Note 2)	 -	 0.8	 V
3	Forward Voltage	V_{F2}	4011	Pulse Method I_F=100mA, Variants 07 to 8 (Note 2)	 -	 1.2	 V
4	Reverse Current	I_{R1}	4016	DC Method V_R=20V Variant 07 to 08	 -	 25	 nA
5	Reverse Current	I_{R2}	4016	DC Method V_R=75V Variant 07 to 08	 -	 50	 nA

Notes

1. See Colum 5 of Table 1(a).
2. For variant 01 to 06 pulsed measurement: tp = 5.0ms maximum
   For variant 07 t o 08 Pulse Width ≤ 680µs; Duty Cycle ≤ 2%
3. See Colum 6 of Table 1(a).

Justification .

Variant 07: new ST variant introduction with LCC2D package
Variant 08: new ST variant introduction with LCC2D package

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - A.C. PARAMETERS

N°	Characteristics	Symbols	MIL-STD-750 Test Method	Test Conditions	Limits		Units
					Min	Max	
added	Junction Capacitance	C_{J1}		V_R=0Vdc Vsig=50mV(p-p)max f=1MHz **(Note 4)** Variants 07 to 08	-	5	pF
added	Junction Capacitance	C_{J2}		V_R=0Vdc Vsig=50mV(p-p)max f=1MHz **(Note 4)** Variants 07 to 08	-	2.8	pF
8	Reverse Recovery Time	Trr1	4031 Cond. 'A'	I_F=I_{RM}=10 to 100mA I_{RR}=10% of I_{RM} (Note 1) **(Note 4 and 5)** Variants 07 to 08	 -	 9	nS
		Trr2	4031 Cond. 'A'	I_F = 1A; V_R =30V DI/dt=-15A/µS **(Note 4)** Variants 07 to 08	-	20	nS
9	Forward Recovery Time	t_{FR}	4026	I_F = 50mA (Note 1 and 2) Variants 01 to 06 I_F = 2000mA **(Note 4)** Variants 07 to 08	 -	 20 20	nS
10	Forward Recovery Voltage	V_{FR}	4026	I_F = 50mA (Note 1 and 2) Variants 01 to 06 I_F = 200mA **(Note 4)**	 -	 5	V

				Variants 07 to 08	-	5	
11	Thermal Impedance	$Z_{TH(J-C)}$	3101	Variants 01 to 06 only			
added	Thermal Impedance	$Z_{TH(J-C)}$	3101	Variants 07 to 08 I_H=0.1 to 0.3A t_H=50ms to 10s I_M=10mA t_{md}=100µs **(Note 6)**	Calculate ΔVF, **(see Note 7)**		°C/W

NOTES

4) See appendix A [Agreed Deviations for STMicroelectronics (F)]
5) Test parameter trr1 is not tested but guaranteed by trr2.
6) Performed only during Screening Tests Parameter Drift Values (Initial Measurements), go-no-go.
7) The limits for ΔVF shall be defined by the Manufacturer on every lot in accordance with MIL-STD-750 Method 3101 and shall guarantee the Rth(j-a) limits specified in Maximum Ratings.

Justification .

Variant 07: new ST variant introduction with LCC2D package
Variant 08: new ST variant introduction with LCC2D package

TABLE 3(a) - ELECTRICAL MEASUREMENTS AT HIGH TEMPERATURES

N°	Characteristics	Symbols	MIL-STD-750 Test Method	Test Conditions	Limits		Units
					Min	Max	
2	Forward Voltage	V_{F1}	4011	I_F=10mA (Note 1) Variants 01, 02, 04, 05 Variants 03, 06 Tamb=+150(+0-5)°C Pulse Method I_F=10mA Variants 07 to 08 (Note 3, 4)	 - - -	 0.65 0.80 0.80	 V
4	Reverse Current	I_{R1}	4016	DC Method V_R= -20V Variants 01, 02, 04, 05 Variants 03, 06 Tamb=+150(+0-5)°C Variants 07 to 08 (Note 4)	 - - -	 50 75 30	µA
5	Reverse Current	I_{R2}	4016	DC Method V_R= Note2 Variants 01, 02, 04, 05 Variants 03, 06 Tamb=+150(+0-5)°C V_R= 75V Variants 07 to 08 (Note 4)	 - - -	 100 160 40	µA

NOTES

3. Pulse Width≤ 680µs; Duty Cycle ≤ 2%
4. Read and record measurements shall be performed on a sample of 5 components with 0 failures allowed. Alternatively a 100% inspection may be performed.

Justification .

Variant 07: new ST variant introduction with LCC2D package
Variant 08: new ST variant introduction with LCC2D package

TABLE 3(b) - ELECTRICAL MEASUREMENTS AT LOW TEMPERATURES

N°	Characteristics	Symbols	MIL-STD-750 Test Method	Test Conditions	Limits		Units
					Min	Max	
1	Forward Voltage	V_{F2}	4011	I_F=200mA (Note 1) Variants 01, 04 I_F=100mA (Note 1) Variants 02, 05 Variants 03, 06 Pulse Method , Tamb=-55(+5-0)°C I_F=100mA Variants 07 to 08 (Note 2, 3)	 - - - -	 1.2 1.2 1.4 1.2	 V

NOTES
2. Pulse Width≤ 680µs; Duty Cycle ≤ 2%
3. Read and record measurements shall be performed on a sample of 5 components with 0 failures allowed. Alternatively a 100% inspection may be performed.

TABLE 4 PARAMETER DRIFT VALUES FOR VARIANTS 07 T08

Characteristics	Symbols	Limits			Units
		Drift Value Δ	Absolute Min	Absolute Max	
Reverse Current 1	I_{R2}	+/-10 or +/-100%	-	50	nA
Forward Voltage 1	V_{F2}	+/-50	-	1200	mV

Note:
1. Whichever is the greater referred to the initial value.

Justification .
Variant 07: new ST variant introduction with LCC2D package
Variant 08: new ST variant introduction with LCC2D package

TABLE 5(a) CONDITION FOR HIGH TEMPERATURE REVERSE BIAS BURN-IN

N°	Characteristics	Symbols	Conditions	Units
2	Reverse Voltage Variants 07 to 08	V_R	 80 (80% of V_{RRM})	V
3	Duration Variants 01 to 06 Variants 07 to 08	 t t	 72 ≥48	 Hours Hours

Justification .
Variant 07: new ST variant introduction with LCC2D package
Variant 08: new ST variant introduction with LCC2D package

TABLE 5(c) - CONDITIONS FOR POWER BURN-IN AND OPERATING LIFE TESTS FOR VARIANTS 07 T08

N°	Characteristics	Symbols	Test Conditions	Units
1	Ambient Temperature	Tamb	+125 (+0/-5)	°C
2	Junction Temperature	Tj	+175 (+0 -5)	°C
3	Average Output Rectified Current	IO	**Note 2**	A

NOTES:
2. The output current may be adjusted, within their given limit ranges, to attain the specified junction temperature.

Justification .
Variant 07: new ST variant introduction with LCC2D package
Variant 08: new ST variant introduction with LCC2D package

TABLE 6 - ELECTRICAL MEASUREMENTS AT INTERMEDIATE POINTS AND ONCOMPLETION OF ENDURANCE TESTING FOR VARIANTS 07 T08

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS (	ABSOLUTE MIN.	ABSOLUTE MAX.	UNIT
3	D.C Forward Voltage 1	V_{F2}	As per Table 2	As per Table 2	-	1.2	V
5	Reverse Current	I_{R2}	As per Table 2	As per Table 2	-	50	nA

Justification .
Variant 07: new ST variant introduction with LCC2D package
Variant 08: new ST variant introduction with LCC2D package

APPENDIX 'B'
AGREED DEVIATIONS FOR STMICROELECTRONICS (F)

ITEMS AFFECTED	DESCRIPTION OF DEVIATIONS
Deviations from Production Control-Chart F2	Internal Visual Inspection: Wedge bonds equal to 1.1 wire diameter are acceptable for bonding with a V-Groove tool.
Deviations from Production Control-Chart F2	Special In-process Control Internal Visual Inspection. For CCP packages the criteria specified for voids in the filet and minimum die mounting material around the visible die perimeter for die mounting defects may be omitted providing that a radiographic inspection to verify the die-attach process is performed on a sample basis in accordance with STMicroelectronics procedure 7050651.
Deviations from Screening Tests- Chart F3	Solderability is not applicable unless otherwise stipulated in the Purchase Order.
Deviations from Room	Test parameter the reverse recovery time trr1 is not tested but guaranteed by trr2.

Temperature Electrical Measurements	AC characteristics (t_{fr2}, C, t_{fr}, V_{fr}), may be considered guaranteed but not tested if successful pilot lot testing has been performed in accordance with STMicroelectronics procedure 7188211 on the wafer lot, which includes AC characteristic measurements per the Detail Specification. A summary of the pilot lot testing shall be provided if required by the Purchase Order.

Justification .

Variant 07: new ST variant introduction with LCC2D package

Variant 08: new ST variant introduction with LCC2D package

DIODE, SILICON, SWITCHING

BASED ON TYPE 1N6642U

ESCC Detail Specification No. 5101/026

Issue 2 Draft C	March 2011

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DOCUMENTATION CHANGE NOTICE

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DCR No.	CHANGE DESCRIPTION
DCR639	Specification up issued to incorporate editorial and technical changes per DCR.

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1. GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics and test and inspection data for the component type variants and/or the range of components specified below. It supplements the requirements of, and shall be read in conjunction with, the ESCC Generic Specification listed under Applicable Documents.

1.2 APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:

(a) ESCC Generic Specification No. 5000
(b) MIL-STD-750, Test Methods and Procedures for Semiconductor Devices

1.3 TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESCC Basic Specification No. 21300 shall apply.

1.4 THE ESCC COMPONENT NUMBER AND COMPONENT TYPE VARIANTS

1.4.1 The ESCC Component Number

The ESCC Component Number shall be constituted as follows:

Example: 510102607

- Detail Specification Reference: 5101026
- Component Type Variant Number: 07

1.4.2 Component Type Variants

The component type variants applicable to this specification are as follows:

Variant Number	Based on Type	Case	Breakdown Voltage $V_{(BR)}$ (V)	Working Peak Reverse Voltage V_{RWM} (V)	Terminal Finish	Weight max g
07	1N6642U	LCC2D	100	75	2 (Note 1)	0.12
08	1N6642U	LCC2D	100	75	4	0.12

NOTES:
1. With electrolytic nickel underplating.

The terminal finish shall be in accordance with the requirements of ESCC Basic Specification No. 23500

1.5 MAXIMUM RATINGS

The maximum ratings shall not be exceeded at any time during use or storage.

Maximum ratings shall only be exceeded during testing to the extent specified in this specification and when stipulated in Test Methods and Procedures of the ESCC Generic Specification.

Characteristics	Symbols	Maximum Ratings	Unit	Remarks
Forward Surge Current	I_{FSM}	2	A	Notes 1, 2
Working Peak Reverse Voltage	V_{RWM}	Note 3	V	
Average Output Rectified Current	I_O	300	mA	Note 4
Operating Temperature Range (Case Temperature)	T_{op}	-65 to +175	^oC	Note 5
Junction Temperature	T_j	+175	^oC	
Storage Temperature Range	T_{stg}	-65 to +175	^oC	Note 5
Soldering Temperature	T_{sol}	+245	^oC	Note 6
Thermal Resistance, Junction to Case	$R_{th(j-c)}$	60	$^oC/W$	Note 7
Thermal Resistance, Junction to Ambient	$R_{th(j-a)}$	280	$^oC/W$	

NOTES:

1. Sinusoidal pulse of 8.3ms duration.
2. At $T_{amb} \leq +25^oC$.
3. See Component Type Variants for V_{RWM} value.
4. At $T_{case} \geq +155°C$, derate linearly to 0A at +175°C.
5. For Variants with hot solder dip lead finish all testing and any handling performed at $T_{amb} > +125^oC$ shall be carried out in a 100% inert atmosphere.
6. Duration 5s maximum and the same package shall not be resoldered until 3 minutes have elapsed.
7. Package mounted on an infinite heat sink.

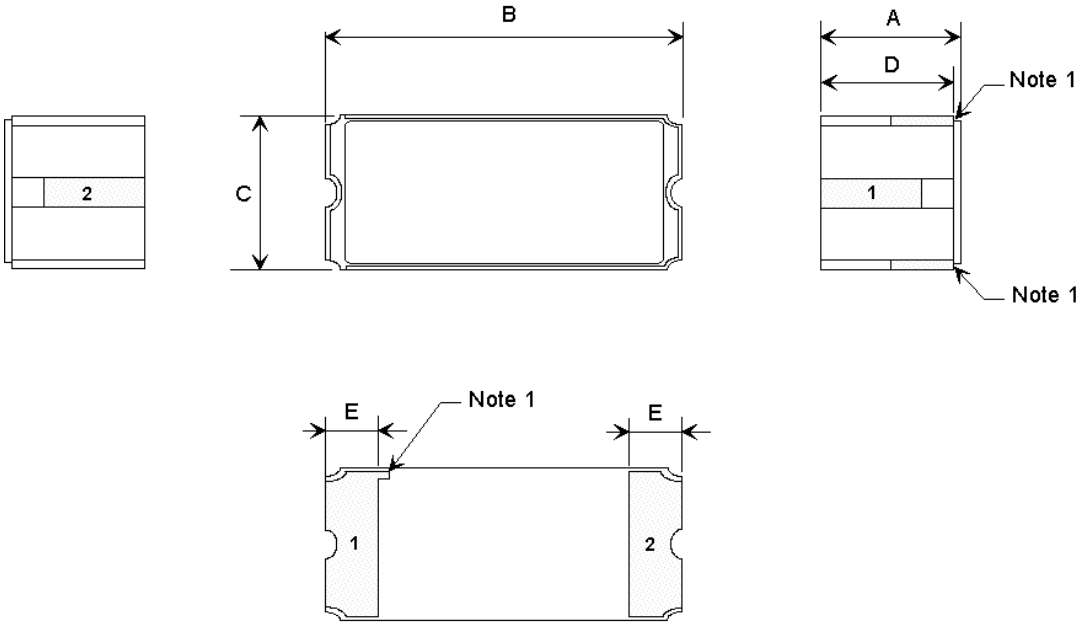
1.6 HANDLING PRECAUTIONS

These devices are susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacture, testing, packaging, shipment and any handling.

These components are categorised as Class 3 per ESCC Basic Specification No. 23800 with a Minimum Critical Path Failure Voltage of 5800 Volts.

1.7 PHYSICAL DIMENSIONS AND TERMINAL IDENTIFICATION

1.7.1 Leadless Chip Carrier Package (LCC2D) - 2 Terminal



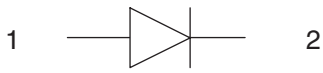
Symbols	Dimensions mm		Notes
	Min	Max	
A	1.86	2.2	2
B	4.44	4.77	
C	1.84	2.1	
D	1.53	1.87	
E	0.48	0.71	

NOTES:

1. Terminal identification: The anode is identified by metallisation in the two castellations and by the index mark on the bottom metallisation.
2. For Variant 08 dimension limits apply prior to solder coating of terminals.

1.8 FUNCTIONAL DIAGRAM

Terminal 1: Anode
Terminal 2: Cathode



NOTES:
1. For LCC2D the lid is not connected to any terminal.

1.9 MATERIALS AND FINISHES

Materials and finishes shall be as follows:

a) Case
The case shall be hermetically sealed and have an Aluminium Nitride body with a Kovar lid.
b) Terminal Finish
As specified in Component Type Variants.

2. REQUIREMENTS

2.1 GENERAL

The complete requirements for procurement of the components specified herein are as stated in this specification and the ESCC Generic Specification. Permitted deviations from the Generic Specification, applicable to this specification only, are listed below.

Permitted deviations from the Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESCC requirement and do not affect the component's reliability, are listed in the appendices attached to this specification.

2.1.1 Deviations from the Generic Specification

None

2.2 MARKING

The marking shall be in accordance with the requirements of ESCC Basic Specification No. 21700 and as follows.

The information to be marked on the component shall be:

(a) Terminal Identification.
(b) The ESCC qualified components symbol (for ESCC qualified components only).
(c) The ESCC Component Number.
(d) Traceability information.

2.3 ELECTRICAL MEASUREMENTS AT ROOM, HIGH AND LOW TEMPERATURES

Electrical measurements shall be performed at room, high and low temperatures. Consolidated notes are given after the tables.

2.3.1 Room Temperature Electrical Measurements

The measurements shall be performed at T_{amb}=+22 ±3°C.

Characteristics	Symbols	MIL-STD-750 Test Method	Test Conditions	Limits		Units
				Min	Max	
Forward Voltage 1	V_{F1}	4011	Pulse Method I_F=10mA, Note 1	-	0.8	V
Forward Voltage 2	V_{F2}	4011	Pulse Method I_F=100mA, Note 1	-	1.2	V
Reverse Current 1	I_{R1}	4016	DC Method V_R= 20V	-	25	nA
Reverse Current 2	I_{R2}	4016	DC Method V_R=V_{RWM}, Note 2	-	50	nA
Reverse Current 3 (Breakdown Voltage)	I_{R3}	4016	DC Method V_R=$V_{(BR)}$, Note 2	-	60	nA
Capacitance 1	C_1	4001	V_R = 0V V_{sig}=50mV (p-p)max f = 1MHz Note 3	-	5	pF
Capacitance 2	C_2	4001	V_R = 1.5V V_{sig}=50mV (p-p)max f = 1MHz Note 3	-	2.8	pF
Reverse Recovery Time 1	t_{rr1}	4031	Test Condition A I_F= I_R= 10mA I_{rr}=1mA Note 4	-	9	ns
Reverse Recovery Time 2	t_{rr2}	4031	Test Condition A I_F= 1A, V_R = 30V dI/dt= -15A/µs Note 3	-	20	ns
Forward Recovery Time	t_{fr}	4026	I_F=200mA V_{fr}=1.1V_F Note 3	-	20	ns
Forward Recovery Voltage	V_{fr}	4026	I_F=200mA V_{fr}=1.1V_F Note 3	-	5	V
Thermal Impedance, Junction to Ambient	$Z_{th(j-a)}$	3101	I_H= 0.1A to 0.3A t_H= 50ms to 10s I_M= 10mA t_{MD}= 100µs Note 5	(Calculate ΔV_F, see Note 6)		°C/W

2.3.2 High and Low Temperatures Electrical Measurements

Characteristics	Symbols	MIL-STD-750 Test Method	Test Conditions Note 7	Limits		Units
				Min	Max	
Forward Voltage 1	V_{F1}	4011	T_{amb}=+150(+0 -5)°C Pulse Method I_F=10mA, Note 1	-	0.8	V

Characteristics	Symbols	MIL-STD-750 Test Method	Test Conditions Note 7	Limits		Units
				Min	Max	
Forward Voltage 2	V_{F2}	4011	T_{amb}=-55(+5 -0)°C Pulse Method I_F=100mA, Note 1	-	1.2	V
Reverse Current 1	I_{R1}	4016	T_{amb}=+150(+0 -5)°C DC Method V_R=20V	-	30	µA
Reverse Current 2	I_{R2}	4016	T_{amb}=+150(+0 -5)°C DC Method V_R=V_{RWM}, Note 2	-	40	µA
Reverse Current 3 (Breakdown Voltage)	I_{R3}	4016	T_{amb}=-55(+5 -0)°C DC Method V_R=$V_{(BR)}$, Note 2	-	50	µA

2.3.3 Notes to Electrical Measurement Tables

1. Pulse Width ≤680µs, Duty Cycle ≤2%.
2. See Component Type Variants for V_{RWM} and $V_{(BR)}$ values.
3. Read and record measurements shall be performed on a sample of 32 components with 0 failures allowed. Alternatively a 100% inspection may be performed.
4. Guaranteed by t_{rr2} but not tested.
5. Performed only during Screening Tests Parameter Drift Values (Initial Measurements), go-no-go.
6. The limits for ΔVF shall be defined by the Manufacturer on every lot in accordance with MIL-STD-750 Method 3101 and shall guarantee the Rth limits specified in Maximum Ratings.
7. Read and record measurements shall be performed on a sample of 5 components with 0 failures allowed. Alternatively a 100% inspection may be performed.

2.4 PARAMETER DRIFT VALUES

Unless otherwise specified, the measurements shall be performed at T_{amb}=+22 ±3°C.

The test methods and test conditions shall be as per the corresponding test defined in Room Temperature Electrical Measurements.

The drift values (Δ) shall not be exceeded for each characteristic specified. The corresponding absolute limit values for each characteristic shall not be exceeded.

Characteristics	Symbols	Limits			Units
		Drift Value Δ	Absolute		
			Min	Max	
Forward Voltage 2	V_{F2}	±0.03	-	1.2	V
Reverse Current 2	I_{R2}	±10 or (1) ±100%	-	50	nA

NOTES:
1. Whichever is the greater referred to the initial value.

2.5 INTERMEDIATE AND END-POINT ELECTRICAL MEASUREMENTS

Unless otherwise specified, the measurements shall be performed at T_{amb}=+22 ±3°C.

The test methods and test conditions shall be as per the corresponding test defined in Room Temperature Electrical Measurements.

Characteristics	Symbols	Limits		Units
		Min	Max	
Forward Voltage 2	V_{F2}	-	1.2	V
Reverse Current 2	I_{R2}	-	50	nA
Reverse Current 3 (Breakdown Voltage)	I_{R3}	-	60	nA

2.6 HIGH TEMPERATURE REVERSE BIAS BURN-IN CONDITIONS

Characteristics	Symbols	Limits	Units
Ambient Temperature	T_{amb}	+150 (+0 -5)	°C
Reverse Voltage	V_R	0.8 x $V_{(BR)}$ (Note 1)	V
Duration	t	≥ 48	hours

NOTES:
1. See Component Type Variants for $V_{(BR)}$ value.

2.7 POWER BURN-IN CONDITIONS

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	T_{amb}	+125 (+0 -5)	°C
Junction Temperature	T_J	+175 (+0 -5)	°C
Average Output Rectified Current	I_O	Note 1	mA

NOTES:
1. The output current may be adjusted, within the given limit range, to attain the specified junction temperature.

2.8 OPERATING LIFE CONDITIONS

The conditions shall be as specified for Power Burn-in.

APPENDIX 'A'

AGREED DEVIATIONS FOR STMICROELECTRONICS (F)

ITEMS AFFECTED	DESCRIPTION OF DEVIATIONS
Deviations from the Generic Specification: Production Control-Chart F2	Special In-process Control Internal Visual Inspection. Wedge bonds equal to 1.1 wire diameters are acceptable for bonding with a V-Groove tool.
	Special In-process Control Internal Visual Inspection. For CCP packages the criteria specified for voids in the fillet and minimum die mounting material around the visible die perimeter for die mounting defects may be omitted providing that a radiographic inspection to verify the die-attach process is performed on a sample basis in accordance with STMicroelectronics procedure 7050651.
Deviations from the Generic Specification: Screening Tests - Chart F3	Solderability is not applicable unless otherwise stipulated in the Purchase Order.
Room Temperature Electrical Measurements	All AC characteristics (C_1, C_2, t_{rr2}, t_{fr}, V_{fr}) may be considered guaranteed but not tested if successful pilot lot testing has been performed in accordance with STMicroelectronics procedure 7188211 on the wafer lot, which includes AC characteristic measurements per the Detail Specification. A summary of the pilot lot testing shall be provided if required by the Purchase Order.
High and Low Temperatures Electrical Measurements	Low temperature characteristic I_{R3} may be considered guaranteed but not tested if successful pilot lot testing has been performed in accordance with STMicroelectronics procedure 7188211 on the wafer lot, which includes low temperature characteristic measurements per the Detail Specification. A summary of the pilot lot testing shall be provided if required by the Purchase Order.