DOCUMENT CHANGE REQUEST

DCR number 701	Changes required for: General	Originator: Steve Thacker
Date: 2014/10/13	Date sent: 2010/11/24	Organisation: ESTEC
Status: IMPLEMENTED		

Title:	Generic Specification for Discrete Microwave Semiconductor Components		
Number:	5010	Issue:	1

Other documents affected:

Page:

Paragraph:

Original wording:

Specification completely rewritten; all pages-paragraphs are affected

Proposed wording:

Specification is proposed to be extensively amended to incorporate various policy, technical & editorial amendments & corrections in order to bring it in line with other ESCC Generic Specifications that have already been converted to the new ESCC format.
In the case of ESCC5010, ESCC5000 is the most similar Generic specification; it has been used as a baseline reference for this DCR.

The layout, format and general structure, and editorial content of 5010 issue 2 draft H are based closely on ESCC 5000 issue 6 per DCRs 149, 236, 286, 313 & 399 (all approved).

The proposed technical content of ESCC5010 draft 2H is based on the current content of ESCC5010 issue 1 plus amendments discussed and agreed by the ESA 5010 Working Group (made up of representatives from ESA and the Manufacturers: Tyco(MaCom)/UK, Infineon/D & Cobham(Chelton)/F).

This DCR summarises all the amendments to 5001 issue 1 plus identifies the additional editorial & technical changes to ESCC 5010 issue 1 not already generally detailed and justified by DCRs 149/236/286/313/399.

For full details of the proposed contents of ESCC 5010 issue 2 see the attached 5010 issue 2 draft H.

Change Details:

A) Main General changes (similar to those already incorporated into ESCC5000 issue 6):

1) The SCC testing level C has been deleted; there is now only a single ESCC testing level, equivalent to old SCC level B.

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2) Qualification and Lot Acceptance Testing have been incorporated, with some modifications, into a single Chart F4, Qualification and Periodic Tests. Modifications include:
- Periodic testing is mandatory for ESCC qualified components with a defined testing schedule.
- Lot Acceptance Testing has been deleted but an Orderer option for similar Lot Validation Testing, for procurement, has been added. Lot Validation Testing is not mandatory (except for procurement of Naked Die Components) and will only be done if specifically stipulated by the Orderer in the PO. The requirement for LAT level 3 as a minimum for non-qualified component procurement is removed.
- No failures are allowed during Chart F4 testing

3) Introduction of Technology Flow Qualification per ESCC No. 25400 to the generic spec.

4) Introduction of ESCC 23100 (ESCC Recommendations on the use of the ESCC Specification System for the Evaluation and Procurement of Unqualified Components) to the generic spec.

5) The Specification has been made applicable and fully usable for procurement of unqualified components (including unqualified Naked Die Components), as well as for ESCC Qualified components.

6) Clarification that the term PID is specific to ESCC qualified components.

7) The minimum required delivered documentation to the customer for procurement is a Certificate of Conformity & a Cover sheet .

8) Clarification of Customer Source inspection options for Pre-Cap & Buy-off where the Customer & Manufacturer mutually agree what is to be performed and how much notification is required.

9) The maximum allowed delay for Lot failure notification (provided by the Manufacturer) is now 5 working days (was 2).

10) Chart F2, Special In-Process Controls, is defined to include the tests from assembly to encapsulation (internal visual, bond strength & die shear, dimension check & weight). Assembly includes definition of the Packaged Test Sublot for naked die procurement.

11) The General Flow Chart F1 has been redrawn to clarify the flow of components for Procurement (including separate Charts for Packaged Components - F1A, & Naked Die Components - F1B).

12) Final Production Tests & Burn-in and Electrical Measurements, Charts II, III(a) & III(b), have been incorporated, with some modifications, into a single Chart F3, Screening Tests. Final Production tests prior to encapsulation are added to Chart F2, Special In-Process Controls.

13) Optional and recommended tests from Final Production Tests (i.e. Electrical at Room Temperature, Seal, Pre-burn-in, Electrical at High & Low Temperatures) are deleted. If any additional testing to the ESCC standard is actually required it will be specified in the detail spec.

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14) Bond Strength test condition: add note about test condition B (in line with ESCC 5000 & Mil-STD-750):
Test Condition B shall only be permitted when Test Condition A cannot be used and never for bond wires of diameter less than 0.127mm.

15) High Temperature Stabilisation Bake duration, during final Production tests, has been changed from 48 hours to 24 hours and changed from being optional to is required. If HTSB is not required this deviation will be specified in the Detail spec.

16) Thermal Shock during Screening tests and Qualification/LVT testing is modified to align the conditions with the equivalent as specified for ESCC 5000 & JANS devices per MIL-PRF-19500 i.e. Temperature Cycling per MIL-STD-750.

17) Solderability testing has been clarified to allow the use of suitable empty packages.

18) Any sampling requirements have been amended to specify the actual fixed sample size and accept criteria rather than by a reference to a sampling plan.

19) Correction of the Screening PDA calculation. The reference quantity for PDA should be all electrically good parts going into the first burn-in (excluding any failures to the initial electrical). The current spec incorrectly defines the reference quantity as the quantity tested at initial electrical.

20) When using the ESCC System to procure components from an unqualified source and marking the parts with the ESCC component number, the Manufacturer should possess a manufacturing and quality assurance system that is compatible with space application. As such, the user expectation should be that parts would be compatible with passing the testing requirements of Chart F4. Accordingly the requirement placed on qualified sources to not knowingly supply components that cannot meet the Chart F4 testing is extended to unqualified sources.

21) Material outgassing reference document is corrected to be ECSS-Q-ST-70-02.

B) Other Editorial and/or Technical Changes (specific to ESCC5010):

22) The spec has been amended to clarify the requirements applicable to Naked Die Components procurement (as opposed to Packaged Components procurement) including:
- Allow procurement of Naked Die components even if the Packaged version of the component is not ESCC qualified (5010 currently implies this is not allowed). A mandatory LVT 1000hours Life Test shall be performed on each wafer lot per Chart F4 for all (qualified or unqualified) Naked Die component procurements.
- Allow radiation testing during procurement of Naked Die components (5010 currently does not specifically allow this)
- Clarify that Die visual inspection can be performed during customer pre-encapsulation source inspection for Naked Die Components.
- Definition of the Packaged Test Sublot (the assembled dice used for Screening and Qual level testing).
- Sampling for Naked Die Components is clarified to ensure the minimum required quantity of packaged dice is presented to Screening at the 1st burn-in and for Chart F4 testing.

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- The check for lot failure requirement applicable to Naked Die components during Screening has been clarified (currently this subject is not clear in 5010 for Naked Die).
- A PDA check after initial electrical on the Packaged Test Sublot (PDA0=10%) has been added to confirm user yield.
- Clarify that Naked Die procurement shall be traceable to the wafer number (as well as the wafer lot).
- Clarify that marking and data applicable to Naked Die should also include the wafer number.
- Clarify that Packaged Components should be hermetically sealed (i.e. spec title is amended).
- Clarify the Bond Strength & Die Shear sampling requirements.

23) Wafer Screening is incorporated into Wafer Lot Acceptance in Chart F2, Production Control (editorial change)

24) The requirements for total dose radiation testing and the radiation test level have been clarified. The device dependant irradiation requirements table has been deleted from the generic specification (only a very limited range of types are included in the table which is therefore considered of little use). The radiation test requirement details, if applicable, will be specified in the detail spec. This includes the possibility of performance of radiation testing as part of the ESCC qualification testing.

25) Introduction of SEE radiation testing requirements per ESCC 25100 into the generic specification. The current spec does not refer to SEE testing, which is applicable to some discrete MW semiconductors. SEE radiation testing is implemented in the same way as currently applies to total dose radiation testing (i.e. as part of Wafer Lot Acceptance).

26) The burn-in details are amended to have Burn-in 1 & 2 (rather than HTRB & Power Burn-in). The details applicable to which category of component is subjected to which burn-in & in which order, is deleted. Burn-in details will be fully specified in the Detail spec. (This simplifies the content of the generic spec but still allows full flexibility for the burn-ins; Only guidance is currently specified for the definition of the 2 categories (1 & 2). Without a clear complete definition it is best to allow the Detail spec to define the Burn-in requirements for each component).

27) Special Testing has been deleted from Qualification testing (as it is currently undefined). Any special testing requirements, if specified, will be specified in the Detail spec as applicable.

28) Reference documents that are not actually referenced in 5010 are removed.
i.e. MIL-STD-105, MIL-STD-202, MIL-STD-414

29) Alternate test conditions for Die Shear, when the test is impractical, shall be specified in the Detail Spec.

30) Wafer level electrical measurements are to be as specified in the Detail spec as an on-wafer or after dice separation test. It is clarified that Wafer level electrical measurements at room, high and low temperatures are performed on a GONOGO basis.

31) Intermediate data point for 3000hour Qual Life test is at 1000hours (not 1500hours). This makes the intermediate data point the same as for the end of the LVT life test.

32) The Period applicable to the Endurance subgroup for Periodic Testing in Chart F4 is set at 24 months (instead of the ESCC standard 12 months) as decided by the ESA Working Group (linked to the facts that the ESCC maintenance of

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qualification period is 24 months and that any given wafer lot will yield enough die to meet the typical space customer demand for over a much longer period than 1 or 2 years.)

Justification:

All changes have been defined and included to serve the purposes of technical improvement, clarification, accuracy, completeness, simplification and consistency.
The aim is to simplify and improve the content and interpretation of the specification and its requirements whilst maintaining an acceptable technical baseline and the same overall structure as the current ESCC 5010 issue 1.

In addition 5010 issue 2 draft H is written to closely follow the layout, format and content of the latest ESCC 5000 issue 6. The justifications for the related policy and editorial changes given in all other previous DCRs related to ESCC 5000 issue 6 (i.e. DCRs 149, 236, 286, 313, 399) also apply to this DCR.

Justification and explanation for the additional changes that apply specifically to ESCC 5010 issue 1 are as given in each change item above (where not considered an editorial change).

Attachments:

5010.pdf, 5010_issue_2_draft_j_for_pswg_review.pdf

Modifications:

This DCR has been extensively reviewed by the PSWG members (: ESA, Thales Alenia Space, Astrium, Tesat-Spacecom) who have agreed changes to be incorporated as part of this DCR.

The following changes & additions to the original DCR text/items apply:

The draft specification that applies to this DCR that incorporates all final changes and replaces the original attachment, is ESCC5010 issue 2 draft J.

DCR Item 2) & 22):

Chart F4 (Qualification and Periodic Tests) is split into 2 separate charts:

- F4A for Packaged Components
- F4B for Naked Die Components. Chart F4B clarifies which tests apply specifically to Naked Die Components (i.e. only Endurance Subgroup plus new De-encapsulation Subgroup applies),

Lot Validation Testing (the Endurance subgroup of Chart F4B (with 1000h operating life test) on each wafer lot) is only mandatory for procurement of ESCC qualified Naked Die Components. LVT requirements for unqualified Naked Die Components are undefined (the same as for to Packaged Components); LVT only applies when deemed necessary by the customer and stipulated in the Purchase Order.

DCR item 22):

The lot identification information relevant to marking & data documentation is clarified to include wafer and wafer lot numbers.

DCR item 25):

This item is deleted from the DCR (SEE requirements are not to be included in this Generic spec as is consistent with other ESCC Generic specs; e.g. 9000)

New DCR item 33) (& item 31):

The Operating life test duration for Qualification Testing is amended to be 2000 hours (was 3000 hours [in Para. 9.20.1]; to be consistent with ESCC9010)

New DCR item 34):

PIND testing during Screening Tests [in Chart II(b)] shall be performed on Naked Die Components (i.e. on all Packaged Test Sublot samples) (to ensure no risk of PIND related problems occurring during Qualification testing, Periodic Testing & Lot Validation Testing). However the PIND lot failure criteria [in Para. 9.7] shall be limited to rejection of the Packaged Test Sublot (not to rejection of the complete wafer lot)

Similarly, Radiographic Inspection, Seal testing and External Visual Inspection during Screening Tests [in Charts III(a) & III(b)] shall be performed on Naked Die Components (i.e. on all the Packaged Test Sublot samples) (to ensure no risk of any related problems occurring during Qualification testing, Periodic Testing & LVT).

New DCR Item 35):

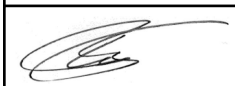
Internal Visual Inspection plus Bond Pull & Die Shear testing during Qualification testing [in Chart IV] is also made applicable to Periodic Testing (MoQ) in charts F4A & F4B for all components, with a period of 24 months (to assess any impact at die level of the various Chart F3 & F4 testing)

The samples to be tested (in the new De-encapsulation subgroup) shall be selected as follows:

- For Packaged Components: 6 samples (2 direct from Screening Tests; 2 from successful Chart F4A Environmental & Mechanical Subgroup testing; 2 from successful Chart F4A Endurance Subgroup testing)

- For Naked Die Components: 4 samples (2 direct from Screening Tests; 2 from successful Chart F4B Endurance Subgroup testing)

Approval signature:



Date signed:

2014-10-13