ESCC QUALIFIED MANUFACTURERS LIST (QML)

Issue 31	December 2025

Document Custodian: European Space Agency – see https://escies.org

LEGAL DISCLAIMER AND COPYRIGHT

DOCUMENTATION CHANGE NOTICE

(Refer to https://escies.org for ESCC DCR content)

DCR No.	CHANGE DESCRIPTION
1786	**Extension:** 356C Exxelia SAS, France 357C Microchip Technology, France 359C Microchip Technology, France **New:** 394 ST Microelectronics, France The ST ASIC platform 28nm FDSOI has been qualified. The first ESCC-qualified product based on this technology is the NG-ULTRA NX2H540TSC, a radiation-hardened-by-design SoC FPGA supplied by NanoXplore.

FOREWORD

This document contains a list of qualified manufacturers that have been certified by the European Space Agency for technology flows to the rules of the ESCC system with principle reference to ESCC Basic Specification no. 25400.

The qualified electronic components produced from the technology flows are intended for use in ESA and other spacecraft and associated equipment in accordance with the requirements of the ECSS standard ECSS-Q-ST-60.

Each technology flow qualification and its subsequent maintenance is monitored and overseen by the ESCC executive. ESA certifies the qualification upon receipt of a formal application from the executive stating that all applicable ESCC requirements have been met by the pertinent manufacturer. The qualified status of a technology flow is noted by an entry in this document, a corresponding entry in the European space components information exchange system, ESCIES, and the issue of a certificate to the qualified manufacturer.

TABLE OF CONTENTS

1 PROMOTION

It is permitted to advertise the ESCC qualification status of a component provided such publicity or advertisement does not state or imply that the component is the only qualified one of that particular type, range or family.

2 PROCURER'S RESPONSIBILITY

When procuring ESCC qualified components, the procurer is responsible for ensuring that the qualification status is valid and that delivered components fulfil the specified requirements of the applicable ESCC specifications. The procurer is advised to utilise the ESCC non- conformance system, per ESCC Basic Specification No. 22800, in the event that a qualified manufacturer delivers non-conforming components.

3 QML ORGANISATION

3.1 TECHNOLOGY FLOWS AND PROCESS CAPABILITY APPROVALS (PCA)

The individual Technology Flows and PCA and are listed in this document by manufacturer in alphabetical order. They may also be found on the ESCIES web site, https://escies.org. A Technology Flow Abstract is provided to describe the main features of the qualified Technology Flow.

3.2 QUALIFIED COMPONENTS

Under each technology flow a list of the qualified components is provided.

3.3 TYPE DESIGNATION

Wherever possible the referenced type (style) designations are derived from industrial standards. Where no standardised type designation is applicable the manufacturer's designation is referenced.

3.4 COMPONENT CHARACTERISTICS

The precise characteristics of the qualified component are defined in the referenced ESCC Detail specifications.

3.5 MANUFACTURER

Contact information and plant locations are indicated in the individual Technology Flow listings Contact information may also be found in the ESCC QML section of the ESCIES web site, https://escies.org.

4 TABLE OF QUALIFIED COMPONENT TECHNOLOGY

Components	Sub-section	Manufacturers	Certificates
05 Filters	SAW	Kongsberg Defence & Aerospace	313F
08 Microcircuits	Digital C-MOS: ATC18RHA	Microchip Technology Nantes	357C
	Digital C-MOS: ATMX150RHA	Microchip Technology Nantes	359C
	ASIC platform C65Space	STMicroelectronics	381A
	ASIC platform 28nm FDSOI	STMicroelectronics	394
	GaN HEMT	United Monolithic Semiconductors	388
10 Resistors	Chip	Vishay SA, Sfernice	287J
14 Transformers	Custom magnetics: linear or toroidal technology	Exxelia Magnetics	356C
	Custom Magnetics (Inductors, Chokes and Transformers)	Flux A/S	364A

5 QUALIFIED TECHNOLOGY FLOWS

The following technology flows are qualified.

5.1 FILTERS (05)

5.1.1 KONSBERG DEFENCE & AEROSPACE, Norway: SAW FILTERS

5.1.1.1 Contact Information

Address	ESCC Chief Inspector
Kongsberg Defence & Aerospace Knutsrødveien 7 N-3189 Horten Norway	Mrs Cecilie Berg Tel: (+47) 3303 2700 Fax: (+47) 3303 2800 email: cecilie.berg@norspace.no

5.1.1.2 Qualification

Current Qualification Certificate No.	In QML since:	Type Designation
313F	Aug. 2011	SAW filters (transversal band pass/resonator/notch/low loss impedance element)

APPLICABLE ESCC DOCUMENTS:

ESCC Generic Specification No. 3502
ESCC Detail Specification Nos. 3502/002

NORSPACE PROCESS IDENTIFICATION DOCUMENTS:

PID534_9 SAW Device Assembly with flow NORSF-A1
PID630_9 SAW Crystal Manufacturing with flow NORSF-C1

5.1.1.3 List of Qualified Components

For each design, a detail specification is produced by Kongsberg Space Electronics. Where the SAW component is not proprietary to the customer the detail specification is published in ESCIES as a supporting document. Available detail specifications are found in the table below.

Detail Specification	Component Type
3502/002	SAW Filters, Hermetically Sealed, Surface Mount, Frequency Range 10 MHz - 4 GHz

5.1.1.4 Technology Flow Abstract

General features

The Technology Flow covers the design, fabrication, assembly, screening, in-process control and testing of the Norspace SAW filters manufactured within the NORSF-C1 and NORSF-A1 processes. The design, crystal manufacturing, assembly, screening and testing is performed in Kongsberg Space Electronics facility at Knudsrødveien 7 in Horten, Norway.

Technology Flow	Scope
Design	Norspace specification Ko 03.00
Crystal manufacturing	Process flow NORSF-C1 on purchased SAW-grade surface polished wafers. Wafer materials: Quartz (SiO_2), Lithium niobate ($LiNbO_3$), Lithium tantalate ($LiTaO_3$), Langasite ($La_3Ga_5SiO_{14}$) Wafer dimensions: 3” diameter 0.5 mm thick 3” diameter 1.0 mm thick 4” diameter 1.5 mm thick
Assembly	Process flow NORSF-A1. Crystal dimensions: from 1.7 mm x 3.1 mm up to 8 mm x 76 mm. Packages: -Gold plated Fe-Ni-Co-alloy flat packs. From 4 up to 50 leads with ceramic or glass feedthroughs. External wings for screw attach on some types Package dimensions: From 8 mm x 8 mm up to 85 mm x 12 mm. -Gold plated Fe-Ni-Co-alloy flat packs with Cu-W base, 4 or 6 leads and ceramic feedthroughs. Package dimensions: From 11 mm x 11 mm up to 7 mm x 21 mm. -Gold plated ceramic Leadless Chip Carrier (LCC) package, 10 solder pads. Package dimension: 5 mm x 7 mm.
Screening and Test	Process flow NORSF-A1. –Incoming inspection –In-process inspection –100% Wafer probe electrical test –100% Visual inspection –Final production tests –Customer Source Inspection –Screening –Burn-in and electrical measurements –Test procedures –External visual inspection –Qualification testing

Basic Information

The SAW devices are passive devices and typically require external tuning. Frequency range: From 10 MHz up to 4 GHz.

Max operating temperature range: -30 / +85 °C (maximum), -20 / +70 °C (typical).

Input power: design sensitive.

Component Types

- Transversal band pass SAW filters with frequencies up to 4 GHz.
- SAW Resonator filters
- SAW Notch filters
- Impedance element filters with low loss

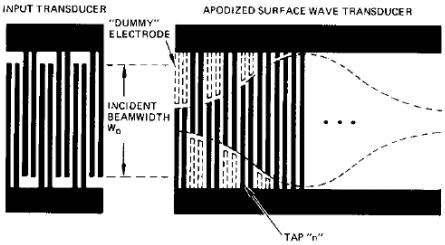
5.1.1.5 Technology Flow definition

1. Design

The design programs are in-house developed procedures and libraries. Each new design is custom made for the application by Kongsberg Space Electronics design engineers. The design centre is in Horten, Norway.

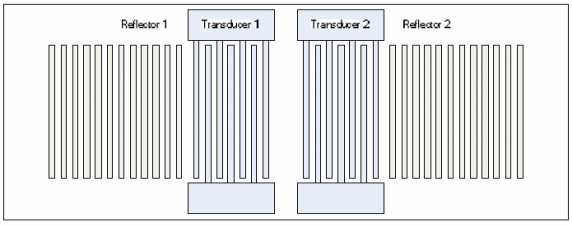
Transversal band pass SAW filters

The transversal filters consist of one input transducer and one output transducer, see figure below. The transducers are interdigital transducers formed by a metal pattern on a piezoelectric material (wafer). The transducers can be withdrawal weighted and/or length (apodization) weighted. The detailed weighting functions are calculated in a dedicated filter synthesis software and used as input to the mask layout software. The simulation of the filter response is performed by a dedicated SAW Analysis software.



Resonator filters

The resonator filter consists of input and output transducers as described above. These are normally unweighted. The transducers are backed by reflectors, see figure below. The reflectors are l/4 wide etched grooves or metal fingers. The same software is used for simulation of the transducers and reflectors.

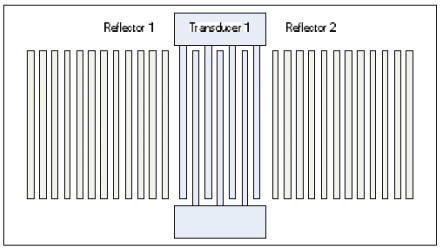


SAW Notch filters

The notch are based on single port resonator elements, so called impedance elements (see below).

Impedance element filters with low loss

Impedance element filters are constructed from one port SAW resonators. The one port SAW resonators consist of one interdigital transducer backed by one reflector on each side, as shown in the figure below.



2. Fabrication

The NORSF-C1 process at Kongsberg Space Electronics comprises:

- SAW crystal manufacturing on SAW grade polished single crystal wafers from quartz, LiNbO3, LiTaO3 and La3Ga5SiO14 (langasite)
- Externally purchased SAW wafers
- SAW wafer thickness between 0.5 mm and 1.5 mm
- Photolithography with line widths down to 0.3 m. No upper limit.Metallization performed with Al or Cr/Al. Metal thickness 400 to 10 000 Å.

The process can manufacture SAW elements of band pass, resonator or notch type with centre frequencies in the range 10 MHz to 4 GHz.

3. Assembly

Norspace assembly flow NORSF-A1 technology flow covers the following capabilities:

Package	Die Attach	Wire Bond	Lid Seal	Leads
Flatpack/LCC. Au plated. CuW base/Fe-Ni-Co alloy or ceramic with Fe-Ni-Co alloy seal ring.	Silicone rubber	Ultrasonic ball- wedge, 25 µm Au wire	Resistance seam sealing. N2 atmosphere.	Au plated

4. Test

Measurements are performed using a Vector Network Analyzer (VNA).

All equipment in the electrical test set-up shall have the same characteristic impedance. The S-parameters are measured on the VNA and transferred to a PC for post-processing and analysis. Before testing the VNA and its test cables must be calibrated as specified in the manual for the instrument (full 2-port calibration).

Test vehicles used for qualification: SQF-3800, SLC-4320.
Test vehicles used for maintenance: SQF-3800, SLC-3900, or similar devices.

5. Radiation

The devices are regarded as radiation insensitive within a small drift in centre frequency and phase allowed for in the design margins.

Radiation testing has been performed successfully up to 50 MRad(Si) for quartz and 1 MRad(Si) for LiNbO3, LiTaO3 and Langasite.

Qualified wafer materials: Quartz, LiNbO3. LiTaO3, Langasite (La3Ga5SiO1)

5.2 MICROCIRCUITS (08)

5.2.1 Microchip Technology, France: ATC18RHA

5.2.1.1 Contact Information

Address	ESCC Chief Inspector
Microchip Technology Nantes Route de Gachet 44300 Nantes France	Ms V. Lepaludier Tel. +33 2 40 18 1633 FAX +33 2 40 18 1946 Valerie.Lepaludier@microchip.com

5.2.1.2 Qualification

Current Qualification Certificate No.	In QML since:	Type Designation
357C	May 2019	Integrated Circuits, Silicon, Monolithic, CMOS, Cell-Based Array, based on Type ATC18RHA

Remarks:

Certificate 357 supersedes previous certificate 312B Rev1. New certificate reflects significant changes in the supply chain.

An End-Of-Life of the ATC18RHA ASIC offer for new design has been announced by Microchip in January 2021. Detail is available in Microchip Notification CRS20-0158 (information added in QML issue 22, published in March 2021). ATMX150RHA ASICs is to be used as replacement for any new design. Microchip will stop wafer manufacturing launch by December 2021. Microchip commits to maintain the wafer/die stock, based on customer needs. Microchip will continue Flight Models manufacturing from this wafer/die stock.

Applicable documents:

ESCC Generic Specification No. 9000; ESCC Detail Specification No. 9202/080

ATC18RHA Process Identification Document PID 0032 Rev G, MMT assembly PID 1G-QM-0105 and HCM columns manufacturing and assembly PID 11 issue F.

5.2.1.3 List of Qualified Components

For each ASIC design an ASIC Sheet is produced by Microchip for use in conjunction with the ESCC Detail Specification No. 9202/080. Where the ASIC is not proprietary to the customer the ASIC sheet is published in ESCIES as a supporting document.

ASIC Sheet	Component Type

In the case of ATC18RHA, standard components are also available. These are listed below with their full ESCC Detail Specification:

Detail Specification	Component Type
9512/004	Integrated Circuits, Silicon, 32-bit SPARC Processor, based on Type AT697F
9512/005	Integrated circuits, silicon monolithic, SPARC V8 GNSS controller based on type AT7991

5.2.1.4 Technology Flow Abstract

GENERAL FEATURES

ATC18RHA standard cells family is designed with a 0.18µm radiation hard CMOS technology. This offering is based on 6 metal layers at 1.8V +/-0.15V for the core and 3.3V +/-0.3V for the periphery. This family features arrays with up to 7 Mgates and 544 pads. With its high speed performance, its low supply current and its radiation hard level, the ATC18RHA is suitable for digital applications working in radiation intensive environment.

BASIC INFORMATION

- CMOS technology AT58KRHA
- 40 to 70 kgates per mm²
- Periphery power supply 3.3V and 2.5V
- Core power supply 1.8V
- Low supply current :
  - Operating maximum value: 85nW/gate/MHz with a duty cycle at 20%
- I/O Interfaces:
  - Cold sparing
  - High speed LVDS (655 Mps) and LVPECL
  - PCI
- 544 pads (+ 8 pads power only)
- Embedded memories: Compiled and Synthesized
- EDAC library
- Radiation :
  - No Single Event Latch-Up below a LET Threshold of 80 MeV/mg/cm² at high temperature
  - SEU hardened DFF's to 30 MeV/mg/cm2
  - Tested up to 300 krad (Si), Radiation Level is 100 krads (Si).

COMPONENT TYPES

Device Types as per ESCC Detail Specification 9202/080 and individual custom ESCC ASIC Sheets.

Die	Supply Voltage I/O / core	Max programmable I/O's	Case	Typical Routable gates
ATC18RHA_216	2.5V or 3.3V/1.8V	216	CQFP-F256	1M
ATC18RHA_216	2.5V or 3.3V/1.8V	216	CQFP-F196	1M

Die	Supply Voltage I/O / core	Max programmable I/O's	Case	Typical Routable gates
ATC18RHA_216	2.5V or 3.3V/1.8V	216	CQFP-F160	1M
AT697F	3.3V/1.8V	-	CQFP-F256	0.85M
ATC18RHA_324	2.5V or 3.3V/1.8V	324	CQFP-F352	2.2M
ATC18RHA_324	2.5V or 3.3V/1.8V	324	CQFP-F256	2.2M
ATC18RHA_324	2.5V or 3.3V/1.8V	324	CQFP-F196	2.2M
ATC18RHA_324	2.5V or 3.3V/1.8V	324	CQFP-F160	2.2M
ATC18RHA_324	2.5V or 3.3V/1.8V	324	CLGA-349	2.2M
ATC18RHA_324	2.5V or 3.3V/1.8V	324	CCGA-349	2.2M
ATC18RHA_404	2.5V or 3.3V/1.8V	404	CQFP-T352	3.5M
ATC18RHA_404	2.5V or 3.3V/1.8V	404	CQFP-T256	3.5M
ATC18RHA_404	2.5V or 3.3V/1.8V	404	CLGA-472	3.5M
ATC18RHA_404	2.5V or 3.3V/1.8V	404	CLGA-349	3.5M
ATC18RHA_404	2.5V or 3.3V/1.8V	404	CCGA-472	3.5M
ATC18RHA_404	2.5V or 3.3V/1.8V	404	CCGA-349	3.5M
ATC18RHA_504	2.5V or 3.3V/1.8V	504	CQFP-T352	5.5M
ATC18RHA_504	2.5V or 3.3V/1.8V	504	CQFP-F256	5.5M
ATC18RHA_504	2.5V or 3.3V/1.8V	504	CLGA-625	5.5M
ATC18RHA_504	2.5V or 3.3V/1.8V	504	CLGA-472	5.5M
ATC18RHA_504	2.5V or 3.3V/1.8V	504	CLGA-349	5.5M
ATC18RHA_504	2.5V or 3.3V/1.8V	504	CCGA-625	5.5M
ATC18RHA_504	2.5V or 3.3V/1.8V	504	CCGA-472	5.5M
ATC18RHA_504	2.5V or 3.3V/1.8V	504	CCGA-349	5.5M
AT7991	3.3V/1.8V	-	CQFP-352	7.6M
ATC18RHA_544	2.5V or 3.3V/1.8V	544	CLGA-625	7M
ATC18RHA_544	2.5V or 3.3V/1.8V	544	CCGA-625	7M

5.2.1.5 Technology Flow Definition

The Technology Flow Definition domain covers the design, fabrication, assembly and testing of the ATC18RHA standard cells family.

1. Design

The design manual and the ASIC library data books cover the design in the Microchip Technology Nantes associated Design Centers (Nantes-France, Milan-Italy, Garching-Germany and Winnersh-UK).

- ATC18RHA Design manual ATD-DE-GR-R0212
- ATC18RHA TOS manual ATD-DE-GR-R0324
- ATC18RHA Buffers library databook ATD-TS-LR-R0252

- ATC18RHA Cells library databook ATD-TS-LR-R0251
- ATC18RHA Memory cells library databook ATD-TS-LR-R0254
- ATC18RHA specific library databook ATD-TS-LR-R0253

All ASIC designs will be performed by the customer at the customer site, with Microchip supported tools (front end).
No new design is proposed on this ASIC technology, replaced by the ATMX150RHA.

2. Fabrication

The ATC58KRHA, processed in UMC Taiwan, is a 0.18µm CMOS, 6 metal, Ti, TiN and AlCu process.
From 2021 December, wafer fabrication shall not be maintained. Flight models shall be manufactured from wafer in stock.

3. Assembly

The assembly of ATC18RHA devices is performed in MMT, Thailand, with the following capabilities:

- Die attach Cyanate Ester (JM7000)
- Wire bond Ultrasonic Wedge, 25 and 32 µm Al
- Lid sealing Brazed with Au/Sn alloy or seam welded
- Leads/pads Gold plated (CQFP and CLGA)

The assembly of columns is performed in SERMA HCM, La Rochelle, with the following capabilities:

- Columns 85Pb15Sn with Tinned Copper ribbon, 0.38 mm diameter

4. Control and Test

The control and test of ATC18RHA devices is performed in Microchip technology Nantes. It includes Lot Acceptance, Test Flows and Test Procedures, Qualification Test and Reliability Monitoring, Screening and associated electrical tests and inspections.

5. TCVs and SEC

The die ATC18RHA_324 is used for both test vehicles. All details are described in the ATC18RHA test chip specification, reference ADF-DE-R0561-CUP.

V56 TEST VEHICLE
The V56 is a buffer test vehicle representative of the range of buffers available for performance testing in the CQFP 256 package. It contains standard IO33 buffers, specific IO33 buffers (LVDS, PCI), a PLL, a set of ring oscillators made of different library cells and a set of interconnect lines.

V40 (5 METAL LAYERS) OR V52 (6 METAL LAYERS) TEST VEHICLE – TECHNOLOGY SEC
The V40/V52 SEC is developed for performance and radiation testing in the CQFP 256 package. It contains a set of memory blocks (compiled memories with and without EDACs and synthesized (on gates) memories made with standard and hardened latches), shift registers chains and a PLL.

6. Radiation Characteristics

The AT58KRHA family has been developed to fulfil the following characteristics:

- No Single Event Latch-up below a LET Threshold of 80MeV/mg/cm2 at high temperature
- Availability of SEU hardened cells
- Total dose capability over 100 krads(Si)

5.2.1.6 Manufacturing sites

DESIGN:
Microchip Technology Nantes, BP70602, 44306 Nantes Cedex 3, France

WAFER FABRICATION:
UMC Fab 8S, Hsin-Chu, Taiwan

DIE ASSEMBLY:
MMT, Microchip Technology (Thailand) Co., Ltd. 17/2 Moo 18 Suwintawong Road, Saladang, Bangnumpriew Chachoengsao, Thailand 24000

CCGA COLUMN ASSEMBLY:
HCM SYSTREL, 34 Av. Joliot Curie, ZI Perigny, 17185 Perigny Cedex, France

CONTROL AND TEST:
Microchip Technology Nantes, BP70602, 44306 Nantes Cedex 3, France

5.2.2 Microchip Technology, France: ATMX150RHA

5.2.2.1 Contact Information

Address	ESCC Chief Inspector
Microchip Technology Nantes Route de Gachet 44300 Nantes France	Ms V. Lepaludier Tel. +33 2 40 18 1633 FAX +33 2 40 18 1946 Valerie.Lepaludier@microchip.com

5.2.2.2 Qualification

Current Qualification Certificate No.	In QML since:	Type Designation
359C	May 2019	Integrated Circuits, Silicon, Monolithic, CMOS, Cell-Based Array, based on ATMX150RHA ASIC family.

Remark:

Certificate 359 supersedes previous certificate 342 Rev1. New certificate reflects significant changes in the supply chain.

An End-Of-Life of the ATMX150RHA ASIC offer for new design has been announced by Microchip in April 2025. Information added in QML issue 31. Microchip will stop wafer manufacturing launch by October 2025. Microchip commits to maintain the wafer/die stock, based on customer needs. Microchip will continue Flight Models manufacturing from this wafer/die stock.

APPLICABLE DOCUMENTS:
ESCC Generic Specification No. 9000; ESCC Detail Specification No. 9202/083

Microchip Process Identification Document PID 37 Rev G, MMT PID 1G-QM-0105, HCM columns manufacturing and assembly PID 11 issue F.

5.2.2.3 *List of Qualified Components*
For each ASIC design an ASIC Sheet is produced by Microchip for use in conjunction with the ESCC Detail Specification No. 9202/083. Where the ASIC is not proprietary to the customer the ASIC sheet is published in ESCIES as a supporting document.

ASIC Sheet	Component Type

5.2.2.4 *Technology Flow Abstract*

GENERAL FEATURES
The ATMX150RHA is a mixed-signal ASIC offer providing high-performance and high-density solutions for space applications. The ATMX150RHA standard cells family is designed with a 0.15µm radiation-hardened CMOS technology. This offer is based on a 5 metal layers with an optional 6th thick metal layer technology, dedicated for large ASIC's to avoid voltage drop issues. The core is supplied at 1.8V +/-0.15V and the periphery at 3.3V +/-0.3V or 2.5V +/- 0.2V. This family features arrays with up to 22 Mgates and more than 700 pads. With its high-speed performance, its low supply current and its radiation hardening level, the ATMX150RHA is suitable for digital applications working in radiation intensive environment.

BASIC INFORMATION
- CMOS technology AT77K9RHA
- 40 to 70 kgates per mm²
- Periphery power supply 3.3V and 2.5V
- Core power supply 1.8V
- Low supply current: Operating maximum value: 8.8 nA/gate/MHz with a duty cycle at 20%
- I/O Interfaces:
    - Cold sparing
    - High speed LVDS (655 Mps) and LVPECL
    - PCI
- 704 pads (+ 8 pads power only)
- Compiled memory cells (ROM, SRAM, DPRAM, register files)
- Pre-qualified IP's
    - a regulator 1.8V 200mA Linear Voltage Regulator REG200RHA
    - a 8-channels analog input multiplexer MUX8RHA
    - a PLL 40 to 450 MHz PLL400MRHA
    - a RC Oscillator4/8/10/12 MHz OSCRC10MRHA
    - a bandgap 1.215V reference BG1V2RHA

- Radiation:
    - No Single Event Latchup to a LET threshold of 67.7 MeV.cm²/mg, and up to 78. 2 MeV.cm²/mg, 30°-tilted at high temperature.
    - SEU Hardened DFF's to 30 MeV/mg/ cm2
    - Tested up to 300 kRads(Si).

COMPONENT TYPES

Device Types as per ESCC Detail Specification 9202/083 and individual custom ESCC ASIC Sheets:

Die	Supply Voltage I/O / core	Max programmable I/O's	Case	Typical Routable gates
ATMX150RHA_216	2.5V or 3.3V/1.8V	216	CQFP-256	1M
ATMX150RHA_216	2.5V or 3.3V/1.8V	216	CQFP-132	1M
ATMX150RHA_324	2.5V or 3.3V/1.8V	324	CQFP-352	2.2M
ATMX150RHA_324	2.5V or 3.3V/1.8V	324	CQFP-256	2.2M
ATMX150RHA_324	2.5V or 3.3V/1.8V	324	CQFP-132	2.2M
ATMX150RHA_324	2.5V or 3.3V/1.8V	324	CLGA-472	2.2M
ATMX150RHA_324	2.5V or 3.3V/1.8V	324	CCGA-472	2.2M
ATMX150RHA_404	2.5V or 3.3V/1.8V	404	CQFP-352	3.5M
ATMX150RHA_404	2.5V or 3.3V/1.8V	404	CQFP-256	3.5M
ATMX150RHA_404	2.5V or 3.3V/1.8V	404	CLGA-625	3.5M
ATMX150RHA_404	2.5V or 3.3V/1.8V	404	CLGA-472	3.5M
ATMX150RHA_404	2.5V or 3.3V/1.8V	404	CCGA-625	3.5M
ATMX150RHA_404	2.5V or 3.3V/1.8V	404	CCGA-472	3.5M

Die	Supply Voltage I/O / core	Max programmable I/O's	Case	Typical Routable gates
ATMX150RHA_504	2.5V or 3.3V/1.8V	504	CQFP-352	5.5M
ATMX150RHA_504	2.5V or 3.3V/1.8V	504	CQFP-256	5.5M
ATMX150RHA_504	2.5V or 3.3V/1.8V	504	CLGA-625	5.5M
ATMX150RHA_504	2.5V or 3.3V/1.8V	504	CLGA-472	5.5M
ATMX150RHA_504	2.5V or 3.3V/1.8V	504	CCGA-625	5.5M
ATMX150RHA_504	2.5V or 3.3V/1.8V	504	CCGA-472	5.5M
ATMX150RHA_544	2.5V or 3.3V/1.8V	544	CQFP-352	6.5M
ATMX150RHA_544	2.5V or 3.3V/1.8V	544	CQFP-256	6.5M
ATMX150RHA_544	2.5V or 3.3V/1.8V	544	CLGA-625	6.5M
ATMX150RHA_544	2.5V or 3.3V/1.8V	544	CLGA-472	6.5M
ATMX150RHA_544	2.5V or 3.3V/1.8V	544	CCGA-625	6.5M
ATMX150RHA_544	2.5V or 3.3V/1.8V	544	CCGA-472	6.5M
ATMX150RHA_604	2.5V or 3.3V/1.8V	604	CQFP-352	7.5M
ATMX150RHA_604	2.5V or 3.3V/1.8V	604	CLGA-896	7.5M
ATMX150RHA_604	2.5V or 3.3V/1.8V	604	CLGA-625	7.5M
ATMX150RHA_604	2.5V or 3.3V/1.8V	604	CCGA-896	7.5M
ATMX150RHA_604	2.5V or 3.3V/1.8V	604	CCGA-625	7.5M
ATMX150RHA_644	2.5V or 3.3V/1.8V	644	CQFP-352	8.7M

Die	Supply Voltage I/O / core	Max programmable I/O's	Case	Typical Routable gates
ATMX150RHA_644	2.5V or 3.3V/1.8V	644	CLGA-896	8.7M
ATMX150RHA_644	2.5V or 3.3V/1.8V	644	CLGA-625	8.7M
ATMX150RHA_644	2.5V or 3.3V/1.8V	644	CCGA-896	8.7M
ATMX150RHA_644	2.5V or 3.3V/1.8V	644	CCGA-625	8.7M
ATMX150RHA_704	2.5V or 3.3V/1.8V	704	CQFP-352	10.4M
ATMX150RHA_704	2.5V or 3.3V/1.8V	704	CLGA-896	10.4M
ATMX150RHA_704	2.5V or 3.3V/1.8V	704	CLGA-625	10.4M
ATMX150RHA_704	2.5V or 3.3V/1.8V	704	CCGA-896	10.4M
ATMX150RHA_704	2.5V or 3.3V/1.8V	704	CCGA-625	10.4M

5.2.2.5 Technology Flow Definition

The Technology Flow covers the design, fabrication, assembly and testing of the ATMX150RHA standard cells ASIC family.

1. Design

The design manual and the ASIC library data books cover the design in the Microchip Technology Nantes associated Design Centers (Nantes and Rousset-France, Milan-Italy, Garching-Germany and Winnersh-UK).

ATMX150RHA design manual	2012_EC_054_ELE
ATMX150RHA TOS (Test Oriented Simulation) Manual	ATD-DE-GR-R0324
ATMX150RHA supply & ESD buffer databook	2012_EC_055_ELE
ATMX150RHA buffer 3.3V databook	2012_EC_051_ELE
ATMX150RHA buffer 2.5V databook	2012_EC_052_ELE
ATMX150RHA Cells library databook	2012_EC_050_ELE
ATMX150RHA memory cells library databook	2012_EC_053_ELE
ATMX150RHA power grid verification flow	2014_EC_131-ELE

All ASIC designs will be performed by customer at customer site, with Microchip supported tools (front end).

2. Fabrication

The AT77K9RHA, processed in UMC Taiwan, is a 0.15 µm CMOS, 5-metal with an optional 6th thick metal, Ti, TiN and AlCu process.

3. Assembly

The assembly of ATMX150RHA devices is performed in MMT, Thailand, with the following capabilities:

- Die attach Cyanate Ester (JM7000)
- Wire bond Ultrasonic Wedge, 25 and 32 µm Al
- Lid sealing Brazed with Au/Sn alloy or seam welded
- Leads/pads Gold plated (CQFP and CLGA)

The assembly of columns on CLGA is performed in SERMA HCM, La Rochelle, with the following capabilities:

- Columns 85Pb15Sn with Tinned Copper ribbon, 0.38 mm diameter

4. Control & Test

The control and test of ATMX150RHA devices is performed in Microchip Technology Nantes.

It includes Lot Acceptance, Test Flows and Test Procedures, Qualification Test and Reliability Monitoring, Screening and associated electrical tests and inspections.

5. TCVs and SEC

002NY TEST VEHICLE
The 002NY is a buffer test vehicle representative of the range of buffers available for performance testing in the CQFP-352 package. It contains standard IO33 buffers, specific IO33 buffers (LVDS, PCI), a PLL, a set of ring oscillators made of different library cells and a set of interconnect lines.

002PF TEST VEHICLE
The 002PF is a test vehicle representative of the IP blocks available for performance testing in the CQFP-256 package. It contains the REG200RHA, the OSCR10MRHA, the MUX8RHA, the BG1V2RHA and the PLL400MRHA.

002OP TEST VEHICLE – TECHNOLOGY SEC
The 002OP SEC is developed for radiation testing, process stability, reliability monitoring and performance characterization, it is assembled in the CQFP-352 package. It contains a set of memory blocks (compiled memories with and without EDACs), shift registers chains, high speed LVDS, PCI buffers and a PLL. It uses the thick-metal layer option.

002MS TEST VEHICLE – TECHNOLOGY SEC
The 002MS has the same characteristics than the 002OP, without the thick-metal layer option. 002MS will be embarked on MPW (Multi-Project Wafer) instead of 002OP when MPW ASIC's do not need thick metal layer. When so, 002MS shall be used for reliability quarterly monitoring.

6. Radiation Characteristics

The AT77K9RHA technology has been developed to fulfil the following characteristics:

- Total dose capability over 100 kRads (Si).
- No Single Event Latchup to a LET threshold of 67.7 MeV.cm²/mg, and up to 78.2 MeV.cm²/mg, 30° tilted at high temperature.
- Availability of SEU hardened cells.

5.2.2.6 Manufacturing sites

DESIGN:
Microchip Technology Nantes, BP70602, 44306 Nantes Cedex 3, France

WAFER FABRICATION:
UMC Fab 8C, Hsin-Chu, Taiwan

DIE ASSEMBLY:
MMT, Microchip Technology (Thailand) Co., Ltd. 17/2 Moo 18 Suwintawong Road, Saladang, Bangnumpriew Chachoengsao, Thailand 24000

CCGA COLUMN ASSEMBLY:
SERMA Microelectronics, 34 Av. Joliot Curie, 17185 Perigny Cedex, France

CONTROL AND TEST:

Microchip Technology Nantes, BP70602, 44306 Nantes Cedex 3, France

5.2.3 ST Microelectronics, France: ASIC platform C65Space

5.2.3.1 Contact Information

Address	ESCC Chief Inspector
STMicroelectronics (Tours) SAS 3 rue de Suisse 35200 Rennes France	Ms Emmanuelle Guerinel Tel. +33 2 99 26 4800 emmanuelle.guerinel@st.com
	ASICs QA Project Manager
	M. Jean-Noël LETRILLARD Tel. +33 2 99 26 4800 ext : 4937 jean-noel.letrillard@st.com

5.2.3.2 Qualification

Current Qualification Certificate No.	In QML since:	Type Designation
381A	Aug 2022	Integrated Circuits, Silicon, Monolithic, CMOS Radiation Hardened 65nm ASIC Platform, based on type C65Space

Applicable documents:

ESCC Generic Specification No. 9000; ESCC Detail Specification No. 9202/086

STMicroelectronics Process Identification Documents:

- 8097046: GENERIC PID Ref. ST.01.2008

- DM00508779: PID FOR ASICs C65S WB and FC

- DM00508782: PID ASICs C65Space WB and FC Die Layout

5.2.3.3 List of Qualified Components

Component Number	Detail Specification	Generic part number	Circuit function	FPGA Matrix	Package
930401001A	9304/010	NX1H35AS-CQ352	3M System gate field programmable gate array	NX1H35AS	CQFP-352

5.2.3.4 Technology Flow Abstract

GENERAL FEATURES

The CMOS 65nm SPACE is a silicon technology node, 8 metal layers. It provides a logic capacity with additional DSPs, a 400 Mbs SpaceWire physical interface and also a DDR 2/3 physical interface. Benefiting from an advanced underlying technology, the NG-Medium provides high performances in terms of frequency and consumption. It is also reprogrammable without any limits.

- Power supply:
  - Core: 1.2V±10%.
  - IOS: 1.5V±10% or 1.8V±10% or 2.5V±10% or 3.3V±10%.
- Performance:
  - 250MHz Logic.
  - 333MHz DSP.
  - 800Mbps I/O.
- Temperature :
  - -55°C to +125°C.

BASIC INFORMATION

Main features

- 65 nm ST-SPACE process technology.
- 4-Input Look-up tables.
- Lut expender to support up to 16 bits boolean functions.
- High performance carry chains.
- Advanced interconnect network to support random logic and coarse grain block functions.
- DSP Blocks for complex arithmetic operations.
- User memories with variable width and depth.
- Configuration modes: JTAG, Parallel 8 bits, Parallel 16 bits, Serial dump bus, Space Wire
- Integrated Space Wire interface available for user applications.
- Dedicated lowskew distribution network for clock, reset and load enable signals.
- On-chip thermal monitoring capability.

Input/Output features

- Multiple I/O powering support from 1.5V to 3.3V
- Cold sparing support.
- Programmable output drive to support multiple industry standards.
- Embedded logic to support DDR2 and DDR3.
- 800 Mbps I/O support.
- LVDS compatible mode.
- All pins support 2000V of ESD-HBM.
- Embedded logic to support Space Wire Data Strobe encoding.
- Programmable delay lines on all pins.
- Programmable resistive termination.

COMPONENT TYPES

Device Types as per ESCC Detail Specification 9202/086 and individual custom ESCC ASIC Sheets:

Part number	Part Type	Package	Temperature range
920208601A####	C65SPACE	CQFP-352	-55°C to +125°C

5.2.3.5 Technology Flow Definition

The Technology Flow Definition domain covers the design, fabrication, assembly and testing of packaged products using ST C65Space silicon technology node and ST assembly line technology capabilities in CQFP352 package family.

7. Design

The following features are based on ST ESCC evaluated libraries from C65SPACE Design Environment:
- DSPs,
- DPRAMs & SPREGs memories,
- Input / Output in I/O Banks (except for the pas itself, which keeps original pad structure but receives Custom Design Add On featuring)
- Bitstream manager,
- PLLs (1201),
- Waveform generators,
- SapceWire Interface (including LVDS pads).

Other features designed by NanoXplore are full in compliant with ST C65Space design rules.

The NG-MEDIUM FPGA is based on NanoXplore patented interconnect architecture offering the highest logic density as well as high efficiency mapping. Application mapping is supported by NanoXplore tools based on proprietary algorithms tailored to the interconnect topology.

The device is composed of a central fabric embedding the programmable logic, RAM and DSP blocks, and peripheral I/O buffers. The fabric is covered with a grid of high level functional blocks interleaved with interconnect structures providing routing resources to realize the connections within the fabric and to the peripheral I/O buffers. The programmable logic resources are arranged in a hierarchical structure called a TILE with a specific local interconnect network. The I/O buffers are arranged into multiple banks. Each bank has its own I/O buffer supply voltage.

8. Fabrication

The wafer manufacturing is performed in ST Crolles 300mm fab using the new C65SPACE technology silicon node developed in ST Crolles 300mm and successfully qualified by ST in September 2014.

The main characteristics of the silicon die are described below:

Mask Levels: 41.
Masks Levels of Metallization: 8 (7 Layers in Cu + 1 Layer Ta/TaN/AlCu).

Die size: 15.3*10.96 mm².
Die Pad Pitch: 70µm min.
Die Pad Opening: 44*108 µm².
Die Pads Numbers: 374 non-staggered.
Die Finish Front Side (passivation): PSG + Nitride.
Die Finish Back Side: Raw Silicon.
An additional step of OPM (Over Pad Metallization) deposition is performed at a third party subcontractor ChipBond (TW), under ST quality control.
OPM : TiW/Au (Au= 3.5µm±1µm)
OPM Pad size : 54*165 µm²

9. Assembly

Process

The assembly process of the C65 Space devices is set-up in the historical ST Space certified plant in Rennes, France using the main following process capabilities:

Die Attach Medium: “Cyanate Ester” JM7000
Wire Bonding technology: Ultrasonic Gold Ball-Bonding.
Wire: 0.8 mils (20µm) Gold 4N
Bonding Decks & Bonding wire number:

	CQFP352
Bonding decks N#	2
Bonding wires N#	448
Bond Wires on Deck #1	223
Bond Wires on Deck #2	225

Package

Ceramic Quad Flat Package with 352 leads (CQFP352) with Ceramic Tie Bar
Dimensions: 75*75*3.51 mm3.
Cavity Size: 17*12.66 mm²
Cavity Volume: 320 mm3.
Lid Material: Kovar with Plating Layers (Ni/Au)
Lid Size: 23.62*19.30 mm²
Lead finishing: Au Plated

10. Control and Test

The control & test of C65 Space devices are performed in both ST Grenoble plant, France for electrical testing and accelerated ageing (reliability screening) and Rennes, France for all other space related tests or at subcontracted third parties under Rennes Quality monitoring and control.

All these space related manufacturing operations are performed under the supervision and control of the ST ESCC Chief Inspector, located in our basic space plant, Rennes.

11. TCVs and SEC

TCV program has been carried out to address intrinsic failure mechanisms of the C65Space technology. NG-Medium encapsulated in CQFP352 are used as SECs to conduct all the requested evaluation and qualification tests.

12. Radiation Characteristics

The ST C65SPACE technology has been developed to fulfil the following characteristics:

- SEL immune up to LET > 60MeV.cm2/mg.
- TID tolerance = 300 krad(Si).

5.2.3.6 Manufacturing sites

DESIGN:
NanoXplore
1 avenue de la Cristallerie, 92310 Sèvres, France

WAFER FABRICATION:
ST Crolles 300 - 850 rue Jean Monnet 38926 Crolles, France

ASSEMBLY:
ST Rennes – 3 rue de Suisse 35200 Rennes, France. Basic Plant

CONTROL AND TEST:
ST Grenoble - 12 rue Jules Horowitz, B.P. 217 38019 Grenoble, France
ST Rennes – 3 rue de Suisse 35200 Rennes, France. Basic Plant

5.2.4 ST Microelectronics, France: ASIC platform FDSOI 28nm

5.2.4.1 Contact Information

Address	ESCC Chief Inspector
STMicroelectronics (Tours) SAS 3 rue de Suisse 35200 Rennes France	Ms Emmanuelle Guerinel Tel. +33 2 99 26 4800 emmanuelle.guerinel@st.com
	ASICs QA Project Manager
	M. Jean-Noël LETRILLARD Tel. +33 2 99 26 4800 ext : 4937 jean-noel.letrillard@st.com

5.2.4.2 Qualification

Current Qualification Certificate No.	In QML since:	Type Designation
394	Nov 2025	Integrated Circuits, Silicon, Monolithic, FDSOI 28nm ASIC Platform

Applicable documents:

ESCC Generic Specification No. 9000; ESCC Detail Specification No. 9304/012

STMicroelectronics Process Identification Documents:

- 8097046: GENERIC PID Ref. ST.01.2008

- DM00978658: PID for ASICs C28FDSOI Space FC

- DM00978698: PID for ASICs C28FDSOI Space FC Die Layout

5.2.4.3 List of Qualified Components

Component Number	Detail Specification	Generic part number	Circuit function	FPGA Matrix	Package
930401201P	9304/012	NX2H540TSC-FF1760	SoC field programmable gate array	NX2H540ATSC	FCTEBGA-1760

5.2.4.1 Technology Flow Abstract

GENERAL FEATURES

The NG-ULTRA NX2H540TSC is a Radiation Hardened By Design (RHBD) SoC FPGA in 28nm with quadcore ARM R52 running at 600MHz each, based on ST CMOS28FDSOI SPACE GEO Technology Platform from STMicroelectronics. It has a logic capacity of 537KLUT. The hardening techniques used in the NG-ULTRA, alongside the FD-SOI technology, provide radiation hardening performance.

NG-ULTRA NX2H540TSC contains two parts: A programmable logic matrix and Microprocessor subsystem.

First part is composed of a central fabric embedding the programmable logic, RAM and DP blocks. The fabric takes benefit from the highspeed connectivity such as High-Speed Serial Links (HSSLs) and DDR2/3 interfaces.
It is covered with a grid of high-level functional blocks interleaved with interconnect structures providing routing resources to realize the connections within the fabric and to the peripheral I/Os. The programmable logic resources are arranged in a hierarchical structure called a TILE with a specific local interconnect network. I/Os are arranged into multiple banks. Each bank has its own I/O bu;er supply voltage.

Second part is the microprocessor subsystem which is based on a complete System on Chip.

Power Supply	Description	Maximum ratings (V)
Supply Voltages	VDDCORE VDD_AUX VDD_SWITCH	1 ±5% 1.8 ±10% 1.8 ±10%
Input/Output Voltage Range Complex I/O Bank: Simple I/O Bank:	VDDIO	 1.2; 1.5; 1.8; 1.8; 2.5; 3.3; ±10%

Table1: maximum ratings of VDDIo

BASIC INFORMATION

Main features

- Technology Node: ST CMOS28FDSOI SPACE GEO technology
- Processing System: Quad core ARM Cortex R52 based System-on-Chip (SoC)
- Programmable Logic:
  537KLUT (4-input Look-Up Tables)
  High-performance carry chains
  Advanced interconnect network enabling both logic and coarse-grain block functions
- Arithmetic Capabilities: Dedicated DSP blocks for complex computations
- User-configurable memories with variable width and depth
- Configuration interfaces:
  Master Serial SPI (Single, Sequential, Triple Modular Redundancy - TMR)
  SpaceWire Protocol Support
- Debug interfaces:
  JTAG

16-bit Parallel
UART
– Dedicated lowskew distribution network for clock, reset and load signals
– On-chip thermal monitoring for system reliability

Input/Output features

– Multiple I/O voltage supported from 1.2V to 3.3V
– Integrated Cold Sparing Capability
– Programmable output drive strength to support various industry standards.
– High-Speed Interfaces:
Embedded logic to support SpaceWire interface (data strobe encoding)
Embedded logic to support DDR2, DDR3 for the fabric + DDR4 via the SoC memory
Up to 1.6 Gbps I/O speed for SSTL, HSTL and POD standards
– LVDS compatible mode
– All I/O pins support 2000V ESD-HBM protection
– Programmable delay lines on complex I/O pins
– Programmable resistive termination on complex I/O pins
– Optional register single rate for direct I/O pins and single or double rate for complex I/O pins

COMPONENT TYPES

Device Types as per ESCC Detail Specification 9304/012 and individual custom ESCC ASIC Sheets:

Part number	Part Type	Package	Temperature range
930401201P	NX2H540ATS C-FF1760 (NG-ULTRA)	Fine pitch Flip-Chip Organic Ball Grid Array with 1760 balls (FF1760)	-40°C to +125°C

5.2.4.2 Technology Flow Definition

1. Design

NG-ULTRA is a SoC-FPGA divided into 2 parts:
• PS: It is composed of 4 ARM cores with multiple peripherals. The PS is responsible for booting, executing the ASW and transferring the bitstream to the PL part.
• PL: It is composed of a central fabric with analog elements on the ring. The PL is managed by a bitstream manager responsible for programming this matrix.

The NG-ULTRA PS features a quad-core ARM Cortex-R52, optimized for real-time and safety-critical systems. This architecture supports hardware-enforced isolation and fault tolerant execution, enabling secure partitioning of tasks and robust system behaviour under adverse conditions.

The following IPs are based on ST ESCC evaluated libraries from ST CMOS28FDSOI SPACE GEO Design Environment:

- Clock subsystem

- Reset subsystem
- Watchdog
- Bootrom
- Flash Controller
- AXI Controller
- Error Management
- QoS Monitor
- SoC Monitoring
- DMA
- eRAM
- RS DDR Controller
- Space Wire Boot AHB
- Network Interconnect
- UART
- DSP
- Register file
- Bitstream Manager
- iobank_complex
- iobank_direct
- iobank_hssl
- iobank_clockgen
- iobank_soc_ddr.

ST CMOS28FDSOI SPACE GEO Standard libraries :

analogmixed
C28SOI_AN_VTSENS_SPACE
C28SOI_PLL_PF_5000MHZ_SPACE
fuse
C28SOI_FU_SAFMEMHV_SPACE
digital standard cells
C28SOI_SC_12/8_CORE/CLK_LL/LR
C28SOI_SC_8_CORESPACE_LL
memory
C28SOI_MEM_ROM_SPACE
C28SOI_MEM_SRAM_DPHD_SPACE
C28SOI_MEM_SRAM_DPREG_SPACE
C28SOI_MEM_SRAM_SPHD_SPACE
C28SOI_MEM_SRAM_SPREG_SPACE
io
C28SOI_IO_SPACE

2. Fabrication

The wafer manufacturing is performed in ST Crolles 300mm fab using the ST CMOS28FDSOI SPACE GEO technology silicon node developed in ST Crolles 300mm and successfully qualified by ST in May 2019.

The main characteristics of the silicon die are described below:

Mask Levels: 42.
Masks Levels of Metallization: 11 (10 Layers in Cu + 1 Layer Ta/TaN/AlCu).
Die size: 21.888*20.348 mm2.
Die Pad Pitch: 180µm min.

Die Pad Opening: 87 µm.
Die Pads Numbers: 11236 non-staggered.
Die Finish Front Side (passivation): PSG + Nitride + PIX
Die Finish Back Side: Raw Silicon.

3. Assembly

Process

The assembly process of the ST CMOS28FDSOI SPACE GEO devices is set-up in the historical ST Space certified plant in Rennes, France using the main following process capabilities:

Substrate : FCTEBGA 45sq, 1760 land pads, SOP µBalls on FC Pads + OSP on bottom side
Flip chip soldering (lead free solder bump): flux dipping
SMD : Capacitor 0.1µF, 0603, 25v +/-10%, Pure Tin finishing, JAXA qualified
Underfill : epoxy liquid
Thermal Interface Material : thermal grease
Lid material : Copper Alloy, nickel finishing
Lid size : 44mm * 44mm
Lid attach : glue
Ball material : SnPb 63/37
Ball size : 0.64mm

4. Control and Test

The control & test of ST CMOS28FDSOI SPACE GEO devices are performed in both ST Grenoble plant, for electrical testing and accelerated ageing (reliability screening) and Rennes, for all other space related tests or at subcontracted third parties under Rennes Quality monitoring and control.
All these space related manufacturing operations are performed under the supervision and control of the ST ESCC Chief Inspector, located in ST basic space plant, Rennes.

5. TCVs and SEC

NG-ULTRA packaged in organic non hermetic FCTEBGA 45*45 is used as SEC to conduct all the requested evaluation and qualification tests.

6. Radiation Characteristics

Radiation Tolerance:
- Radiation-hardened design applied to configuration memories and registers for enhanced resilience
- Single Event Upset (SEU) immunity validated up to LET > 60 MeV.cm2/mg for configuration memory, DPRAM user memory and programmable logic registers.
- Total Ionizing Dose (TID) tolerance up to 50Krads (Si), ensuring long-term reliability in harsh environments
- Embedded Error Detection and Correction (EDAC) mechanisms safeguard user memory integrity

- Critical logic blocks are triplicated to enhance fault tolerance and reliability

5.2.4.3 Manufacturing sites

DESIGN:

NG-ULTRA
NanoXplore
1 avenue de la Cristallerie, 92310 Sèvres, France

WAFER FABRICATION:
ST Crolles 300 - 850 rue Jean Monnet 38926 Crolles, France

WAFER LOT BUMPING

AMKOR Korea - 150, Songdomirae-ro, Yeonsu-gu, Incheon 21991, Korea

WAFERLOT ELECTRICAL TESTING

ST GRENOBLE - 12 RUE JULES HOROWITZ, B.P. 217 38019 GRENOBLE, FRANCE

ASSEMBLY:
ST Rennes – 3 rue de Suisse 35200 Rennes, France. Basic Plant

CONTROL AND TEST:

ST GRENOBLE - 12 RUE JULES HOROWITZ, B.P. 217 38019 GRENOBLE, FRANCE
ST RENNES – 3 RUE DE SUISSE 35200 RENNES, FRANCE. BASIC PLANT

5.2.5 United Monolithic Semiconductors, France : GaN HEMT

5.2.5.1 Contact Information

Address	ESCC Chief Inspector
United Monolithic Semiconductors Batiment Charmille Mosaic parc Courtaboeuf 10 avenue du Quebec 91140 Villebon sur Yvette	Mr B. LAMBERT +33 6 45 74 51 75 +33 1 69 86 32 88 Benoit.Lambert@ums-rf.com

5.2.5.2 Qualification

Current Qualification Certificate No.	In QML since:	Type Designation
388	Mar 2024	Transistors, Microwave, GaN HEMT Unmatched in Metal Ceramic Package CHKxxxx-SYx Product Family

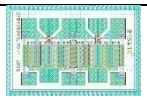
5.2.5.3 List of Qualified Components

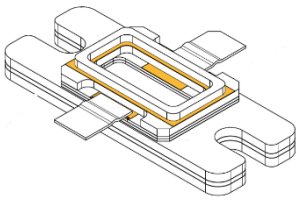
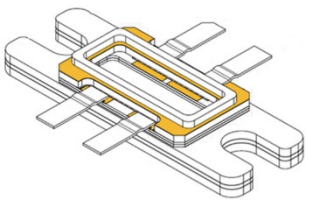
Variant number	Detail Specification	Generic part number	Component type	Package
01	5614/009	CHK8101-SYC	15W @ 1.7GHz	Ceramic-Metal, Flanged,Type C
02	5614/009	CHK8201-SYA	50W @ 1.7GHz	Ceramic-Metal, Flanged,Type A
03	5614/009	CHKA012bSYA	130W @ 1.7GHz	Ceramic-Metal, Flanged,Type A

5.2.5.4 Technology Flow Abstract

CHKxxxx-SYx Product Family is based on the UMS GH50-20 GaN power bar technology. Power bars are assembled using AuSn eutectic soldering in a highly dissipated ceramic-metal Flanged packaged. To assure RF stability of each component type, an RF absorber is used in the package cavity. All manufacturing and test production is performed in accordance to the ESCC/5010.

	CAPABILITY APPROVAL DOMAIN
	RIC1 (Product: CHK8101-SYC) RIC3 (Product: CHKA012bSYA)

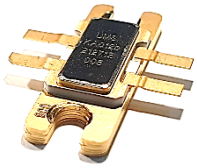
GaN DIE PROCESS		
Die overview		
Manufacturer	UMS – Ulm – Germany	
Power bar dies technology	UMS 4GH50-20	
Gate pitches	70µm	
Unitary gate finger width	250µm & 400µm	
Finger gates per block	8	
Number of blocks	2 , 4, 8	
Max operating Freq. (GHz)	6 GHz	

PACKAGE TECHNOLOGY		
Package overview (without Lid)		
Package manufacturer	Kyocera – Gamo – Japan	
UMS Package reference	SYC	SYA
UMS SAP Material N°	47003170	47002520
Sealing	Seam-welding process	

Lead	2	4
Base plate length (mm)	17.5	20
Base plate width (mm)	6.7	
Lid for Package: Manufacturer	Hi-REL Group	
UMS Drawing Document N°	61504640	61503116 last version
RF Absorber : Manufacturer	DEMGY	
UMS Material N°	47003186	47003186

ASSEMBLY TECHNOLOGY	
Assembly subcontractor	RHe Microsystems GmbH – Radeberg – Germany
Preform characteristics	Material: Eutectic Au80Sn20 (Liquidis:278°C),
Sealing process	Hermetical seam sealed
Assembly screening (100%)	Stabilization bake - 24h @ 150°C / MIL-STD-750 method 1032 Temp. Cycling - 20 cycles -55/+150°C / MIL-STD-750 method 1051 PIND test - MIL-STD-750 method 2052 X-ray - Wire bonding inspection / MIL-STD-883 2009.12 Leak test - MIL-STD-883-1014.15 Cond A2

ELECTRICAL SCREENING FLOW	
Manufacturer	UMS – Villebon – France
Burn In 1 Electrical Stabilization (100%)	10hrs - Tamb=+125°C; VD=+50V; VG=-7V 10hrs - Tj=200°C; VD=+50V; VG=cst (RIC1:ID=256mA / RIC3:ID=1.25A)
Burn-In 2 (100%)	240hrs - Tj=200°C; VD=+50V; VG=cst (RIC1:ID=256mA / RIC3:ID=1.25A) RF characterization / Acceptance criteria based on specification and on parameter drift (before/after burn-in) / Pulsed or CW

FINAL PRODUCT		
Product overview		
Typical RF-power @1.3GHz (Vds=50V, Idq=25mA/mm)	>15W	>100W
Product reference	**CHK8101-SYC**	**CHKA012bSYA**

Radiation characteristics

Displacement Damage (DD) tests show no influence of proton irradiation on the electrical performance up to a tested fluence of 10^{12} p/cm2.

Total Ionizing Dose (TID) tests show no influence of Co60 irradiation up to a final tested dose of 274 krad (in GaN).

Single Event Burn-out (SEB) levels for gate and drain RF voltage excursions for transistors operating in class AB, such as described in next table.

Characteristics	Symbols	Safe Operating Area	Units	Remarks
Drain-Source Voltage RF-Excursion	V_{DS_peak}	≤ 125	V	Xe ions (LET-Si = 62.5keV/µm) Fluence = 1.E+07 ions/cm2
Gate-Source Voltage RF-Excursion	V_{GS_peak}	≥ -6	V	
Drain-Source Voltage RF-Excursion	V_{DS_peak}	≤ 125	V	Rh ions (LET-Si = 46.1keV/µm) Fluence = 1.E+07 ions/cm2
Gate-Source Voltage RF-Excursion	V_{GS_peak}	≥ -9	V	

In vacuum environment characteristics

Corona/Multipaction free operation test campaign was performed. No failure occurred up-to the maximum levels that it was possible to evaluate and which are provided in table here after.

Characteristics	Symbols	Safe Operating Area	Units	Remarks
Drain-Source Voltage RF-Excursion	V_{DS_peak}	≤ 133	V	Multipaction Phenomena See Note 1
Drain-Source Voltage RF-Excursion	V_{DS_peak}	≤ 138	V	Corona Phenomena See Note 2

NOTES:

1) Multipaction test conditions: Pressure < 1.5 10^{-5} mbar, frequency = 1.25GHz, Test board temperature from -30°C to 70°C
2) Corona test conditions: Pressure from 900mbar to <1.5 10^{-5} mbar, frequency = 1.25GHz, Test board temperature from -30°C to 70°C

5.2.5.5 Manufacturing sites

WAFER FABRICATION:
UMS Gmbh Wilhelm Runge Strasse 11 D-089081 Ulm Germany

DIE ASSEMBLY:
RHe Microsystems Gmbh Heidestrass 70 01454 Radeberg Germany

CONTROL AND TEST:
UMS SAS 10 avenue du Quebec 91140 Villebon sur Yvette France

5.3 RESISTORS (10)

5.3.1 VISHAY S.A. Fance: Chip resistors

5.3.1.1 Contact Information

Address	ESCC Chief Inspector
Vishay S.A. Division SFERNICE 199, Boulevard de la Madeleine CS71159 F-06003 Nice Cedex 01 France	Mathilde FONTAINE EMAIL: mathilde.fontaine@vishay.com

5.3.1.2 Qualification

Current Qualification Certificate No.	In QML since:	Type Designation
287J	Feb. 2009	Thin Film Technology for Chip, Wraparound, Single and Network Resistors, Fixed, Based on Types P for Single Chip, PRA and CNW for Resistor Networks

APPLICABLE DOCUMENTS

ESCC Generic Specification No. 4001

ESCC Detail Specification Nos. 4001/023, 4001/025

Vishay S.A. Process Identification Document PID PID-TFD P PRA CNW Is. 15

5.3.1.3 List of Qualified Components

NOTE: the Established Reliability Level R is evaluated according to ESCC specification 26000.

Type PHR, Variants 01 to 08, 13 and 14 are qualified

Type PFRR, Variants 09 to 12 and 15 are qualified

Type PRAHR/CNWHR, Variants 01 to 42 are qualified

Detail Specification		
4001/023	PHR	High Stability and Precision Chip
4001/023	PFRR	High Stability and Precision Chip with Established Reliability Level R
4001/025	PRA/CNWHR	High Stability and Precision Surface Mount Array

Lead material is E with either Type 2 or Type 4 finish. The terminal material and finish of some of these variants makes them unsuitable for solder assembly methods. They shall be assembled using glue or wire bond techniques. See Detail specifications.

Operating Temperature Range, (°C): -55 to +155

TYPE PHR:

Detail Specification	Style	Critical R (kΩ)	Rated Dissipation (W)	Limiting Element Voltage (V)	Type Variant
4001/023	0402	18	0.050	30	13; 14
	0603	12.25	0.100	35	01; 05
	0805	45	0.125	75	02; 06
	1206	40	0.250	100	03; 07
	2010	45	0.500	150	04; 08

Variant	Style	Resistance Range (Note 1)		Tolerance (±%) (Note 2)	Temperature Coefficient (10^{-6}/°C) (Note 2)	Weight (g)
		Min (Ω)	Max (MΩ)			
01, 05	0603	10	0.200 (0.160 for TC"C")	0.01; 0.02; 0.05; 0.1	±5; ±10; ±25	0.003
02, 06	0805	10	0.250	0.01; 0.02; 0.05; 0.1	±5; ±10; ±25	0.004
03, 07	1206	10	1.000	0.01; 0.02; 0.05; 0.1	±5; ±10; ±25	0.01
04,08	2010	10	3.000	0.01; 0.02; 0.05; 0.1	±5; ±10; ±25	0.03
13, 14	0402	10	0.100 (0.067 for TC"C")	0.01; 0.02; 0.05; 0.1	±5; ±10; ±25	0.002

NOTE 1:

Variant	Style	Critical Resistance (KΩ)
01 - 05	0603	12.25
02 - 06	0805	45
03 - 07	1206	40
04 - 08	2010	45
13 - 14	0402	18

NOTE 2:

Resistance (Ω)	Available Tolerances (±%)	Series
10 ≤ R < 50	0.1	Any value in the resistance range
50 ≤ R < 100	0.05 and 0.1	
100 ≤ R < 250	0.02; 0.05 and 0.1	
R ≥ 250	0.01; 0.02; 0.05 and 0.1	

Resistance (Ω)	Temperature Coefficient (ppm/ºC)	Series
10 ≤ R < 20	E: 25 (-55ºC; +155 ºC)	Any value in the resistance range
20 ≤ R < 50	Y: 10 (-55ºC; +155 ºC)	
20 ≤ R < 50	Z: 5 (+22ºC; +70 ºC)	
R ≥ 50	C: 5 (-55ºC; +155 ºC)	

TYPE PFRR:

Detail Specification	Style	Critical R (kΩ)	Rated Dissipation (W)	Limiting Element Voltage (V)	Type Variant
4001/023	0402	32	0.050	40	15
	0603	25	0.100	50	09
	0805	80	0.125	100	10
	1206	90	0.250	150	11
	2010	80	0.500	200	12

Style	Resistance Range (Ω)	Tolerance (±%)	Temperature Coefficient TC($\pm 10^{-6}$ /°C)
0402; 0603; 0805; 1206; 2010	From 100 to ≤ 100K	0.05; 0.1	10; 25
0603; 0805; 1206; 2010	From 100 to ≤ 261K	0.05; 0.1	10; 25
0805; 1206; 2010	From 261K to ≤ 301K	0.05; 0.1	10; 25
1206; 2010	From 301K to ≤ 1M	0.05; 0.1	10; 25
2010	From 1M to 3M01	0.05; 0.1	10; 25

TYPE PRAHR/CNWHR:

Detail Specification	Style	Critical R (K Ω)	Rated Dissipation (W/resistor)	Limiting Element Voltage (V/resistor)	Type Variant	
					Same Ohmic Values	Different Ohmic Values
4001/025	PRA100	12.25	0.100	35	01 to 07	22 to 28
	PRA135	56.25	0.100	75	08 to 14	29 to 35
	PRA182	100	0.100	100	15 to 21	36 to 42

Style	Resistance Range (Ω)	Tolerance (±%)		Temperature Coefficient TC(±10-6 /°C)	
		Absolute	Relative	Absolute	Relative
PRA100; PRA135; PRA182	From 100 to 200K	0.1; 0.5; 1	0.05; 0.1	10	3; 5
PRA135; PRA182	From 200K to 250K	0.1; 0.5; 1	0.05; 0.1	10	3; 5
PRA182	From 250K to 1M	0.1; 0.5; 1	0.05; 0.1	10	3; 5

Number of Resistors per Array: 2 to 8

NOTES:

1. Note that gold finish variants are not intended for de-golding and tinning.
2. The electrical ranges of these ESCC QML Qualified components variants are listed in the ESCC Detail Specifications and in the Qualified Part List (REP005) document available on the ESCIES website, https:// escies.org.

5.3.1.4 Technology Flow Abstract

GENERAL FEATURES

The thin film technology for chip, fixed, wraparound, single and network resistors are designed on types based on P for single chip, PRA for 2 to 8 resistors of similar value and CNW for 2 to 8 resistors with at least two different values with the same form factor as PRA.

Technology Flow	Scope	Site
Design Centre	Single resistor chips in 0402 0603, 0805, 1206 and 2010 formats 2 to 8 resistors of similar value in formats 0603, 0805 and 1206 2 to 8 resistors with at least 2 different values with the same form factor, 0603, 0805 or 1206	Vishay S.A. Division SFERNICE 199, Boulevard de la Madeleine CS71159 F-06003 Nice Cedex 01 France
Fabrication	Film deposition Photolithography Thermal treatment Passivation Thermal stabilization and control	As above
Assembly	Laser trim Protective layer Termination and Test	As above
Test	Chart F2, F3 and F4 Periodic Testing	As above

BASIC INFORMATION

The technology consists of:

–Substrate: High purity alumina (99.5%)

–Resistive Layer: Nickel chromium
–Passivation Layer: Silicon Nitride
–Protection: Epoxy and Silicone
–Termination: Nickel barrier
–Processes: Thin film deposition
–Finish: SnPbAg or Au

Critical resistance by style:

– P 0402 FR:32 k
– P 0603 FR:25 k
– P 0603 HR:12.25 k
– P 0805 FR: 80k
– P 0805 HR: 45 k
– P 1206 FR: 90 k
– P 1206 HR: 40 k
– P 2010 FR: 80k
– P 2010 HR: 45 k
– PRA 100: 12.25 k
– PRA 135: 56.25 k
– PRA 182: 100 k

COMPONENT TYPES

The available formats are defined in the variants table in the Detail Specifications. Variants with established reliability in accordance with Basic specification No. 26000 are designated with an ''FR" suffix here for convenience. Variants 09, 10, 11 and 12 have established reliability level 'R' at 60% confidence level.

5.3.1.5 Technology Flow definition

1. Design

The design manuals covers the design rules and limits:

– HP-BE/001 (Maîtrise de la conception)
– HP-BE/004 (Données technologiques, Régles d'implementation, Performances)

Critical design characteristics:

– Minimum metal width: 10 µm
– Power dissipation lower than 250mW/mm2
– Current density lower than 7000 A/mm2
– Electrical field lower than 5V/ µm

2. Fabrication/Assembly

The manufacturing flows and procedures are described in section 4 of Vishay S.A.PID.

3. Test

Complete test sequence as detailed in ESCC Generic 4001 and the relevant Detail Specifications is conducted by Vishay S.A.

The deletion of the Third Harmonic Control requirement from ESCC Detail Specification No. 4001/023 for thin film wraparound technology is documented in reference report MAT/ 3HC/07.02 revision 3 dated 2007-06-20.

For variants with established reliability the efficiency of the Overload Test is increased with the implementation of a resistance change rejection criteria of 500 ppm and approved by TRB decisions on 2007-04-04.

4. Radiation Characteristics

The resistors covered in this technology domain is considered insensitive to radiation effects.

5.4 TRANSFORMERS (08)

5.4.1 Exxelia SAS: Custom magnetics: linear and toroidal technology

5.4.1.1 Contact Information

Address	ESCC Chief Inspector
Exxelia SAS 16, Parc d'Activités du Beau Vallon F-57970 Illange France	Mr. J. Pierre Tel: +33 3 82 59 13 33 EMAIL: info@exxelia.com

5.4.1.2 Qualification

Current Qualification Certificate No.	In QML since:	Type Designation
356C	February 2019	Molded SMD custom magnetic components, linear (CCM) winding technology

APPLICABLE DOCUMENTS

ESCC Generic Specification No.3201

ESCC Detail Specification Nos. 3201/011 (CCM technology)

Exxelia. Process Identification Document PID 101 issue 6 (CCM technology)

5.4.1.3 List of Qualified Components

The component type variants and range of magnetics components applicable to the linear CCM technology are as follows:

Variant Number	Type	Design Domain	Electrical Characteristics	Total Power Max (W)	No. of Terminals (3)	Terminal Finish (4)	Weight Max (g)
01	CCM4	Note 1	Note 2	≤ 18	12	Sn60Pb40	5.1
02	CCM5	Note 1	Note 2	≤ 40	16	Sn60Pb40	7.4
03	CCM6	Note 1	Note 2	≤ 50	16	Sn60Pb40	12.1
04	CCM20	Note 1	Note 2	≤ 120	16	Sn60Pb40	21.4
05	CCM25	Note 1	Note 2	≤ 150	20	Sn60Pb40	44.2

NOTE 1

The design domain for components produced in accordance with these specifications includes the following items:

- Development of customized electrical functions:

  - -Single or multi-coupled inductors
  - -Common mode chokes
  - -Power transformers (flyback, forward, push-pull, half/full bridge, specific architectures)
  - -Signal transformers
  - -Pulse transformers
  - -Current/voltage measurement transformers
  - -Specific magnetic functions within environment and thermal requirements

•Temperature range: -55°C +125°C

•Power, losses, and component heating:

  - Maximum power depends on component heating. The heating is calculated from losses and thermal resistances for each Variant according to the electrical function. The thermal resistances are given in Maximum Rating.
  - The maximum temperature rise at Tamb = +100°C is +25°C.
  - Examples of maximum power per Variant are given above.

•Dielectric strength:

  - Single insulation: 500Vrms
  - Reinforced insulation for CCM technology: 1000Vrms

NOTE 2
All electrical characteristics applicable to a particular component design are specified in the document: Specific Component Design Sheet provided by the manufacturer.

5.4.1.4 Technology Flow abstract

GENERAL FEATURES
The Technology Flow covers the design, manufacturing, assembly, in-process inspection, screening and testing of custom magnetic components at Exxelia, Illange, France.

These SMD inductors, chokes and transformers use linear winding (CCM technology) assembled on a lead frame and molded with epoxy resin.

BASIC INFORMATION
Leads: Brass with copper layer and SnPb finish

Molding: Epoxy resin

Wire: 180 °C magnet wire

Magnetic core: Chosen during design phase to meet customer requirements

Formats component types: See Details specifications 3201/011

5.4.1.5 Technology Flow definition

1. Design

The magnetic components are designed according to design rules and following a design process both described in the Exxelia document PID 101.

The design rules ensure maximum operating temperature below 125°C and dielectric strength

2. Manufacturing process

The manufacturing process is described in the document PID 101 (CCM technology). Process summary:

- Linear winding for CCM technology
- High temperature soldering on the lead frame
- Transfer molding
- Magnetic core assembly for CCM technology
- Leads forming

3. Control and testing

The control and test are performed in Exxelia Illange. They are performed according to the document Specific Component Design Sheet and the generic ESCC specification 3201 and the ESCC detail specification 3201/011

4. Radiation characteristics

CCM magnetics components are not sensitive to radiations.

5.4.1.6 Manufacturing site

Exxelia 16 Parc d'Activités du Beau Vallon F57970 Illange France

5.4.2 Flux A/S: Custom Magnetics (Inductors, Chokes and Transformers)

5.4.2.1 Contact Information

Address	ESCC Chief Inspector
Flux A/S Industrivangen 5 4550 Asnaes Denmark	Mr. C. A. D. Winther Tel: +45 5935 7713 EMAIL: caw@flux.dk

5.4.2.2 Qualification

Current Qualification Certificate No.	In QML since:	Type Designation
364B	March 2020	Custom Magnetics (Inductors, Chokes and Transformers)

APPLICABLE DOCUMENTS
ESCC Generic Specification No.3201

ESCC Detail Specification No. 3201/013

Process Identification Document PID 088699015-9, ESCC DML 08699003, ESCC DPL 08699004

A public extract of the qualified domain and PID is available in Flux document 08699018.

5.4.2.3 List of Qualified Components

The part number is 3201/01301F[12345678-#] and has been generated in accordance with ESCC 3201/013. Flux A/S component identification is as follows: 12345678-#-C

The component types and range of magnetic components applicable to the inductors and chokes technology are defined herein:

Variant Number	Design Domain	Electrical Characteristics	Number of Terminals	Finish	Weight
Based on core size and type of termination 12345xxx	Note 1	Note 2	Note 3	Note 4	Note 5

The component types and range of magnetic components applicable to the transformers technology are defined herein:

Variant Number	Design Domain	Electrical Characteristics	Number of Terminals	Finish	Weight
Based on core size and type of termination 14345xxx	Note 1	Note 2	Note 3	Note 4	Note 5

The component types and range of magnetic components applicable to the data transmission (Chokes, Inductors, Transformers) technology are defined herein:

Variant Number	Design Domain	Electrical Characteristics	Number of Terminals	Finish	Weight
Based on core size and type of termination 15345xxx	Note 1	Note 2	Note 3	Note 4	Note 5

NOTE 1 - DOMAIN
The design domain for the components manufactured includes the following:

- Development of customized electrical functions:
  - Single or multi-coupled inductors

- Common mode chokes /Differential
- Power transformers (flyback, forward, push-pull, half/full bridge, specific architectures)
- Signal transformers
- Pulse transformers
- Current/voltage measurement transformers
- Specific magnetic functions within environment and thermal requirements
- Integrated Magnetics
- Spike Killer (high frequency filter)
- High Frequency
- High Voltage

- Temperature Range -55ºC to +130ºC, depending on temperature class
- Maximum Power - See Note 2
- Temperature rise – See Note 2
- Dielectric Strength – See Note 2

The multi-element assemblies featuring multiple transformers/inductors assembled on substrate, that Flux are capable of manufacturing, are not included into ESCC QML domain.

NOTE 2 - ELECTRICAL CHARACTERISTICS

All electrical characteristics to a particular design are specified in the magnetics sheet, which is either produced or verified by the manufacturer.

The maximum ratings shall not be exceeded at any time during use or storage. Maximum ratings shall only be exceeded during testing to the extent specified in this specification and when stipulated in Test Methods and Procedures of the ESCC Generic Specification.

Characteristics	Symbols	Maximum Ratings (Note 1)	Units	Remarks
Power	P	See Magnetic Sheet	W	Upto 5 kW
Rated DC Current	I_R	See Magnetic Sheet	mA	Upto 62.5A
Dielectric Withstanding Voltage	DWV	See Magnetic Sheet	Vrms	
Operating Frequency	f	See Magnetic Sheet	Hz	Upto 10 Mhz
Operating Temperature Range	T_{op}	See Magnetic Sheet (-55 to +130ºC)	°C	T_{amb}
Storage Temperature Range	T_{stg}	See Magnetic Sheet (-55 to +155ºC)	°C	
Soldering Temperature	T_{sol}	+260 for SnPb +300 for SnAg	°C	Note 2

NOTES:

1. This Maximum Rating for a particular component will be specified in the Magnetic Sheet for that component
2. The maximum operating temperature shall not exceed the derated material temperature– (Temperature rise+Hotspot)
3. The maximum storage temperature shall not exceed the derated material temperature

4. Unless otherwise specified in the applicable Magnetic Duration 5 seconds maximum, the same terminal shall not be resoldered until 3 minutes have elapsed.

NOTE 3 – NUMBER OF TERMINALS

The number of terminals or leads are specified in the magnetics sheet, which is either produced or verified by the manufacturer.

NOTE 4 – MATERIAL AND FINISHES

The minimum wire size shall be Ø0.10mm

The materials and finishes including case and terminals for a particular component will be specified in the Magnetic Sheet for that component. All materials shall meet the requirements of ECSS-Q-ST-70-71 and are detailed in FT08699004.

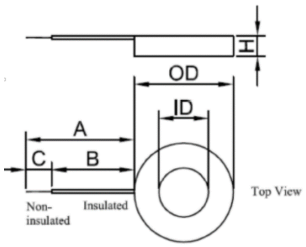
NOTE 5 – WEIGHT AND PHYSICAL DIMENSIONS

The weight and physical dimension are specified in the magnetics sheet.

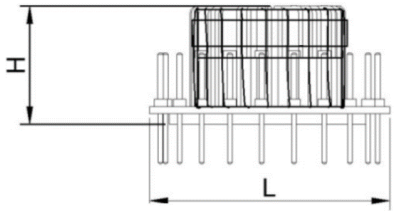
The overall dimensions for the range of cores used in components, depending on the design type used, are as follows:

- For toroid based designs: effective core (The minimum physical area which the total flux runs through the core) area of 2mm2 to 199mm2; see examples below:

Toroid with flying leads

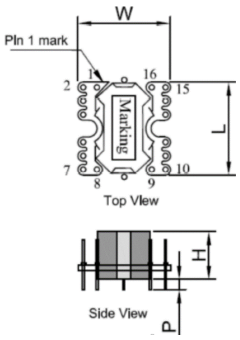


Toroid on base with pins

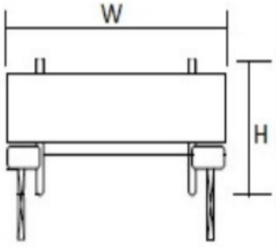


- For coil former based designs: effective core area 2.66mm2 to 146mm2; see examples below:

RM (Rectangular Module) based design with pins

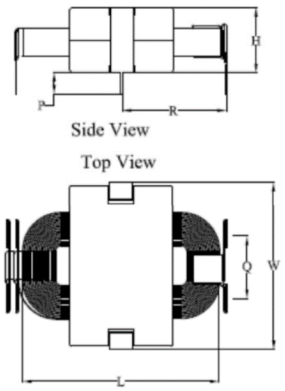


EFD (Economic Flat Design) based design with pins

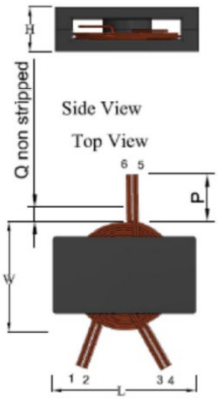


– For custom designs: effective core area 0.14mm2 to 484mm2; see examples below:

Planar design with foil



Planar design with wire



Unless otherwise specified in the applicable Magnetic Sheet and where applicable, terminals shall be colour coded.

5.4.2.4 Technology Flow abstract

GENERAL FEATURES

The Technology Flow covers the design, manufacturing, assembly, in-process inspection, screening and testing of custom magnetic components at Flux A/S, Denmark.

BASIC INFORMATION

Leads: As per ECSS-Q-ST-70-08

Molding: As specified and listed in DML

Wire: As specified and listed in DML

Magnetic core: Chosen during design phase to meet customer requirements and listed in DML.

Formats component types: See Detail specification 3201/013 and magnetic sheets.

5.4.2.5 Technology Flow definition

1. Design

The magnetic components are designed according to design rules and following a design process described in the PID FT088699015. The design rules ensures operation within specified temperature class, see magnetic sheet.

During the electrical design the specified voltage, current, frequency, and power is ensured the design is within the domain.

With the electrical design in place the core and mechanical design is checked against the physical domain constraints.

Finally the materials and production processes are compared to the ESCC DML and DPL to ensure the complete design is within the domain.

Electrical rule set:

Parameter	Inductor	Transformer
Output Power [W]	0≤P≤2,5kW	0≤P≤ 5 kW
Voltage [V]	0≤V≤110V	0≤V≤3kV
Current [A]	0≤I≤35A	0≤I≤62.5 A
Dielectrical Breakdown	950≤V≤8kV	950≤V≤8kV
Temperature [ºC]	-55≤T≤155	-55≤T≤155
Dimensions[mm^3] (Core Volume)	1≤V≤164000	2≤V≤234000

NOTE: Voltage and current values are absolute values.

2. Manufacturing process

The manufacturing process is described in the PID FT088699015 and DPL FT08699004. Materials and Processes are selected from Flux's ESCC DML and DPL respectively.

3. Control and testing

Control and testing are performed at Flux A/S.

They are performed according to the part specific magnetic sheet and the generic ESCC specification 3201 and the ESCC detail specification 3201/013

4. Radiation characteristics

These magnetic components are not sensitive to radiation.

5.4.2.6 Manufacturing site

Flux A/S, Industrivangen 5, 4550 Asnaes, Denmark