



**INTEGRATED CIRCUITS, SILICON MONOLITHIC,
CURRENT MODE PULSE WIDTH MODULATOR
CONTROLLER,
BASED ON TYPE UC1843
ESCC Detail Specification No. 9108/018**

**ISSUE 1
October 2002**



	ESCC Detail Specification		PAGE ii ISSUE 1
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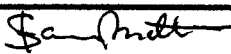
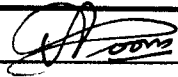
Pages 1 to 33

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ESA/SCC Detail Specification No. 9108/018



**space components
coordination group**

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SCC

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PAGE 2

ISSUE 1

DOCUMENTATION CHANGE NOTICE

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**TABLE OF CONTENTS**

	<u>Page</u>
1. GENERAL	5
1.1 Scope	5
1.2 Component Type Variants	5
1.3 Maximum Ratings	5
1.4 Parameter Derating Information	5
1.5 Physical Dimensions	5
1.6 Pin Assignment	5
1.7 Truth Table	5
1.8 Circuit Schematic	5
1.9 Functional Diagram	5
1.10 Handling Precautions	5
2. APPLICABLE DOCUMENTS	12
3. TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS	12
4. REQUIREMENTS	12
4.1 General	12
4.2 Deviations from Generic Specification	12
4.2.1 Deviations from Special In-process Controls	12
4.2.2 Deviations from Final Production Tests	12
4.2.3 Deviations from Burn-in and Electrical Measurements	12
4.2.4 Deviations from Qualification Tests	12
4.2.5 Deviations from Lot Acceptance Tests	12
4.3 Mechanical Requirements	12
4.3.1 Dimension Check	12
4.3.2 Weight	13
4.4 Materials and Finishes	13
4.4.1 Case	13
4.4.2 Lead Material and Finish	13
4.5 Marking	13
4.5.1 General	13
4.5.2 Lead Identification	13
4.5.3 The SCC Component Number	13
4.5.4 Traceability Information	13
4.6 Electrical Measurements	14
4.6.1 Electrical Measurements at Room Temperature	14
4.6.2 Electrical Measurements at High and Low Temperatures	14
4.6.3 Circuits for Electrical Measurements	14
4.7 Burn-in Tests	14
4.7.1 Parameter Drift Values	14
4.7.2 Conditions for High Temperature Reverse Bias Burn-in	14
4.7.3 Conditions for Power Burn-in	14
4.7.4 Electrical Circuits for High Temperature Reverse Bias Burn-in	14
4.7.5 Electrical Circuits for Power Burn-in	14
4.8 Environmental and Endurance Tests	31
4.8.1 Electrical Measurements on Completion of Environmental Tests	31
4.8.2 Electrical Measurements at Intermediate Points during Endurance Tests	31
4.8.3 Electrical Measurements on Completion of Endurance Tests	31
4.8.4 Conditions for Operating Life Tests	31
4.8.5 Electrical Circuits for Operating Life Tests	31
4.8.6 Conditions for High Temperature Storage Test	31



TABLES

	<u>Page</u>
1(a) Type Variants	6
1(b) Maximum Ratings	6
2 Electrical Measurements at Room Temperature - d.c. Parameters	15
Electrical Measurements at Room Temperature - a.c. Parameters	16
3 Electrical Measurements at High and Low Temperatures - d.c. Parameters	17
Electrical Measurements at High and Low Temperatures - a.c. Parameters	18
4 Parameter Drift Values	29
5(a) Conditions for High Temperature Reverse Bias Burn-in	30
5(b) Conditions for Power Burn-in and Operating Life Tests	30
6 Electrical Measurements on Completion of Environmental Tests and at Intermediate Points and on Completion of Endurance Testing	32

FIGURES

1 Parameter Derating Information	7
2 Physical Dimensions	8
3(a) Pin Assignment	10
3(b) Truth Table	10
3(c) Circuit Schematic	11
3(d) Functional Diagram	11
4 Circuits for Electrical Measurements	19
5(a) Electrical Circuit for High Temperature Reverse Bias Burn-in	30
5(b) Electrical Circuit for Power Burn-in and Operating Life Tests	30

APPENDICES (Applicable to specific Manufacturers only)

'A' AGREED DEVIATIONS FOR UNITRODE (USA)	33
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**1. GENERAL****1.1 SCOPE**

This specification details the ratings, physical and electrical characteristics, test and inspection data for a silicon monolithic, Current Mode Pulse Width Modulator Controller, based on Type UC1843. It shall be read in conjunction with ESA/SCC Generic Specification No. 9000, the requirements of which are supplemented herein.

1.2 COMPONENT TYPE VARIANTS

Variants of the basic type integrated circuits specified herein, which are also covered by this specification, are given in Table 1(a).

1.3 MAXIMUM RATINGS

The maximum ratings, which shall not be exceeded at any time during use or storage, applicable to the integrated circuits specified herein, are as scheduled in Table 1(b).

1.4 PARAMETER DERATING INFORMATION

The parameter derating information of the integrated circuits specified herein is shown in Figure 1.

1.5 PHYSICAL DIMENSIONS

The physical dimensions of the integrated circuits specified herein are shown in Figure 2.

1.6 PIN ASSIGNMENT

As per Figure 3(a).

1.7 TRUTH TABLE (FIGURE 3(b))

Not applicable.

1.8 CIRCUIT SCHEMATIC (FIGURE 3(c))

Not applicable.

1.9 FUNCTIONAL DIAGRAM

As per Figure 3(d).

1.10 HANDLING PRECAUTIONS

These devices are susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacture, testing, packaging, shipment and any handling.

These components are categorised as Class 3 with a Minimum Critical Path Failure Voltage of 4000 Volts.

**TABLE 1(a) - TYPE VARIANTS**

VARIANT	CASE	FIGURE	LEAD MATERIAL AND FINISH
01	D.I.L.	2	G4

TABLE 1(b) - MAXIMUM RATINGS

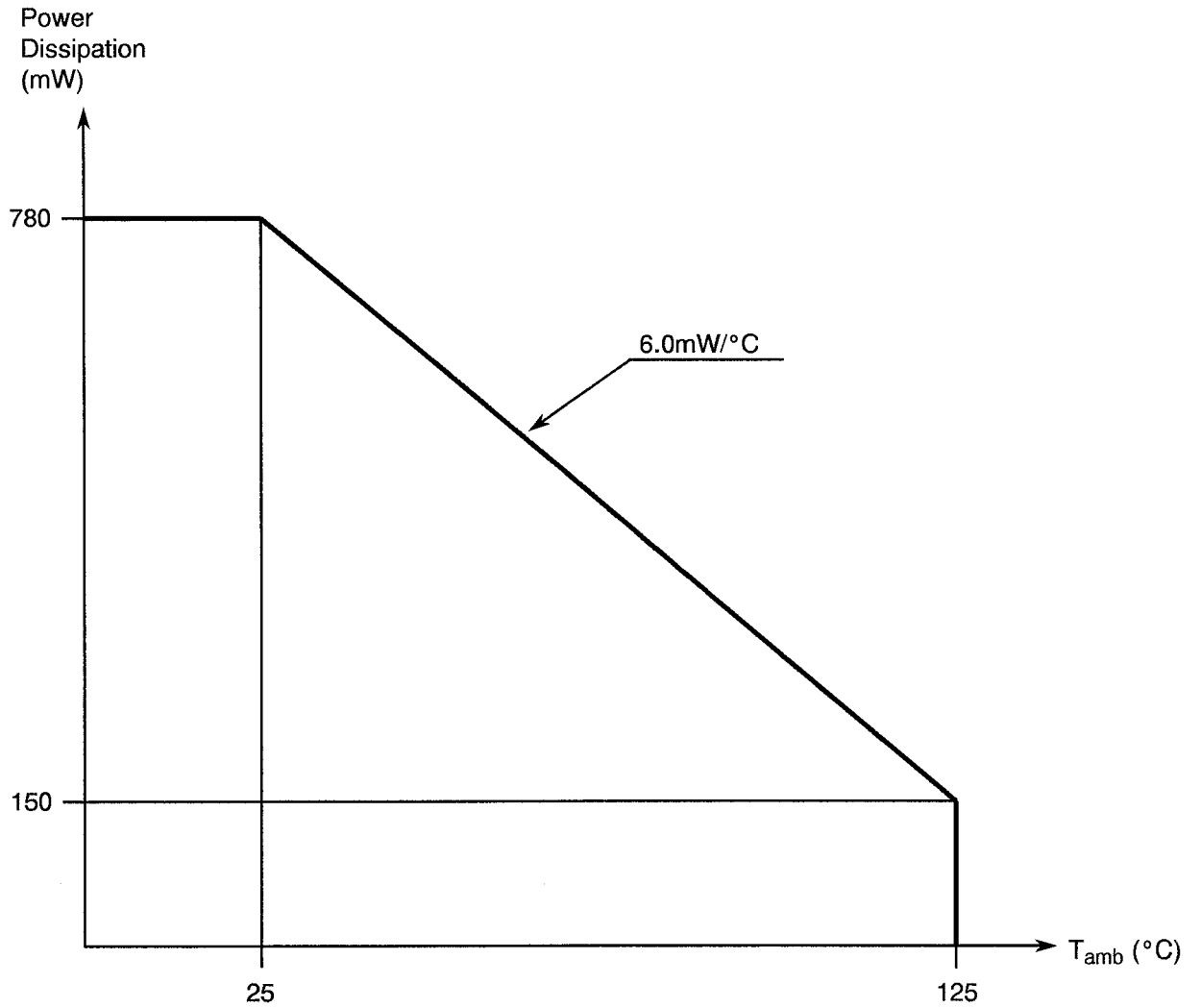
No.	CHARACTERISTICS	SYMBOL	MAXIMUM RATINGS	UNIT	REMARKS
1	Supply Voltage Range	V_{CC}	± 30	V	-
2	Output Current	I_{OUT}	± 1.0	A	-
3	Input Voltage Range	V_{IN}	-0.3 to 6.3	V	-
4	Output Sink Current	I_{SINK}	10	mA	-
5	Device Power Dissipation (Continuous)	P_D	780	mW	Note 1
6	Operating Temperature Range	T_{OP}	-55 to +125	°C	T_{amb}
7	Storage Temperature Range	T_{stg}	-65 to +150	°C	-
8	Soldering Temperature	T_{sol}	+265	°C	Note 2
8	Junction Temperature	T_J	+150	°C	-
10	Thermal Resistance	$R_{TH(J-C)}$	29	°C/W	-

NOTES

1. At $T_{amb} \leq +25^\circ\text{C}$. For derating at $T_{amb} > +25^\circ\text{C}$, see Figure 1.
2. Duration 10 seconds maximum at a distance of not less than 1.5mm from the device body and the same lead shall not be resoldered until 3 minutes have elapsed.



FIGURE 1 - PARAMETER DERATING INFORMATION

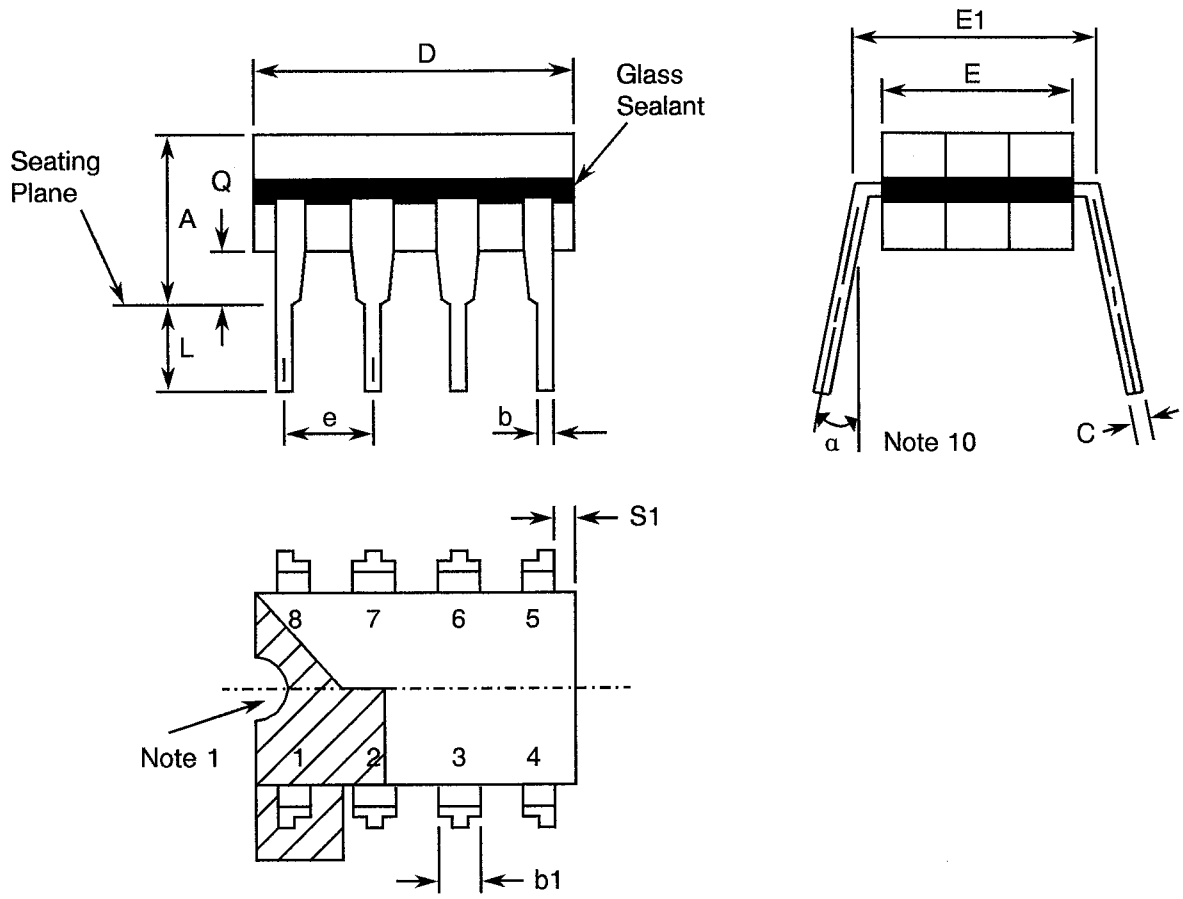


Power Dissipation versus Temperature



FIGURE 2 - PHYSICAL DIMENSIONS

FIGURE 2 - DUAL-IN-LINE PACKAGE, 8-PIN



SYMBOL	MILLIMETRES		NOTES
	MIN	MAX	
A	-	5.08	-
b	0.36	0.66	8
b1	1.14	1.65	8
C	0.20	0.38	8
D	-	10.29	-
E	5.59	7.87	-
E1	7.37	8.13	4
e	2.54 TYPICAL		6, 9
L	3.18	5.08	-
Q	0.38	1.52	3
S1	0.13	-	7
α	0°	15°	10

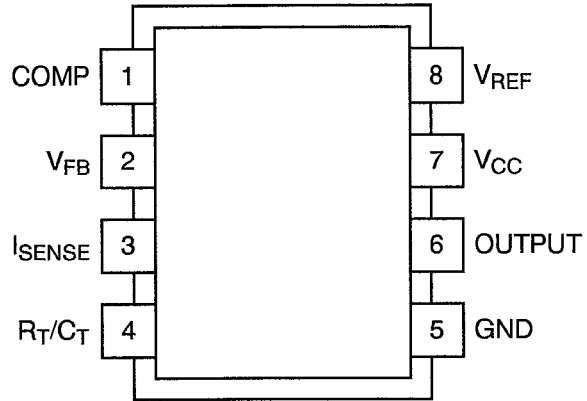
NOTES: See Page 9.

**FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)****NOTES TO FIGURE 2**

1. Index area: a notch or dot shall be located adjacent to Pin 1 and shall be within the shaded area shown.
2. Not applicable.
3. The dimension shall be measured from the seating plane to the base plane.
4. This dimension allows for off-centre lids, meniscus and glass overrun.
5. Not applicable.
6. The true position pin spacing is 2.54mm between centrelines. Each pin centreline shall be located within $\pm 0.25\text{mm}$ of its true longitudinal position relative to Pins 1 and the highest pin number.
7. Applies to all 4 corners.
8. All leads or terminals.
9. 6 spaces for dual-in-line packages.
10. Lead centre when α is 0° .



FIGURE 3(a) - PIN ASSIGNMENT



(TOP VIEW)

FIGURE 3(b) - TRUTH TABLE

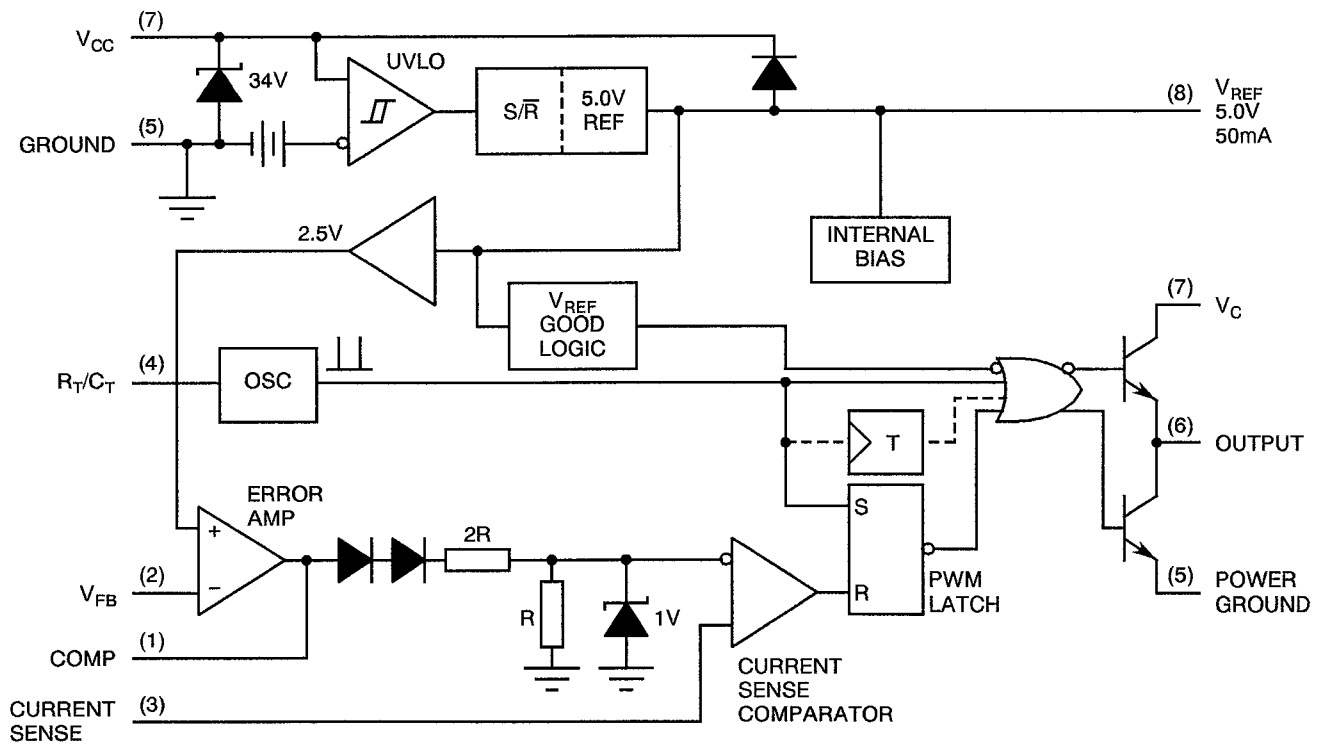
Not applicable.



FIGURE 3(c) - CIRCUIT SCHEMATIC

Not applicable.

FIGURE 3(d) - FUNCTIONAL DIAGRAM



**2. APPLICABLE DOCUMENTS**

The following documents form part of this specification and shall be read in conjunction with it:-

- (a) ESA/SCC Generic Specification No. 9000 for Integrated Circuits.
- (b) MIL-STD-883, Test Methods and Procedures for Micro-electronics.

3. TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESA/SCC Basic Specification No. 21300 shall apply. In addition, the following abbreviations are used:-

V_{CC} = Supply Voltage.

4. REQUIREMENTS**4.1 GENERAL**

The complete requirements for procurement of the integrated circuits specified herein are stated in this specification and ESA/SCC Generic Specification No. 9000 for Integrated Circuits. Deviations from the Generic Specification applicable to this specification only, are listed in Para. 4.2.

Deviations from the applicable Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESA/SCC requirements and do not affect the components' reliability, are listed in the appendices attached to this specification.

4.2 DEVIATIONS FROM GENERIC SPECIFICATION**4.2.1 Deviations from Special In-process Controls**

None.

4.2.2 Deviations from Final Production Tests (Chart II)

None.

4.2.3 Deviations from Burn-in and Electrical Measurements (Chart III)

- (a) Para. 7.1.1(a), "High Temperature Reverse Bias" tests and subsequent electrical measurements related to this test shall be omitted.

4.2.4 Deviations from Qualification Tests (Chart IV)

None.

4.2.5 Deviations from Lot Acceptance Tests (Chart V)

None.

4.3 MECHANICAL REQUIREMENTS**4.3.1 Dimension Check**

The dimensions of the integrated circuits specified herein shall be checked. They shall conform to those shown in Figure 2.



4.3.2 Weight

The maximum weight of the integrated circuits specified herein shall be 2.2 grammes.

4.4 MATERIALS AND FINISHES

The materials and finishes shall be as specified herein. Where a definite material is not specified, a material which will enable the integrated circuits specified herein to meet the performance requirements of this specification shall be used. Acceptance or approval of any constituent material does not guarantee acceptance of the finished product.

4.4.1 Case

The case shall be hermetically sealed and have a ceramic body and the lids shall be welded, brazed, preform-soldered or glass frit-sealed.

4.4.2 Lead Material and Finish

The lead material shall be Type 'G' with Type '4' finish in accordance with the requirements of ESA/SCC Basic Specification No. 23500.

4.5 MARKING

4.5.1 General

The marking of all components delivered to this specification shall be in accordance with the requirements of ESA/SCC Basic Specification No. 21700 and the following paragraphs. When the component is too small to accommodate all of the marking specified, as much as space permits shall be marked and the marking information, in full, shall accompany the component in its primary package.

The information to be marked and the order of precedence, shall be as follows:-

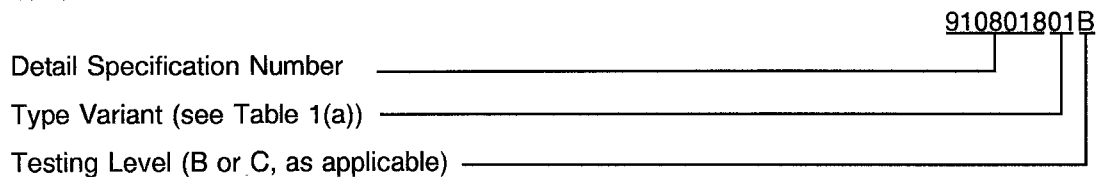
- (a) Lead Identification.
- (b) The SCC Component Number.
- (c) Traceability Information.

4.5.2 Lead Identification

An index shall be located at the top of the package in the position defined in Note 1 to Figure 2 or, alternatively, a tab may be used to identify Pin No. 1. The pin numbering must be read with the index or tab on the left-hand side.

4.5.3 The SCC Component Number

Each component shall bear the SCC Component Number which shall be constituted and marked as follows:



4.5.4 Traceability Information

Each component shall be marked in respect of traceability information in accordance with the requirements of ESA/SCC Basic Specification No. 21700.



4.6 ELECTRICAL MEASUREMENTS

4.6.1 Electrical Measurements at Room Temperature

The parameters to be measured in respect of electrical characteristics are scheduled in Table 2. Unless otherwise specified, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.6.2 Electrical Measurements at High and Low Temperatures

The parameters to be measured at high and low temperatures are scheduled in Table 3. The measurements shall be performed at $T_{amb} = +125(+0-5)$ and $-55(+5-0)$ °C respectively.

4.6.3 Circuits for Electrical Measurements

Circuits for use in performing the electrical measurements listed in Tables 2 and 3 of this specification are shown in Figure 4.

4.7 BURN-IN TESTS

4.7.1 Parameter Drift Values

The parameter drift values applicable to burn-in are specified in Table 4 of this specification. Unless otherwise stated, measurements shall be performed at $T_{amb} = +22 \pm 3$ °C. The parameter drift values (Δ) applicable to the parameters scheduled, shall not be exceeded. In addition to these drift value requirements, the appropriate limit value specified for a given parameter in Table 2 shall not be exceeded.

4.7.2 Conditions for High Temperature Reverse Bias Burn-in (Table 5(a))

Not applicable.

4.7.3 Conditions for Power Burn-in

The requirements for power burn-in are specified in Section 7 of ESA/SCC Generic Specification No. 9000. The conditions for power burn-in shall be as specified in Table 5(b) of this specification.

4.7.4 Electrical Circuits for High Temperature Reverse Bias Burn-in (Figure 5(a))

Not applicable.

4.7.5 Electrical Circuits for Power Burn-in

Circuits for use in performing the power burn-in tests are shown in Figure 5(b) of this specification.

**TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS**

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
1	Reference Output Voltage	V_{REF}	-	4(a)	$V_{CC} = 15V$, $I_{OUT} = 1.0mA$ (Pin 8)	4.95	5.05	V
2	Line Regulation	K_{LI}	-	4(a)	$V_{CC} = 12V$ or $25V$ (Pin 8)	-	20	mV
3	Load Regulation	K_{LO}	-	4(a)	$V_{CC} = 15V$ $I_{OUT} = 1.0mA$ or $20mA$ (Pin 8)	-	25	mV
4	Output Short Circuit Current	I_{OS}	-	4(b)	$V_{CC} = 15V$ (Pin 8)	- 30	- 180	mA
5	Input Voltage	V_{IN}	4001	4(c)	$V_{CC} = 15V$, $V_{PIN1} = 2.5V$ (Pin 2)	2.45	2.55	V
6	Input Bias Current	I_{IB}	4001	4(d)	$V_{CC} = 15V$ (Pin 2)	- 1.0	1.0	μA
7	Open Loop Voltage Gain	A_{VOL}	4004	4(e)	$V_{CC} = 15V$ $V_{PIN1} = 2.0V$ or $4.0V$ (Pin 2)	65	-	dB
8	Power Supply Rejection Ratio	PSRR	4003	4(f)	$V_{CC} = 12V$ or $25V$ (Pin 2)	60	-	dB
9	Output Sink Current	I_{SINK}	-	4(g)	$V_{CC} = 15V$ $V_{PIN1} = 1.1V$, $V_{PIN2} = 2.7V$ (Pin 1)	2.0	-	mA
10	Output Source Current	I_{SOURCE}	-	4(g)	$V_{CC} = 15V$ $V_{PIN1} = 5.0V$, $V_{PIN2} = 2.3V$ (Pin 1)	- 0.5	-	mA
11	Output Voltage High Level	V_{OH}	3006	4(h)	$V_{CC} = 15V$ $V_{PIN2} = 2.3V$, $R_L = 15k\Omega$ (Pin 1)	5.0	-	V
12	Output Voltage Low Level	V_{OL}	3007	4(h)	$V_{CC} = 15V$ $V_{PIN2} = 2.7V$, $R_L = 15k\Omega$ (Pin 1)	-	1.1	V
13	Gain	A_V	4004	4(i)	$V_{CC} = 15V$, $V_{PIN2} = 0V$ $V_{PIN3} = 0V$ or $0.8V$ (Pin 1)	2.85	3.15	-
14	Maximum Input Signal	-	-	4(j)	$V_{CC} = 15V$ (Pin 3)	0.9	1.1	V
15	Input Bias Current (Sense)	I_{IBSC}	4001	4(k)	$V_{CC} = 15V$, $V_{PIN3} = 0V$ (Pin 3)	- 10	-	μA

**TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS (CONT'D)**

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
16	Output Voltage Low Level 1	V _{OL1}	3007	4(l)	V _{CC} = 15V, I _{SINK} = 20mA (Pin 6)	-	0.4	V
17	Output Voltage Low Level 2	V _{OL2}	3007	4(l)	V _{CC} = 15V, I _{SINK} = 200mA (Pin 6)	-	2.2	V
18	Output Voltage High Level 1	V _{OH1}	3006	4(m)	V _{CC} = 15V, I _{SOURCE} = 20mA (Pin 6)	13	-	V
19	Output Voltage High Level 2	V _{OH2}	3006	4(m)	V _{CC} = 15V, I _{SOURCE} = 200mA (Pin 6)	12	-	V
20	Threshold Voltage	V _{TH}	4001	4(n)	V _{CC} ≤ 7.0V to ≥ 9.0V (Pin 7)	7.8	9.0	V
21	Minimum Operating Voltage	V _{MIN}	4001	4(n)	V _{CC} ≥ 9.0V to ≤ 7.0V (Pin 7)	7.0	8.2	V
22	Maximum Duty Cycle	DC _{MAX}	-	4(o)	V _{CC} = 15V (Pin 6)	95	100	%
23	Minimum Duty Cycle	DC _{MIN}	-	4(o)	V _{CC} = 15V (Pin 6)	-	0	%
24	Start-Up Current	I _{START}	-	4(p)	V _{CC} ≤ 7.0V or = 7.0V (Pin 7)	-	1.0	mA
25	Supply Current (Standby)	I _{CC}	3005	4(p)	V _{CC} = 15V (Pin 7)	-	17	mA

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
26	Initial Accuracy	f _{OSC}	-	4(q)	V _{CC} = 15V (Pin 4)	47	57	kHz
27	Voltage Stability	Δf _{OSC}	-	4(q)	V _{CC} = 12V or 25V (Pin 4)	-	1.0	%



TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES - d.c. PARAMETERS

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
1	Reference Output Voltage	V_{REF}	-	4(a)	$V_{CC} = 15V$, $I_{OUT} = 1.0mA$ (Pin 8)	4.90	5.10	V
2	Line Regulation	K_{LI}	-	4(a)	$V_{CC} = 12V$ or $25V$ (Pin 8)	-	20	mV
3	Load Regulation	K_{LO}	-	4(a)	$V_{CC} = 15V$ $I_{OUT} = 1.0mA$ or $20mA$ (Pin 8)	-	25	mV
4	Output Short Circuit Current	I_{OS}	-	4(b)	$V_{CC} = 15V$ (Pin 8)	-30	-180	mA
5	Input Voltage	V_{IN}	4001	4(c)	$V_{CC} = 15V$, $V_{PIN1} = 2.5V$ (Pin 2)	2.45	2.55	V
6	Input Bias Current	I_{IB}	4001	4(d)	$V_{CC} = 15V$ (Pin 2)	-1.0	1.0	μA
7	Open Loop Voltage Gain	A_{VOL}	4004	4(e)	$V_{CC} = 15V$ $V_{PIN1} = 2.0V$ or $4.0V$ (Pin 2)	65	-	dB
8	Power Supply Rejection Ratio	PSRR	4003	4(f)	$V_{CC} = 12V$ or $25V$ (Pin 2)	60	-	dB
9	Output Sink Current	I_{SINK}	-	4(g)	$V_{CC} = 15V$ $V_{PIN1} = 1.1V$, $V_{PIN2} = 2.7V$ (Pin 1)	2.0	-	mA
10	Output Source Current	I_{SOURCE}	-	4(g)	$V_{CC} = 15V$ $V_{PIN1} = 5.0V$, $V_{PIN2} = 2.3V$ (Pin 1)	-0.5	-	mA
11	Output Voltage High Level	V_{OH}	3006	4(h)	$V_{CC} = 15V$ $V_{PIN2} = 2.3V$, $R_L = 15k\Omega$ (Pin 1)	5.0	-	V
12	Output Voltage Low Level	V_{OL}	3007	4(h)	$V_{CC} = 15V$ $V_{PIN2} = 2.7V$, $R_L = 15k\Omega$ (Pin 1)	-	1.1	V
13	Gain	A_V	4004	4(i)	$V_{CC} = 15V$, $V_{PIN2} = 0V$ $V_{PIN3} = 0V$ or $0.8V$ (Pin 1)	2.85	3.15	-
14	Maximum Input Signal	-	-	4(j)	$V_{CC} = 15V$ (Pin 3)	0.9	1.1	V
15	Input Bias Current (Sense)	I_{IBSC}	4001	4(k)	$V_{CC} = 15V$, $V_{PIN3} = 0V$ (Pin 3)	-10	-	μA

**TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES - d.c. PARAMETERS
(CONT'D)**

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
16	Output Voltage Low Level 1	V _{OL1}	3007	4(l)	V _{CC} = 15V, I _{SINK} = 20mA (Pin 6)	-	0.4	V
17	Output Voltage Low Level 2	V _{OL2}	3007	4(l)	V _{CC} = 15V, I _{SINK} = 200mA (Pin 6)	-	2.2	V
18	Output Voltage High Level 1	V _{OH1}	3006	4(m)	V _{CC} = 15V, I _{SOURCE} = 20mA (Pin 6)	13	-	V
19	Output Voltage High Level 2	V _{OH2}	3006	4(m)	V _{CC} = 15V, I _{SOURCE} = 200mA (Pin 6)	12	-	V
20	Threshold Voltage	V _{TH}	4001	4(n)	V _{CC} ≤ 7.0V to ≥ 9.0V (Pin 7)	7.8	9.0	V
21	Minimum Operating Voltage	V _{MIN}	4001	4(n)	V _{CC} ≥ 9.0V to ≤ 7.0V (Pin 7)	7.0	8.2	V
22	Maximum Duty Cycle	DC _{MAX}	-	4(o)	V _{CC} = 15V (Pin 6)	95	100	%
23	Minimum Duty Cycle	DC _{MIN}	-	4(o)	V _{CC} = 15V (Pin 6)	-	0	%
24	Start-Up Current	I _{START}	-	4(p)	V _{CC} ≤ 7.0V or = 7.0V (Pin 7)	-	1.0	mA
25	Supply Current (Standby)	I _{CC}	3005	4(p)	V _{CC} = 15V (Pin 7)	-	17	mA

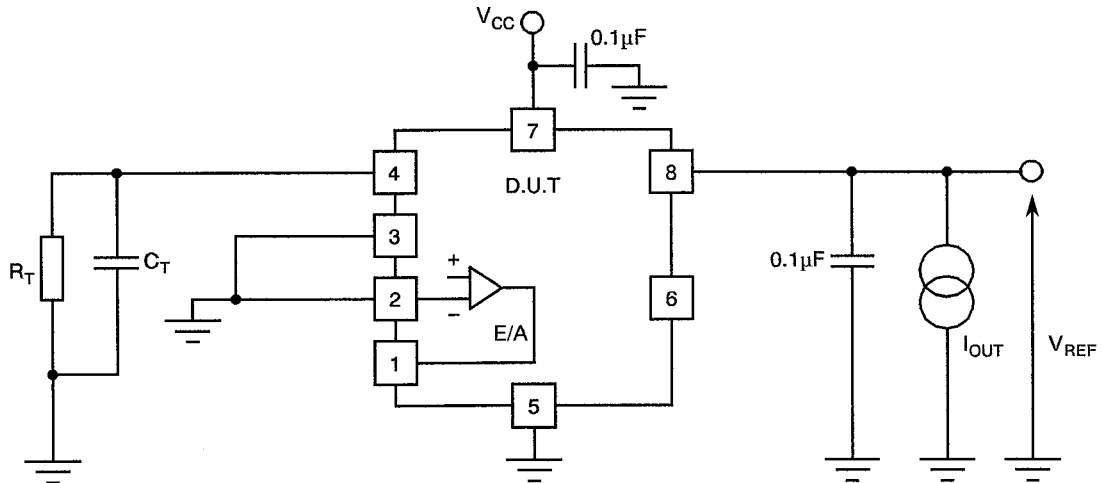
TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES - a.c. PARAMETERS

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
26	Initial Accuracy	f _{OSC}	-	4(q)	V _{CC} = 15V (Pin 4)	42	62	kHz
27	Voltage Stability	Δf _{OSC}	-	4(q)	V _{CC} = 12V or 25V (Pin 4)	-	1.0	%



FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS

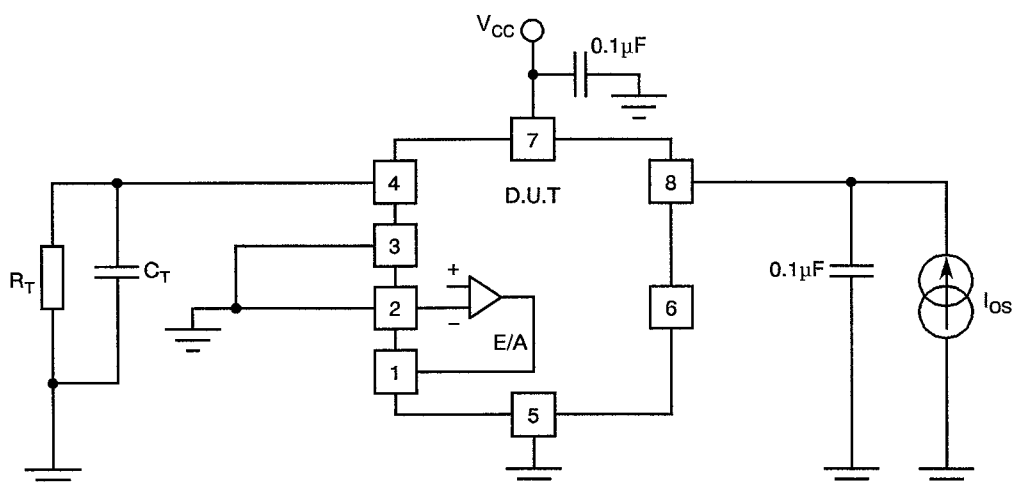
FIGURE 4(a) - "REFERENCE SECTION": OUTPUT VOLTAGE, LINE AND LOAD REGULATION



NOTES

1. $R_T = 10k\Omega$, $C_T = 3.3nF$.
2. Test 1: Measure V_{REF} on Pin 8 with $I_{OUT} = 1.0mA$.
3. Test 2: Measure $V_{REF} = V_{REF1}$ on Pin 8 when $V_{CC} = 12V$, and $V_{REF} = V_{REF2}$ when $V_{CC} = 25V$:
 $K_{LI} = V_{REF2} - V_{REF1}$
4. Test 3: Measure $V_{REF} = V_{REF1}$ on Pin 8 when $I_{OUT} = 1.0mA$, and $V_{REF} = V_{REF2}$ when $I_{OUT} = 20mA$:
 $K_{LO} = V_{REF1} - V_{REF2}$

FIGURE 4(b) - "REFERENCE SECTION": OUTPUT SHORT CIRCUIT CURRENT



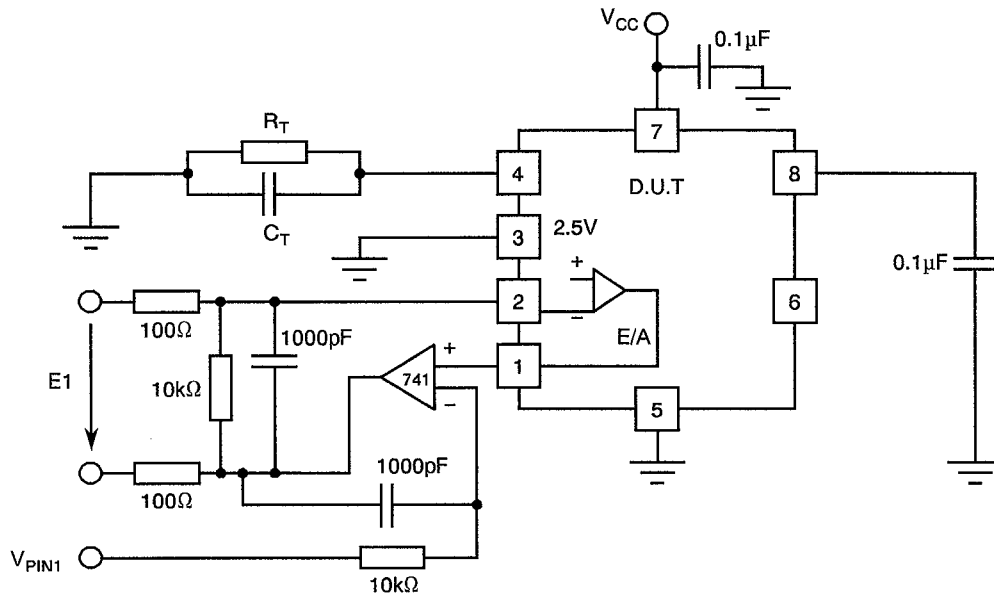
NOTES

1. $R_T = 10k\Omega$, $C_T = 3.3nF$.
2. Test 4: Measure I_{OS} into Pin 8.



FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

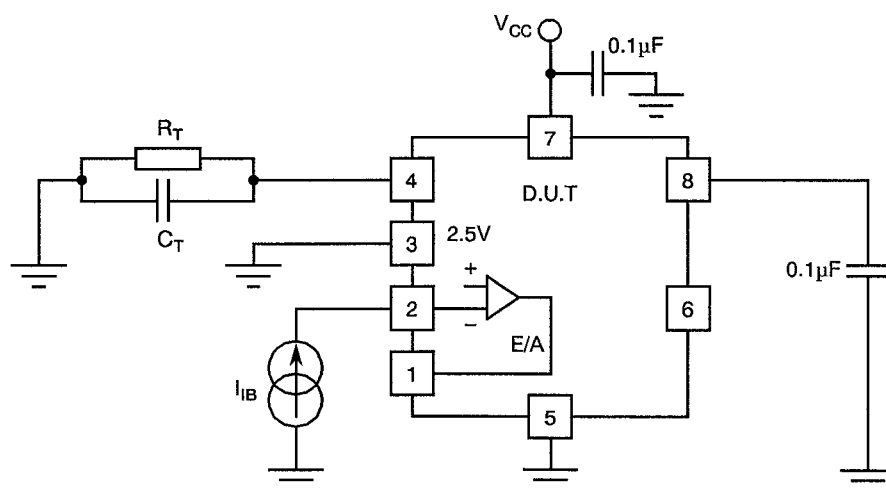
FIGURE 4(c) - "ERROR AMPLIFIER SECTION": INPUT VOLTAGE



NOTES

1. $R_T = 10k\Omega$, $C_T = 3.3nF$.
2. Test 5: Measure E1 on Pin 2 when $V_{PIN1} = 2.5V$: $V_{IN} = \frac{E1}{101}$

FIGURE 4(d) - "ERROR AMPLIFIER SECTION": INPUT BIAS CURRENT



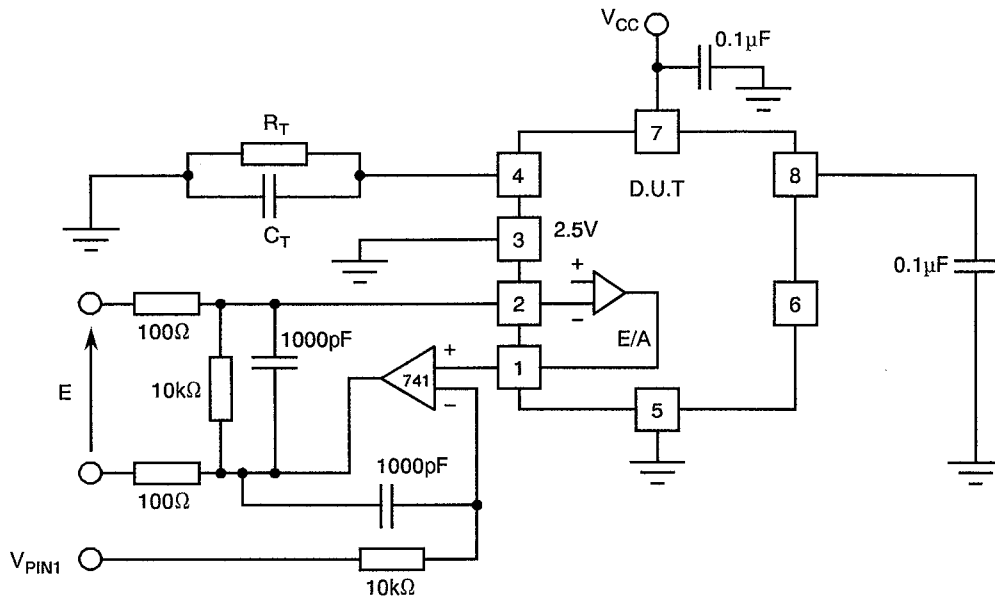
NOTES

1. $R_T = 10k\Omega$, $C_T = 3.3nF$.
2. Test 6: Measure I_{IB} into Pin 2.



FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

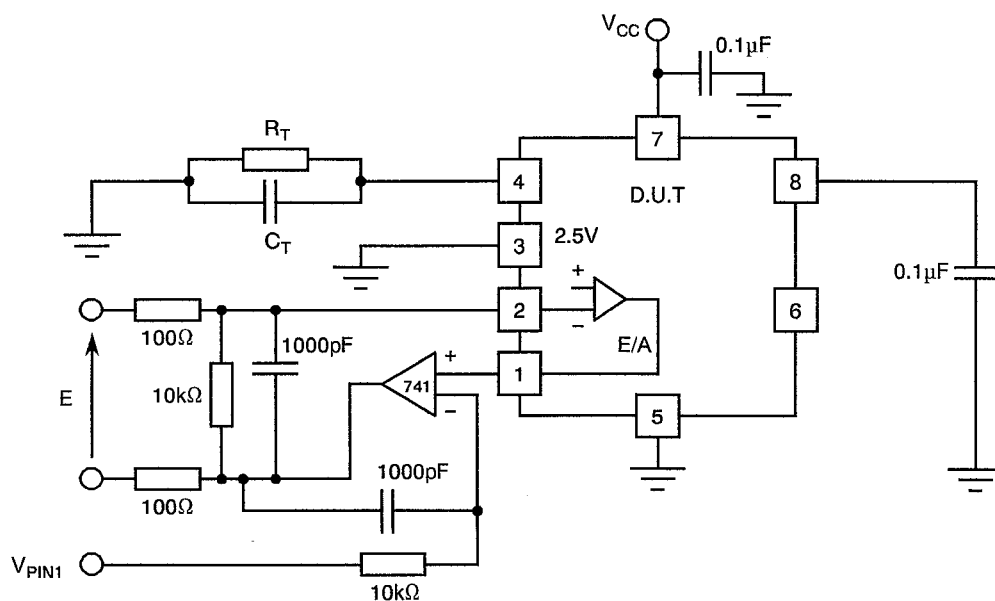
FIGURE 4(e) - "ERROR AMPLIFIER SECTION": OPEN LOOP VOLTAGE GAIN



NOTES

1. $R_T = 10k\Omega$, $C_T = 3.3nF$.
2. Test 7: Measure $E = E1$ when $V_{PIN1} = 2.0V$ and $-E = E2$ when $V_{PIN1} = 4.0V$. $A_{VOL} = 20 \text{ Log } \frac{202}{E2 - E1}$

FIGURE 4(f) - "ERROR AMPLIFIER SECTION": POWER SUPPLY REJECTION RATIO



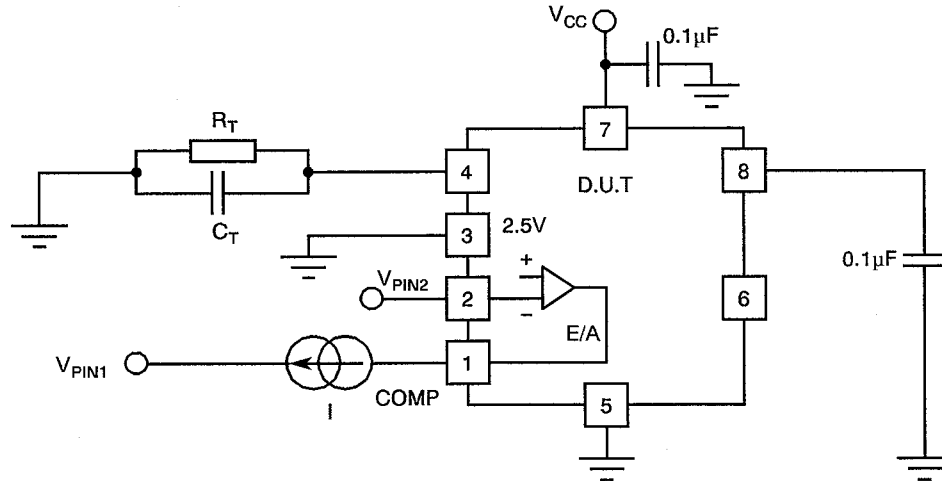
NOTES

1. $R_T = 10k\Omega$, $C_T = 3.3nF$.
2. Test 8: Measure $E = E1$ on Pin 2 when $V_{CC} = 12V$ and $-E = E2$ when $V_{CC} = 25V$. $PSRR = 20 \text{ Log } \frac{1313}{E2 - E1}$



FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

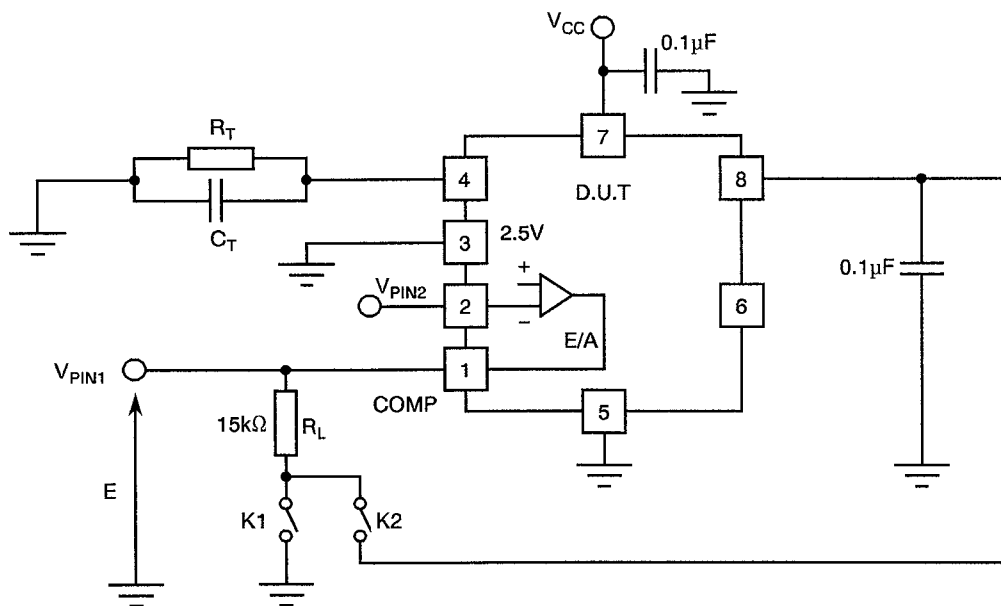
FIGURE 4(g) - "ERROR AMPLIFIER SECTION": OUTPUT SINK AND SOURCE CURRENT



NOTES

1. $R_T = 10k\Omega$, $C_T = 3.3nF$.
2. Test 9: Measure $I = I_{SINK}$ into Pin 1 when $V_{PIN1} = 1.1V$ and $V_{PIN2} = 2.7V$.
3. Test 10: Measure $I = I_{SOURCE}$ into Pin 1 when $V_{PIN1} = 50V$ and $V_{PIN2} = 2.3V$.

FIGURE 4(h) - "ERROR AMPLIFIER SECTION": OUTPUT VOLTAGE HIGH AND LOW LEVELS



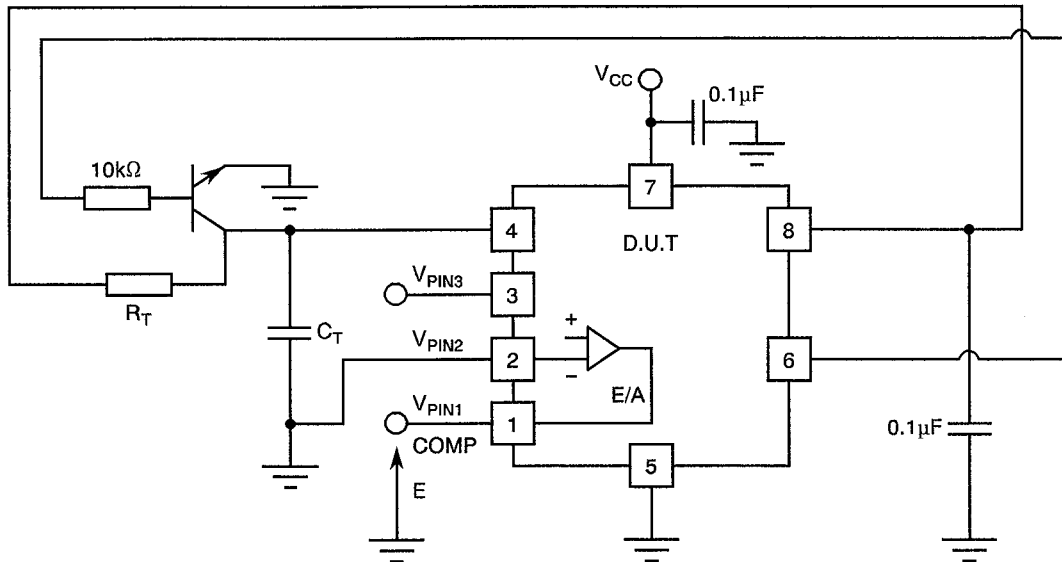
NOTES

1. $R_T = 10k\Omega$, $C_T = 3.3nF$.
2. Test 11: When K1 closed and K2 open, measure $E = E1$ with $V_{PIN2} < 2.3V$. $E1 = V_{OH}$.
3. Test 12: When K1 open and K2 closed, measure $E = E2$ with $V_{PIN2} > 2.7V$. $E2 = V_{OL}$.



FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(i) - "CURRENT SENSE SECTION": GAIN

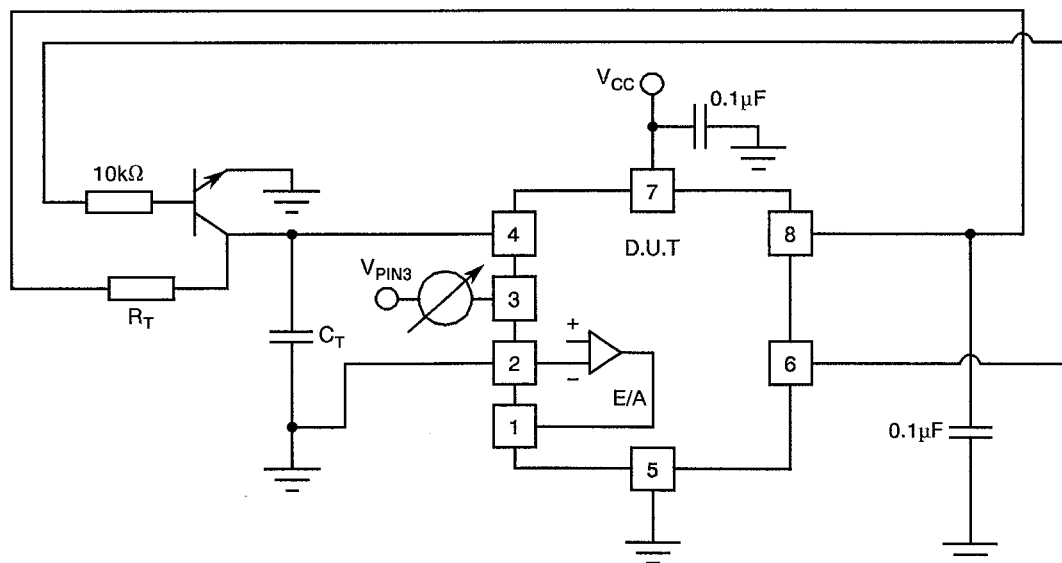


NOTES

1. $R_T = 10k\Omega$, $C_T = 3.3nF$.
2. Parameter measured at trip point of latch with $V_{PIN2} = 0V$.
3. Test 13: Set $V_{PIN3} = 0V$, Adjust V_{PIN1} down from 5.0V until OUTPUT goes LOW then measure $E = E1$.
Set $V_{PIN3} = 0.8V$, Adjust V_{PIN1} down from 5.0V until OUTPUT goes LOW then measure $E = E2$.

$$A_V = \frac{E2 - E1}{0.8}$$

FIGURE 4(j) - "CURRENT SENSE SECTION": MAXIMUM INPUT SIGNAL



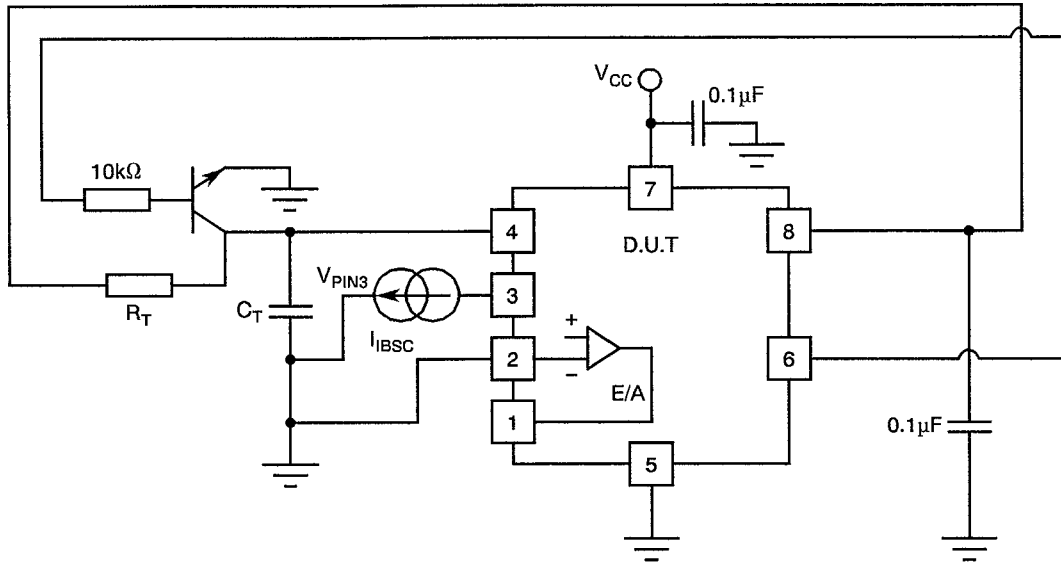
NOTES

1. $R_T = 10k\Omega$, $C_T = 3.3nF$.
2. Test 14: Set $V_{PIN3} = 0V$, OUTPUT goes HIGH. Then adjust V_{PIN3} until OUTPUT goes LOW then measure V_{PIN3} .



FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

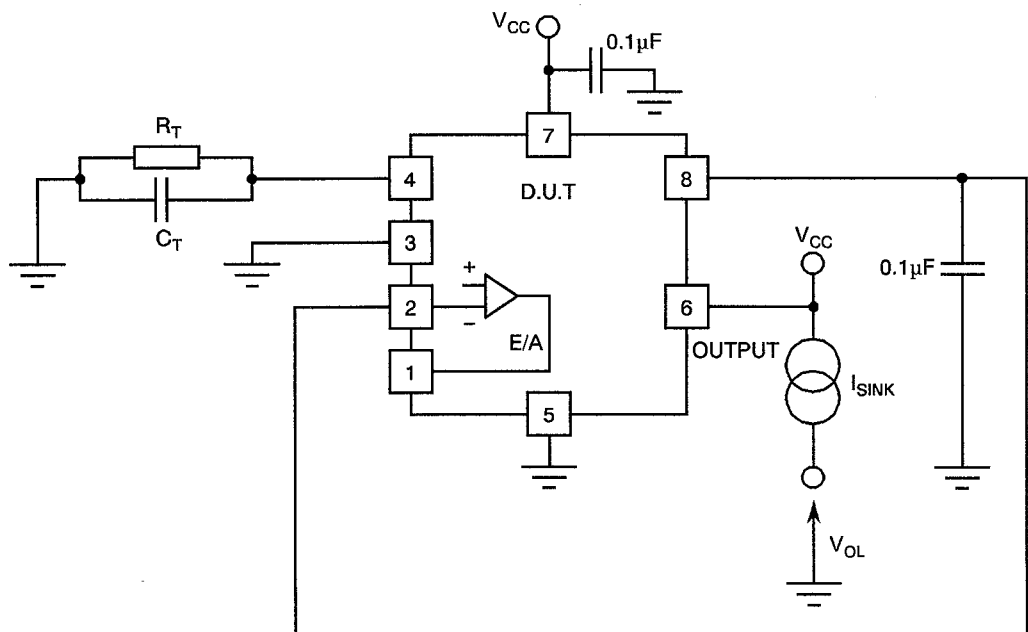
FIGURE 4(k) - "CURRENT SENSE SECTION": INPUT BIAS CURRENT



NOTES

1. $R_T = 10k\Omega$, $C_T = 3.3nF$.
2. Test 15: Measure I_{IBSC} into Pin 3 with $V_{PIN3} = 0V$.

FIGURE 4(l) - "OUTPUT SECTION": OUTPUT VOLTAGE LOW LEVEL



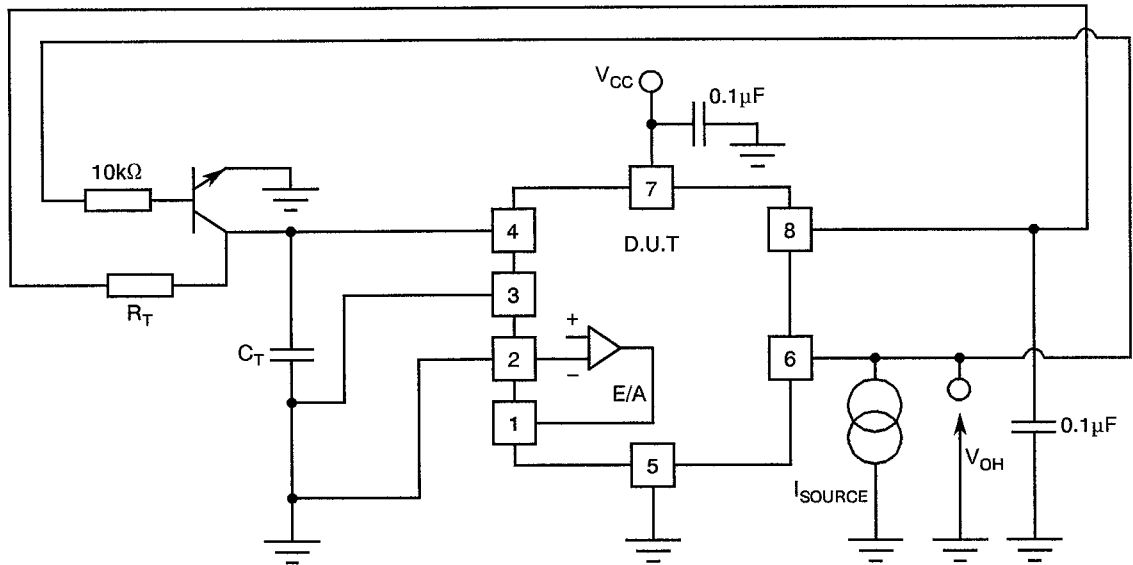
NOTES

1. $R_T = 10k\Omega$, $C_T = 3.3nF$.
2. Test 16: Measure $V_{OL} = V_{OL1}$ on Pin 6 with $I_{SINK} = 20mA$.
3. Test 17: Measure $V_{OL} = V_{OL2}$ on Pin 6 with $I_{SINK} = 200mA$.



FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

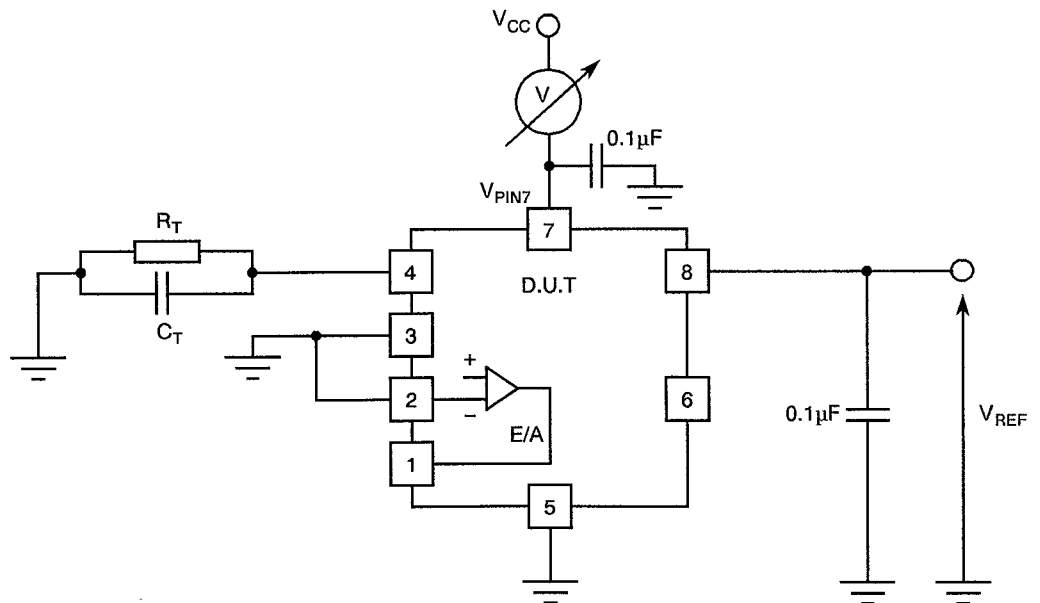
FIGURE 4(m) - "OUTPUT SECTION": OUTPUT VOLTAGE HIGH LEVEL



NOTES

1. $R_T = 10k\Omega$, $C_T = 3.3nF$.
2. Test 18: Measure $V_{OH} = V_{OH1}$ on Pin 6 with $I_{SOURCE} = 20mA$.
3. Test 19: Measure $V_{OH} = V_{OH2}$ on Pin 6 with $I_{SOURCE} = 200mA$.

FIGURE 4(n) - "UNDER VOLTAGE LOCKOUT SECTION": THRESHOLD AND MINIMUM OPERATING VOLTAGE



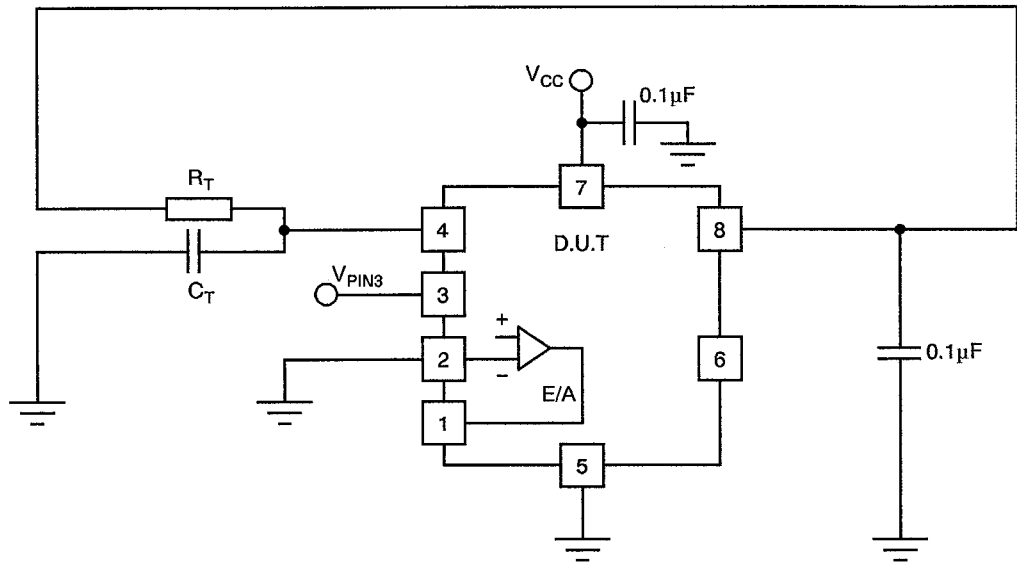
NOTES

1. $R_T = 10k\Omega$, $C_T = 3.3nF$.
2. Test 20: Measure $V_{PIN7} = V_{TH}$ by setting V_{CC} below 7.0V then adjusting up to 9.0V until $V_{REF} > 4.0V$.
3. Test 21: Measure $V_{PIN7} = V_{MIN}$ by setting V_{CC} above V_{TH} then adjusting down to 7.0V until $V_{REF} < 4.0V$.

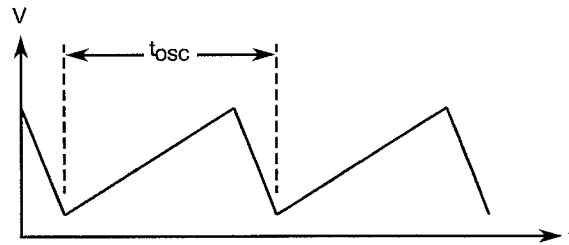


FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

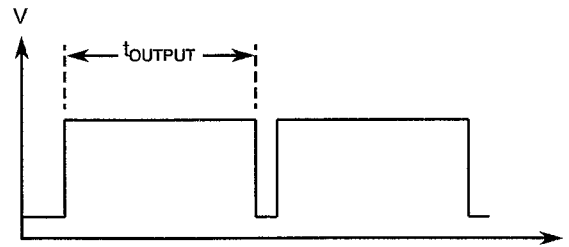
FIGURE 4(o) - "PWM SECTION": MAXIMUM AND MINIMUM DUTY CYCLE



R_T/C_T Voltage Waveform:



OUTPUT Voltage Waveform:



NOTES

1. $R_T = 10k\Omega$, $C_T = 3.3nF$.

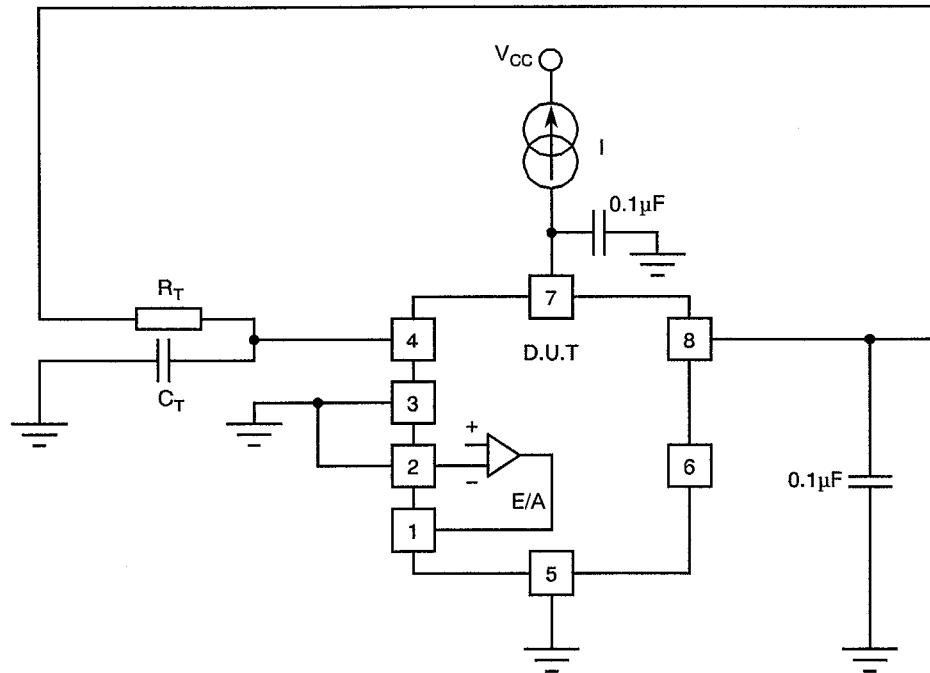
2. Test 22: When $V_{PIN3} = 0V$, measure t_{OUTPUT} : $DC_{MAX} = \frac{t_{OUTPUT}}{t_{osc}}$

3. Test 23: When $V_{PIN3} = 1.2V$, measure t_{OUTPUT} : $DC_{MIN} = \frac{t_{OUTPUT}}{t_{osc}}$



FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(p) - TOTAL STANDBY CURRENT



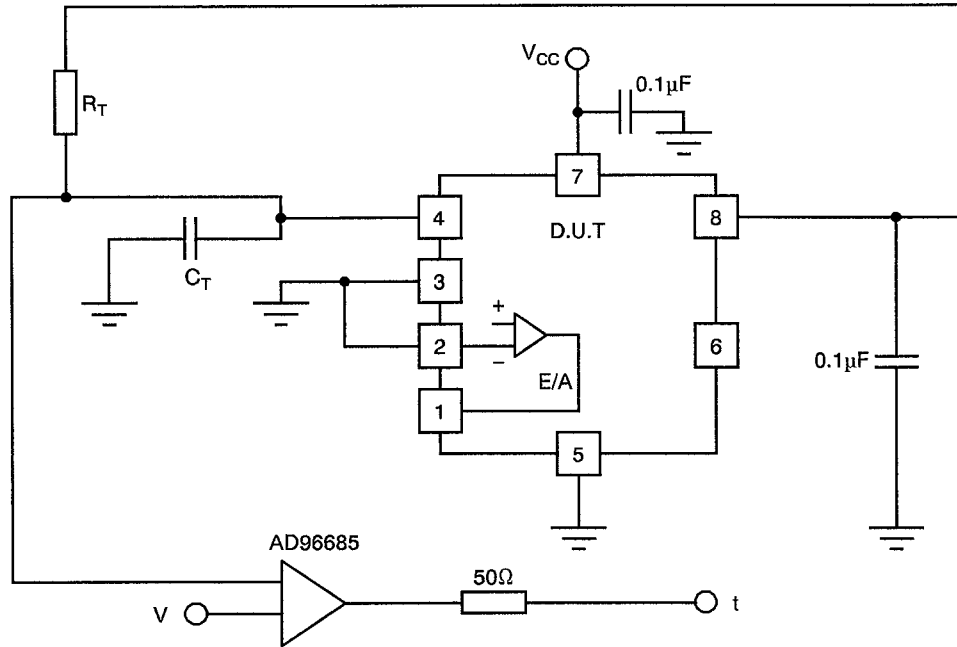
NOTES

1. $R_T = 10k\Omega$, $C_T = 3.3nF$.
2. Test 24: Measure $I = I_{START}$ into Pin 7 by setting V_{CC} below 7.0V to ensure Under Voltage Lockout (UVLO) mode then set to 7.0V.
3. Test 25: Measure $I = I_{CC}$ into Pin 7 by setting V_{CC} to 15V.

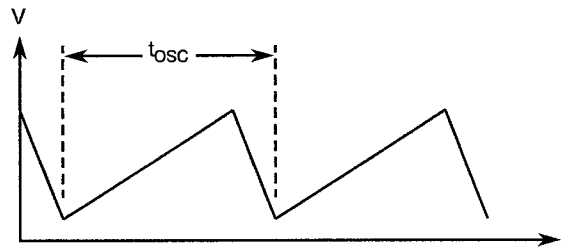


FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(g) - "OSCILLATOR SECTION"



R_T/C_T Voltage Waveform:



NOTES

1. $R_T = 10k\Omega$, $C_T = 3.3nF$.

2. Test 26: Measure $t = t_1$ when $V = 1.8V$. $f_{osc} = \frac{1}{t_1}$

3. Test 27: Measure $t = t_2$ when $V_{CC} = 12V$.

Measure $t = t_3$ when $V_{CC} = 25V$. $\Delta f_{osc} = \frac{1/t_3 - 1/t_2}{f_{osc}}$

**TABLE 4 - PARAMETER DRIFT VALUES**

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	CHANGE LIMITS (Δ)	UNIT
1	Reference Output Voltage	V_{REF}	As per Table 2	As per Table 2	± 40	mV
2	Line Regulation	K_{LI}	As per Table 2	As per Table 2	± 3.0	mV
6	Input Bias Current	I_{IB}	As per Table 2	As per Table 2	± 100	nA
11	Output Voltage High Level	V_{OH}	As per Table 2	As per Table 2	± 10	%
12	Output Voltage Low Level	V_{OL}	As per Table 2	As per Table 2	± 10	%
25	Supply Current (Standby)	I_{CC}	As per Table 2	As per Table 2	± 10	%
26	Initial Accuracy	f_{OSC}	As per Table 2	As per Table 2	± 10	%



TABLE 5(a) - CONDITIONS FOR HIGH TEMPERATURE REVERSE BIAS BURN-IN

Not applicable.

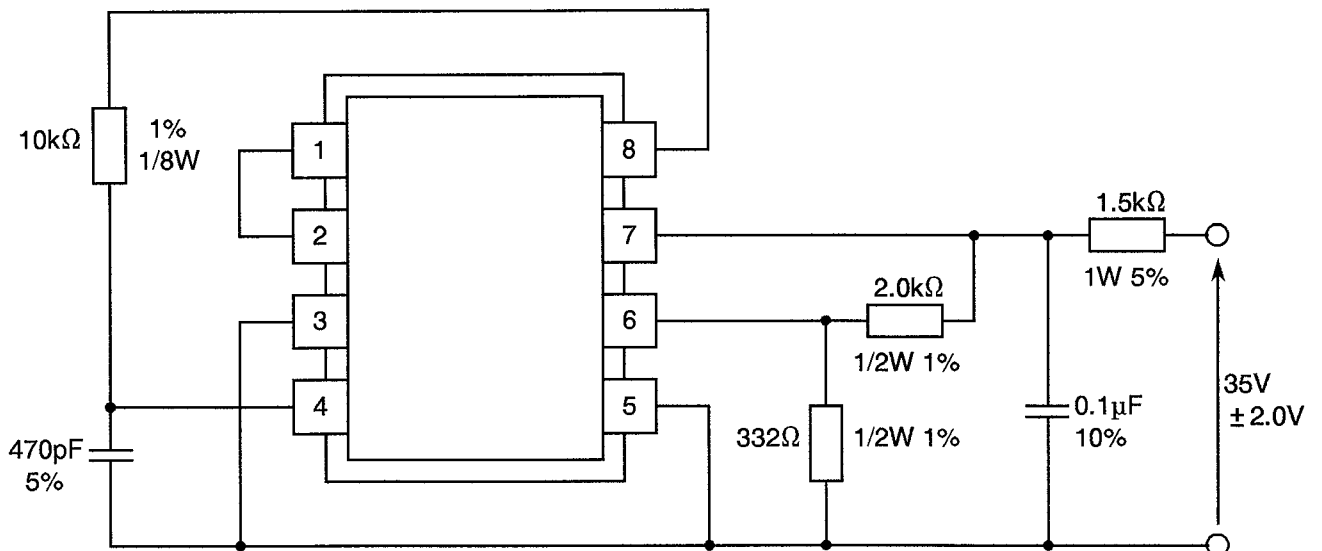
TABLE 5(b) - CONDITIONS FOR POWER BURN-IN AND OPERATING LIFE TESTS

No.	CHARACTERISTICS	SYMBOL	CONDITION	UNIT
1	Ambient Temperature	T_{amb}	+ 125(+ 0 - 5)	°C
2	Power Supply Voltage	V_{CC}	35	V
3	Negative Supply Voltage	V_{EE}	0	V

FIGURE 5(a) - ELECTRICAL CIRCUIT FOR HIGH TEMPERATURE REVERSE BIAS BURN-IN

Not applicable.

FIGURE 5(b) - ELECTRICAL CIRCUIT FOR POWER BURN-IN AND OPERATING LIFE TESTS



NOTES

- Unless otherwise specified: For resistors, wattage values at $T_{amb} = +125^{\circ}\text{C}$. All capacitors are rated 50V at $T_{amb} = +125^{\circ}\text{C}$.



4.8 ENVIRONMENTAL AND ENDURANCE TESTS (CHARTS IV AND V OF ESA/SCC GENERIC SPECIFICATION NO. 9000)

4.8.1 Electrical Measurements on Completion of Environmental Tests

The parameters to be measured on completion of environmental tests are scheduled in Table 6. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.8.2 Electrical Measurements at Intermediate Points during Endurance Tests

The parameters to be measured at intermediate points during endurance tests are as scheduled in Table 6 of this specification. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.8.3 Electrical Measurements on Completion of Endurance Tests

The parameters to be measured on completion of endurance testing are as scheduled in Table 6 of this specification. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.8.4 Conditions for Operating Life Tests

The requirements for operating life testing are specified in Section 9 of ESA/SCC Generic Specification No. 9000. The conditions for operating life testing shall be as specified in Table 5(b) of this specification.

4.8.5 Electrical Circuits for Operating Life Tests

Circuits for use in performing the operating life tests are shown in Figure 5(b) of this specification.

4.8.6 Conditions for High Temperature Storage Test

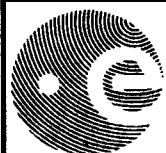
The requirements for the high temperature storage test are specified in ESA/SCC Generic Specification No. 9000. The temperature to be applied shall be the maximum storage temperature specified in Table 1(b) of this specification.

**TABLE 6 - ELECTRICAL MEASUREMENTS ON COMPLETION OF ENVIRONMENTAL TESTS AND AT INTERMEDIATE POINTS AND ON COMPLETION OF ENDURANCE TESTING**

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	CHANGE LIMITS (Δ) (NOTE 1)	ABSOLUTE		UNIT
						MIN.	MAX.	
1	Reference Output Voltage	V_{REF}	As per Table 2	As per Table 2	$\pm 40\text{mV}$	4.95	5.05	V
2	Line Regulation	K_{LI}	As per Table 2	As per Table 2	$\pm 3.0\text{mV}$	-	20	mV
6	Input Bias Current	I_{IB}	As per Table 2	As per Table 2	$\pm 100\text{nA}$ or (2) $\pm 100\%$	-1.0	1.0	μA
25	Supply Current (Standby)	I_{CC}	As per Table 2	As per Table 2	$\pm 10\%$	-	17	mA
26	Initial Accuracy	f_{OSC}	As per Table 2	As per Table 2	$\pm 10\%$	47	57	kHz

NOTES

1. The change limits (Δ) are applicable to the Operating Life test only. The change in parameters between initial and end point measurements shall not exceed the limits given. In addition, the absolute limits shall not be exceeded.
2. Whichever is greater, referred to the initial value.

**ESCE**ESA/SCC Detail Specification
No. 9108/018

PAGE 33

ISSUE 1

APPENDIX 'A'Page 1 of 1**AGREED DEVIATIONS FOR UNITRODE (USA)**

ITEMS AFFECTED	DESCRIPTION OF DEVIATIONS
Para. 4.2.1	ESA/SCC No. 21400 (S.E.M. Inspection) may be replaced by MIL-STD-883, Test Method 2018.
Para. 4.2.2	ESA/SCC No. 20400 (Internal Visual Inspection) may be replaced by MIL-STD-883, Test Method 2010, Condition A. ESA/SCC No. 20500 (Physical Dimensions) may be replaced by MIL-STD-2016.
Paras. 4.2.2, 4.2.3, 4.2.4 and 4.2.5	ESA/SCC No. 20500 (External Visual Inspection) may be replaced by MIL-STD-883, Test Method 2009.
Paras. 4.2.4 and 4.2.5	ESA/SCC No. 24800 (Permanence of Marking) may be replaced by MIL-STD-883, Test Method 2015.
	Lot information according to ESA/SCC Generic Specification No. 9000, Para. 10.1 will be on the front page of the data package but not repeated on each page of the documentation.