



**INTEGRATED CIRCUITS, SILICON MONOLITHIC,
CMOS SILICON GATE, STATIC (512x9 BIT)
FIRST IN, FIRST OUT MEMORY
WITH 3-STATE OUTPUTS,
BASED ON TYPE M67201FV
ESCC Detail Specification No. 9301/041**

**ISSUE 1
October 2002**



	ESCC Detail Specification		PAGE ii ISSUE 1
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**space components
coordination group**

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SCC

ESA/SCC Detail Specification
No. 9301/041

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ISSUE 1

DOCUMENTATION CHANGE NOTICE

Rev. Letter	Rev. Date	Reference	CHANGE Item	Approved DCR No.

**SCC**ESA/SCC Detail Specification
No. 9301/041

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**1. GENERAL****1.1 SCOPE**

This specification details the ratings, physical and electrical characteristics, test and inspection data for a silicon, monolithic, CMOS Silicon Gate, Static, (512×9 BIT) First In First Out Memory with 3-State Outputs, based on Type M67201FV. It shall be read in conjunction with ES/SCC Generic Specification No. 9000, the requirements of which are supplemented herein.

1.2 COMPONENT TYPE VARIANTS

Variants of the basic type integrated circuits specified herein, which are also covered by this specification, are given in Table 1(a).

1.3 MAXIMUM RATINGS

The maximum ratings, which shall not be exceeded at any time during use or storage, applicable to the integrated circuits specified herein, are as scheduled in Table 1(b).

1.4 PARAMETER DERATING INFORMATION (FIGURE 1)

Not applicable.

1.5 PHYSICAL DIMENSIONS

As per Figure 2.

1.6 PIN ASSIGNMENT

As per Figure 3(a).

1.7 TRUTH TABLE

As per Figure 3(b).

1.8 CIRCUIT DESCRIPTION

As per Figure 3(c).

1.9 FUNCTIONAL DIAGRAM

As per Figure 3(d).

1.10 HANDLING PRECAUTIONS

These devices are susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacture, testing, packaging, shipment and any handling.

These components are categorised as Class 1 with a Minimum Critical Path Failure Voltage of 1 000 Volts.

1.11 INPUT PROTECTION NETWORK

Double transistor protection shall be incorporated into each input as shown in Figure 3(e).

**TABLE 1(a) - TYPE VARIANTS**

VARIANT	BASED ON TYPE	CASE	FIGURE	LEAD MATERIAL AND/OR FINISH
01	M67201FV-30	D.I.L.	2(a)	G2
02	M67201FV-30	CHIP CARRIER	2(b)	2
03	M67201FV-30	FLAT PACK	2(c)	G2
04	M67201FV-40	D.I.L.	2(a)	G2
05	M67201FV-40	CHIP CARRIER	2(b)	2
06	M67201FV-40	FLAT PACK	2(c)	G2
07	M67201FV-50	D.I.L.	2(a)	G2
08	M67201FV-50	CHIP CARRIER	2(b)	2
09	M67201FV-50	FLAT PACK	2(c)	G2

TABLE 1(b) - MAXIMUM RATINGS

No.	CHARACTERISTICS	SYMBOL	MAXIMUM RATINGS	UNIT	REMARKS
1	Supply Voltage	V_{DD}	-0.3 to +7.0	V	Note 1
2	Input Voltage	V_{IN}	-0.3 to $V_{DD} + 0.3$	V	Note 2 Power On
3	Output Current	$\pm I_{OUT}$	$V_{OUT} = V_{DD}$: +110 $V_{OUT} = V_{SS}$: -60	mA	Note 3
4	Device Dissipation (Continuous)	P_D	825	mW	Per Package
5	Operating Temperature Range	T_{op}	-55 to +125	°C	T_{amb}
6	Storage Temperature Range	T_{stg}	-65 to +150	°C	
7	Soldering Temperature For DIL and FP For CCP	T_{sol}	+265 +245	°C	Note 4 Note 5
8	Thermal Resistance	$R_{TH(J-A)}$	48	°C/W	
9	Junction Temperature	T_J	+165	°C	

NOTES

- Device is functional from +4.5V to +5.5V with reference to Ground.
- $V_{DD} + 0.3V$ should not exceed +7.0V.
- The maximum output current of any single output.
- Duration 10 seconds maximum at a distance of not less than 1.5mm from the device body and the same lead shall not be resoldered until 3 minutes have elapsed.
- Duration 5 seconds maximum and the same terminal shall not be resoldered until 3 minutes have elapsed.

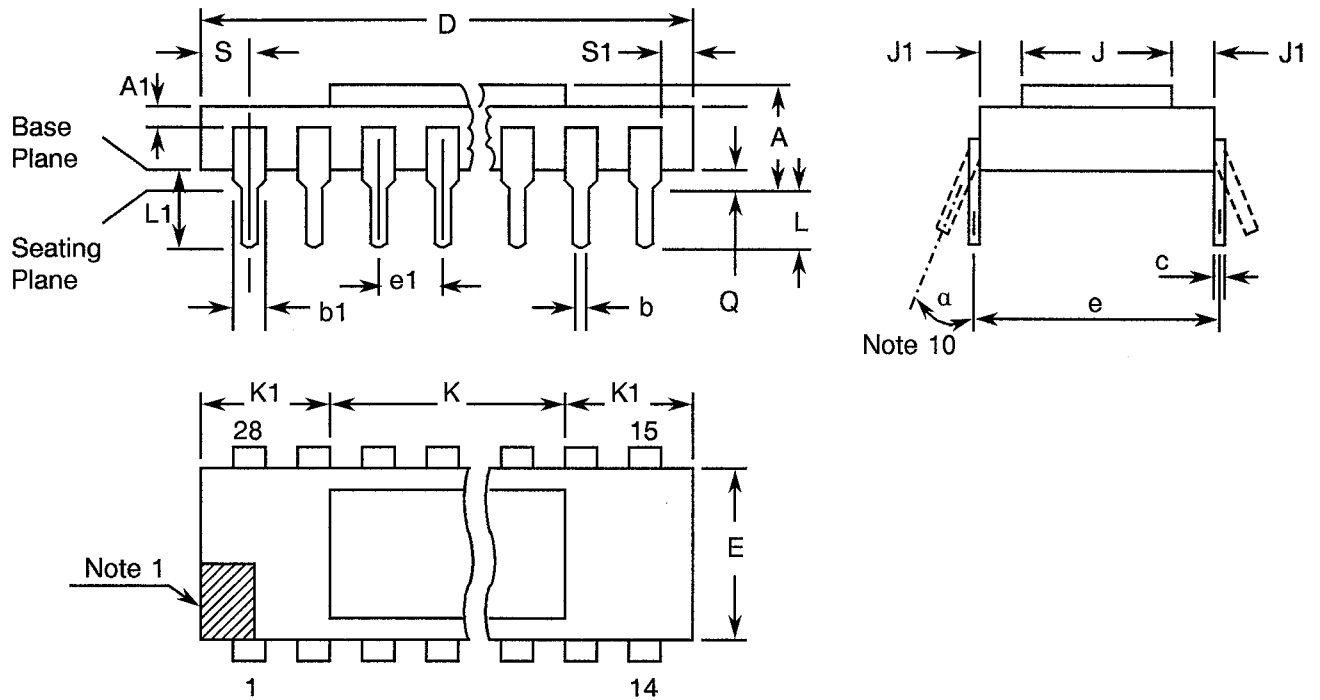
FIGURE 1 - PARAMETER DERATING INFORMATION

Not applicable.



FIGURE 2 - PHYSICAL DIMENSIONS

FIGURE 2(a) - DUAL-IN-LINE PACKAGE, 28-PIN



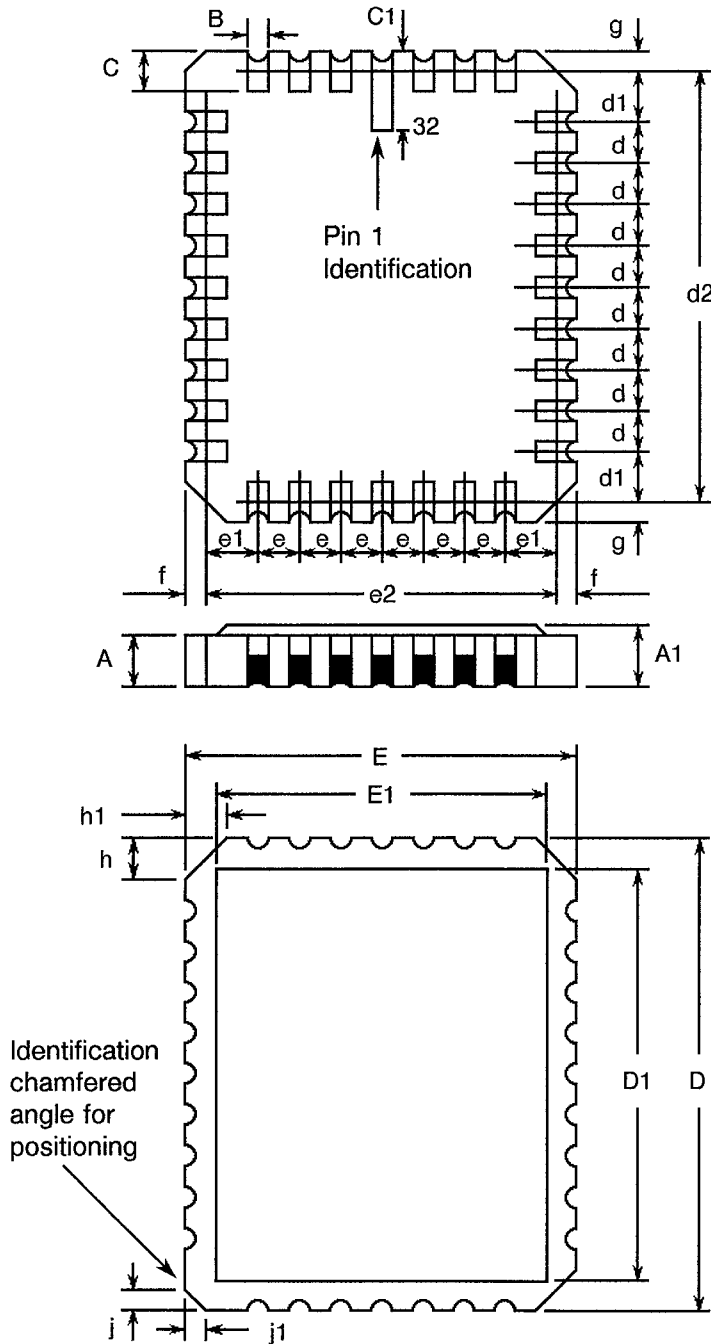
SYMBOL	MILLIMETERS		NOTES
	MIN.	MAX.	
A	3.30	5.84	-
A1	0.13	-	-
b	0.36	0.58	8
b1	0.96	1.65	8
c	0.20	0.38	8
D	-	37.72	-
E	6.10	7.87	4
e	7.37	8.13	-
e1	2.54 TYPICAL		6,9
J	6.85 TYPICAL		-
J1	0.31 TYPICAL		-
K	11.43 TYPICAL		-
K1	12.06 TYPICAL		-
L	2.92	5.08	8
L1	3.30	-	8
S	-	2.54	7
S1	0.13	-	7
Q	0.38	2.54	3
alpha	0°	15°	10

NOTES: See Page 10.



FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)

FIGURE 2(b) - CHIP CARRIER PACKAGE, 32-TERMINAL



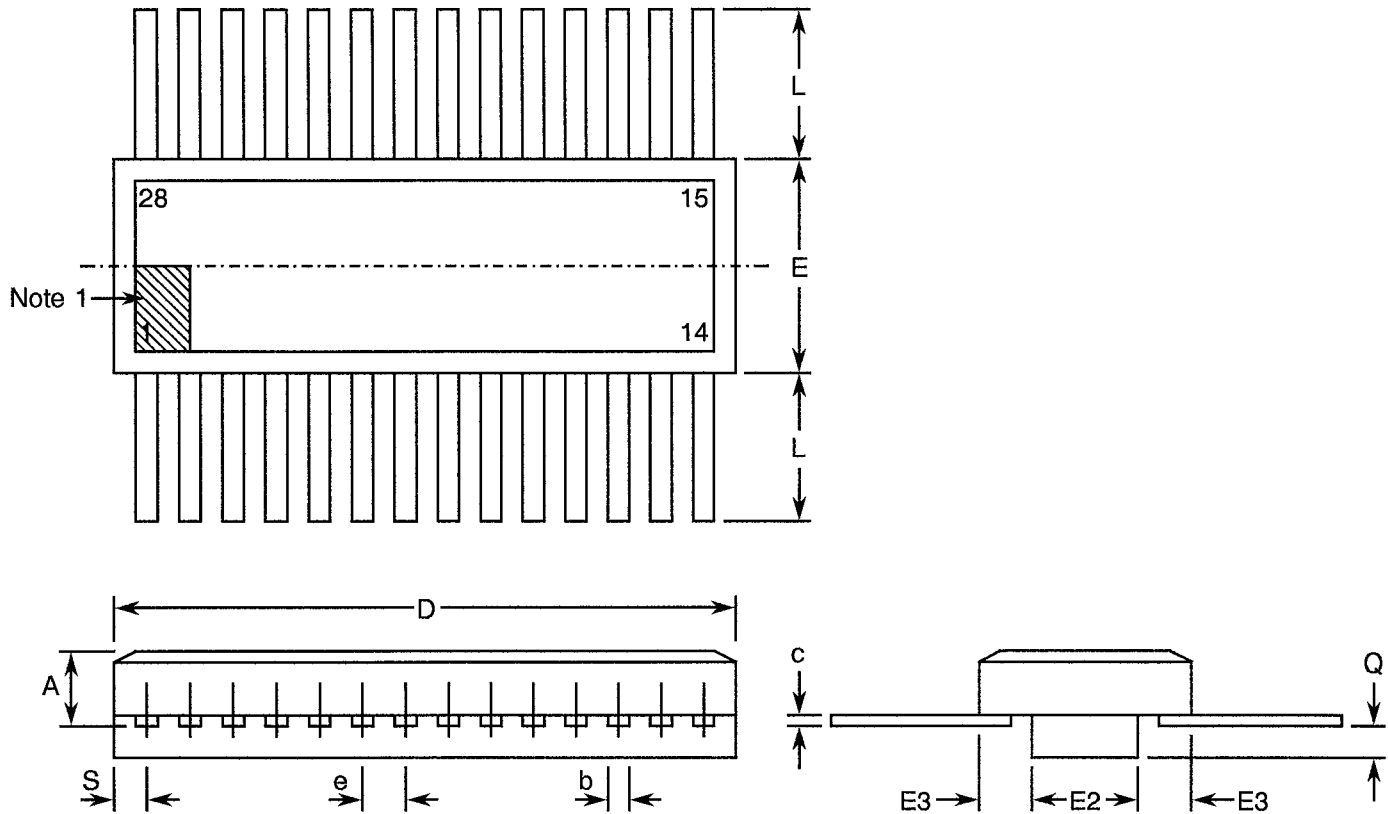
SYMBOL	MILLIMETRES		NOTES
	MIN	MAX	
A	1.37	1.93	-
A1	1.62	2.23	-
B	0.635 TYPICAL		8
C	0.99	1.30	8
C1	1.95	2.36	-
D	13.81	14.22	-
D1	10.41 TYPICAL		-
d	1.27 TYPICAL		5, 9
d1	1.71	1.97	-
d2	12.70 TYPICAL		-
E	11.30	11.63	-
E1	12.95 TYPICAL		-
e	1.27 TYPICAL		5, 9
e1	1.27 TYPICAL		-
e2	10.16 TYPICAL		-
f, g	0.63 TYPICAL		-
h, h1	1.016 TYPICAL		11
j, j1	0.51 TYPICAL		12

NOTES: See Page 10.



FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)

FIGURE 2(c) - FLAT PACKAGE, 28-PIN



SYMBOL	MILLIMETRES		NOTES
	MIN.	MAX.	
A	2.29	3.30	-
b	0.38	0.48	8
c	0.08	0.15	8
D	-	18.80	-
E	9.65	10.67	-
E2	4.57	-	-
E3	0.76	-	-
e	1.27 TYPICAL		5, 9
L	6.35	9.40	8
Q	0.66	-	2
S	-	1.30	7

NOTES: See Page 10.



FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)

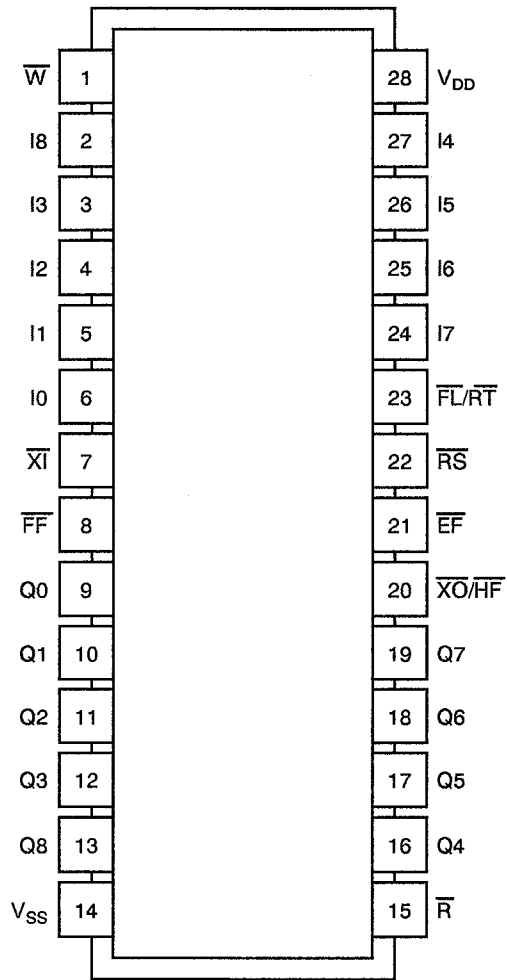
NOTES TO FIGURES 2(a) TO 2(c) INCLUSIVE

1. Index area: a notch, letter or dot shall be located adjacent to Pin 1 and shall be within the shaded area shown. For chip carrier packages the index shall be as defined in Figure 2(b).
2. Dimension Q shall be measured at the point of exit of the lead from the body.
3. The dimension shall be measured from the seating plane to the base plane.
4. The dimension allows for off-centre lids, meniscus and glass overrun.
5. The true position pin or terminal spacing is 1.27mm between centrelines. Each pin or terminal centreline shall be located within 0.13mm of its true longitudinal position relative to Pin 1 and the highest pin number.
6. The true position pin spacing is 2.54mm between centrelines. Each pin centreline shall be located within 0.25mm of its true longitudinal position relative to Pin 1 and the highest pin number.
7. Applies to all 4 corners.
8. All leads or terminals.
9. 26 spaces for dual-in-line and flat packages.
28 spaces for chip carrier packages.
10. Lead centre when α is 0° .
11. 3 non-index corners - 6 dimensions.
12. Index corner only - 2 dimensions.



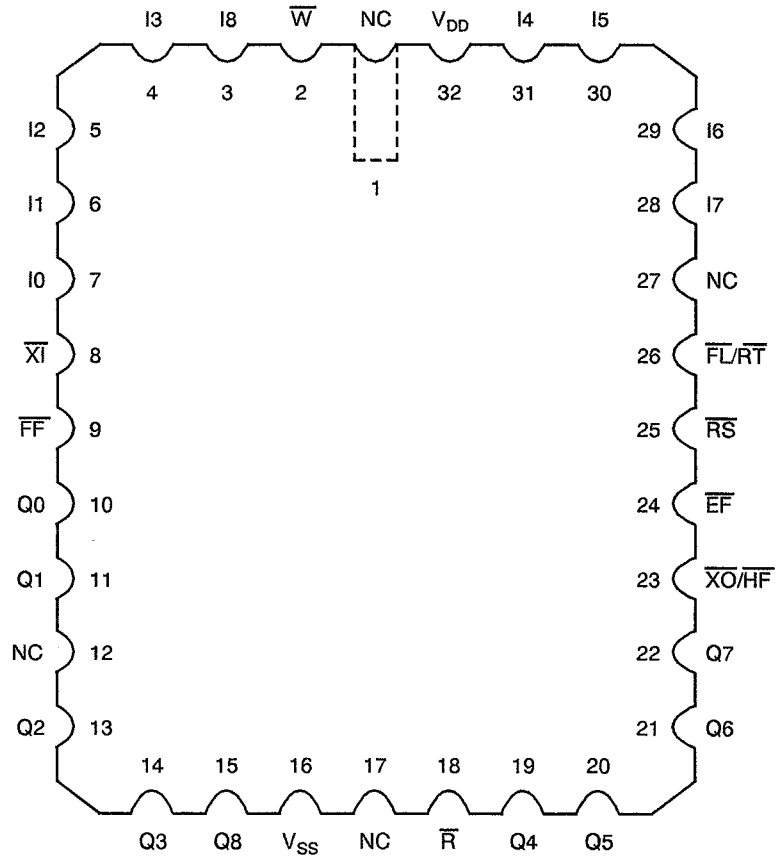
FIGURE 3(a) - PIN ASSIGNMENT

DUAL-IN-LINE AND FLAT PACKAGE



TOP VIEW

CHIP CARRIER PACKAGE



TOP VIEW

NOTES

1. I0 to I8 = Data Inputs.
2. Q0 to Q8 = Data Outputs.
3. \overline{W} = Write Enable.
4. \overline{R} = Read Enable.
5. \overline{RS} = Reset.
6. \overline{EF} = Empty Flag.
7. \overline{FF} = Full Flag.
8. $\overline{XO/HF}$ = Expansion Out/Half Full Flag.
9. \overline{XI} = Expansion In.
10. $\overline{FL/RT}$ = First Load/Retransmit.

FLAT PACKAGE AND DUAL-IN-LINE TO CHIP CARRIER PIN ASSIGNMENT

FLAT PACKAGE AND

DUAL-IN-LINE PIN OUTS 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28

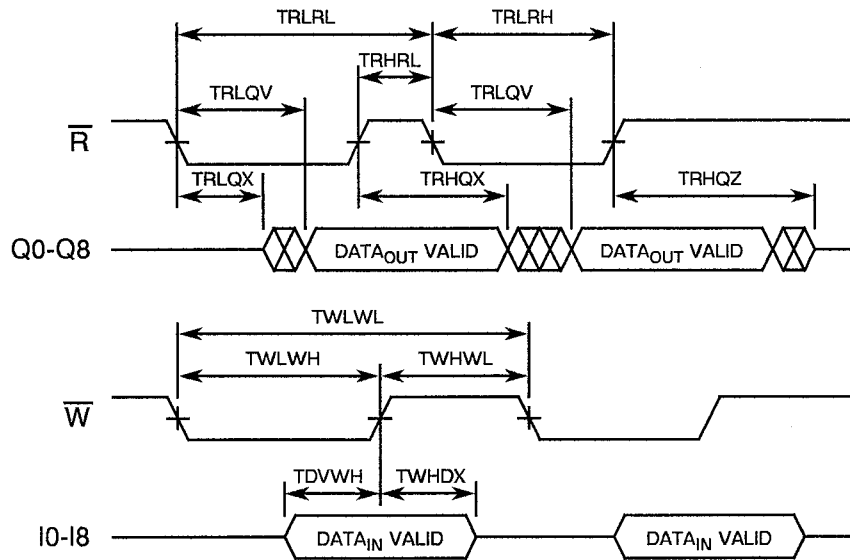
CHIP CARRIER PIN OUTS 2 3 4 5 6 7 8 9 10 11 13 14 15 16 18 19 20 21 22 23 24 25 26 28 29 30 31 32



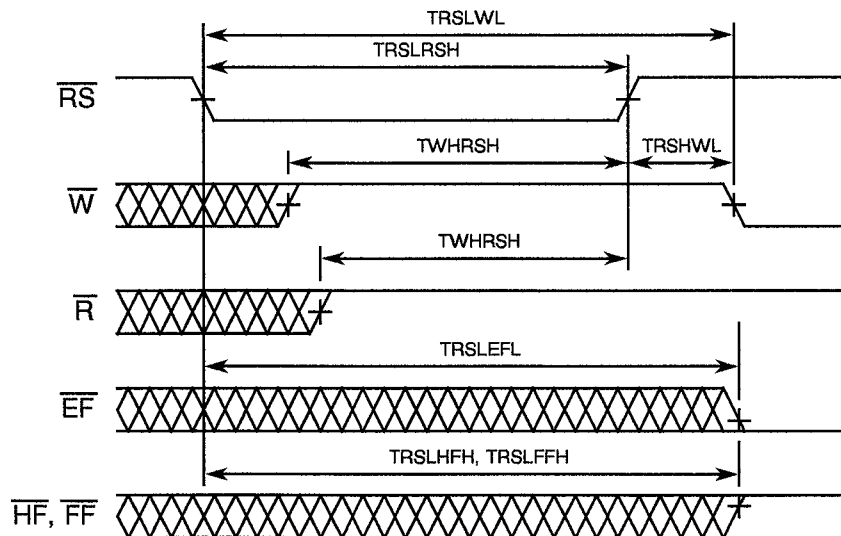
FIGURE 3(b) - TRUTH TABLE

TIMING WAVEFORMS

ASYNCHRONOUS WRITE AND READ OPERATION



RESET TIMING



NOTES

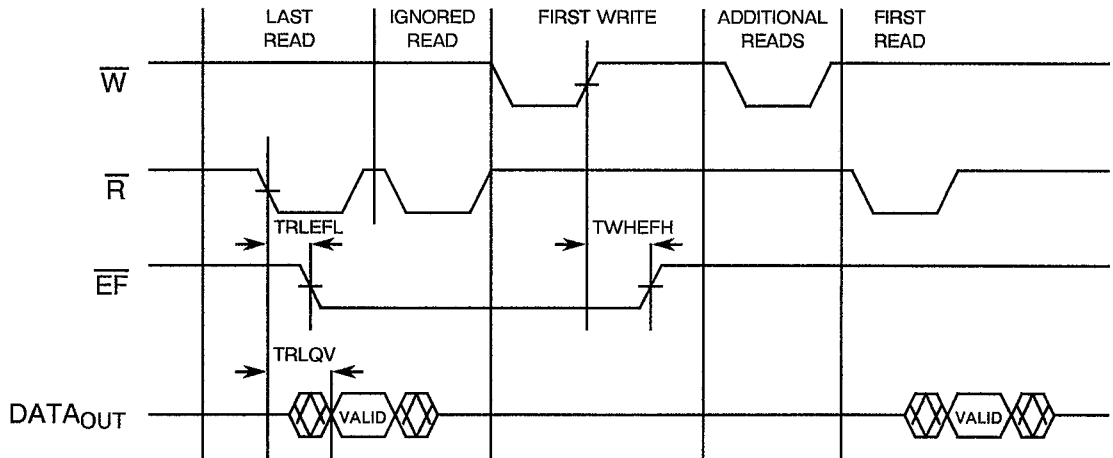
1. \overline{EF} , \overline{HF} and \overline{FF} may change status during Reset, but flags will be valid at TRSLWL.
2. \overline{W} and $\overline{R} = V_{IH}$ around the rising edge of \overline{RS} .



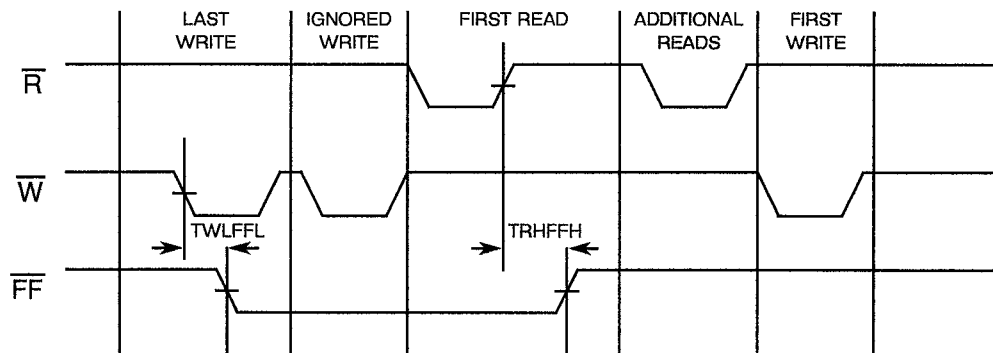
FIGURE 3(b) - TRUTH TABLE (CONTINUED)

TIMING WAVEFORMS (CONTINUED)

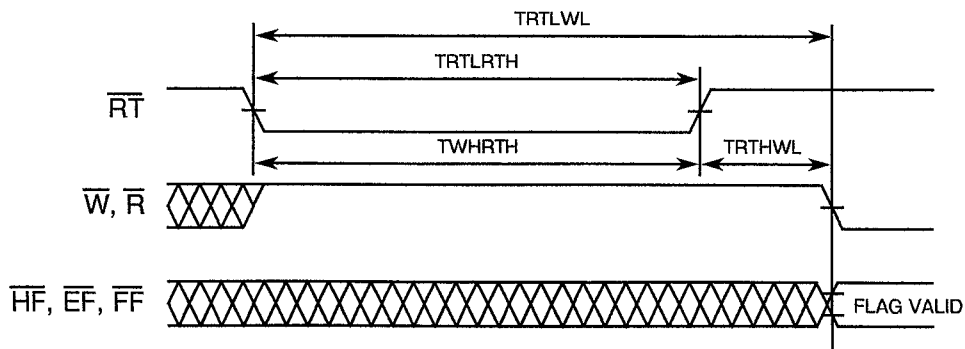
EMPTY FLAG FROM LAST READ TO FIRST WRITE



FULL FLAG FROM LAST WRITE TO FIRST READ



RETRANSMIT



NOTES

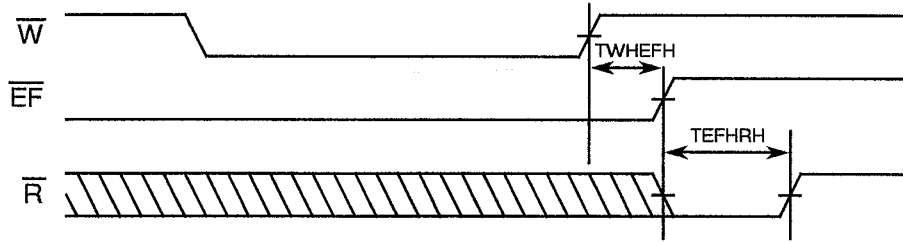
1. \overline{EF} , \overline{FF} and \overline{HF} may change status during Retransmit, but flags will be valid at TRTLWL.



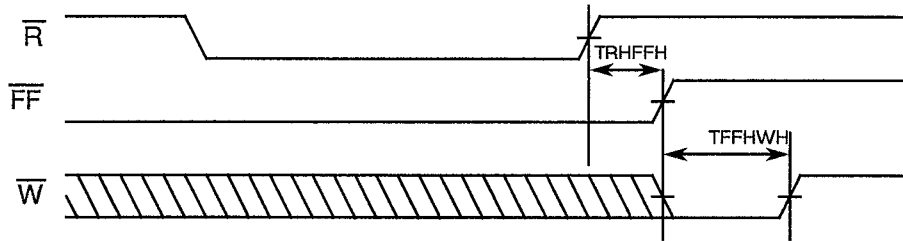
FIGURE 3(b) - TRUTH TABLE (CONTINUED)

TIMING WAVEFORMS (CONTINUED)

EMPTY FLAG TIMING



FULL FLAG TIMING



HALF-FULL FLAG TIMING

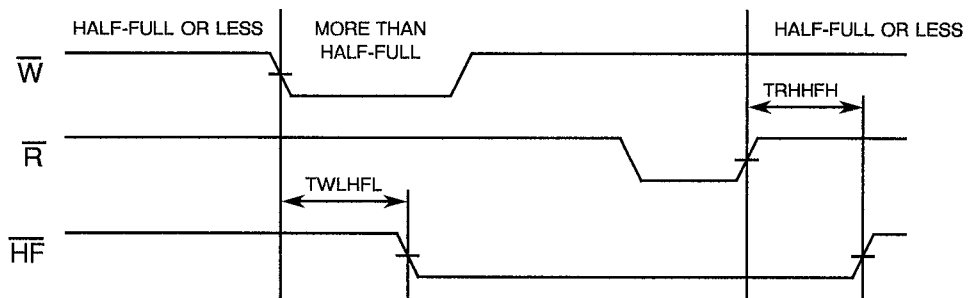
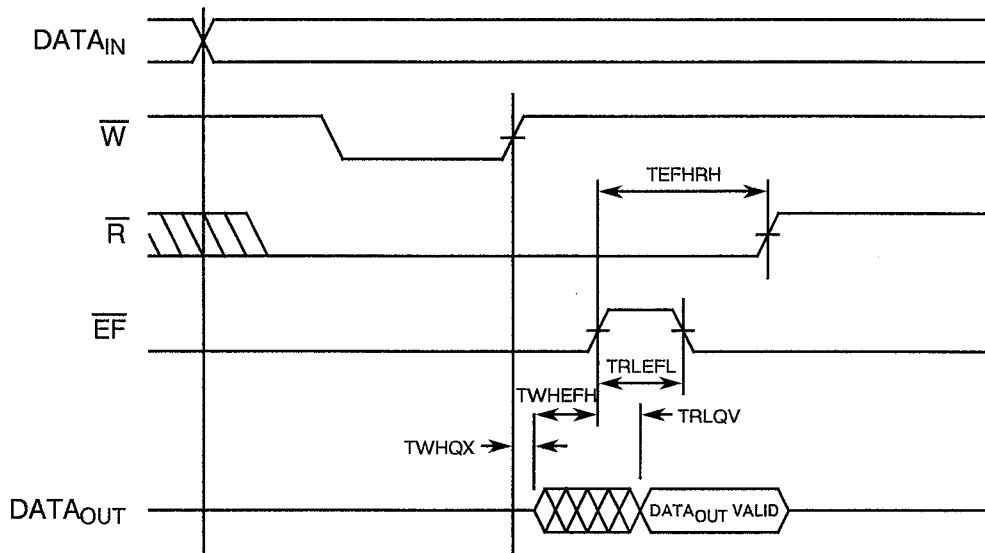




FIGURE 3(b) - TRUTH TABLE (CONTINUED)

TIMING WAVEFORMS (CONTINUED)

READ DATA FLOW - THROUGH MODE



WRITE DATA FLOW - THROUGH MODE

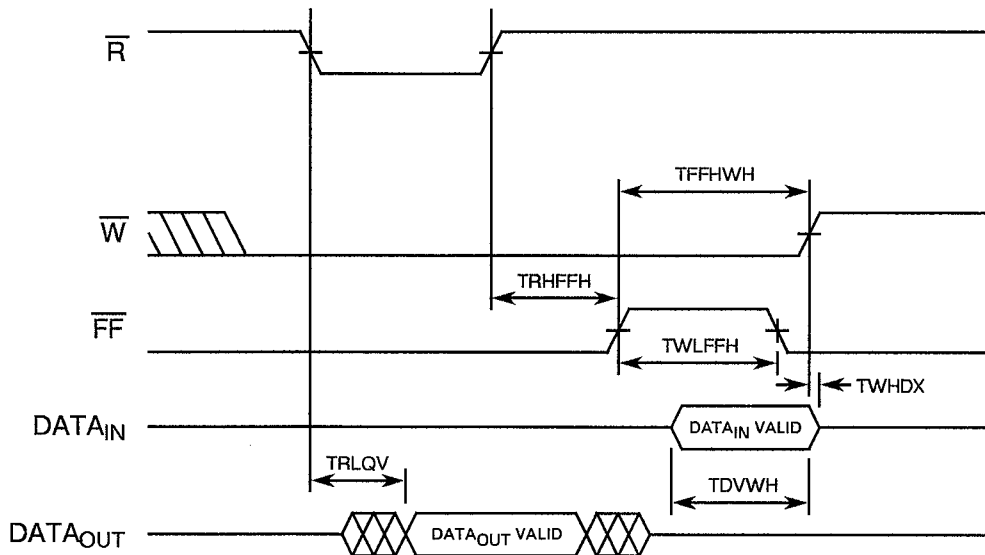
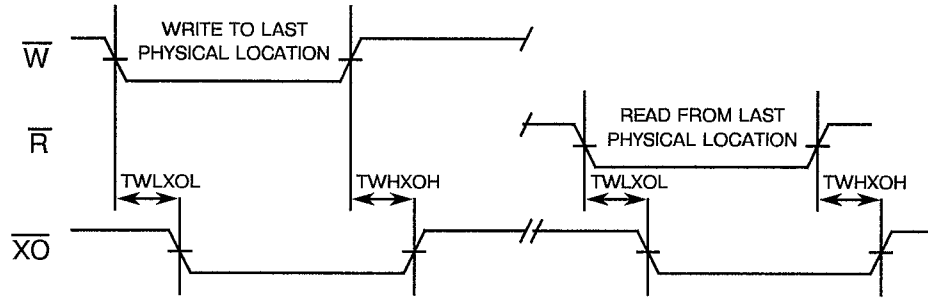




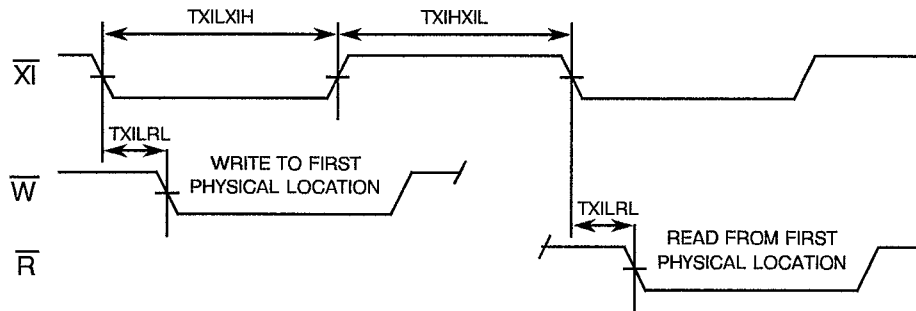
FIGURE 3(b) - TRUTH TABLE (CONTINUED)

TIMING WAVEFORMS (CONTINUED)

EXPANSION OUT



EXPANSION IN



**FIGURE 3(c) - CIRCUIT DESCRIPTION****CONTROLS****RESET (\overline{RS})**

Reset occurs whenever the Reset (\overline{RS}) input is taken to a low state. Reset returns both internal read and write pointers to the first location. A reset is required after power-up before a write operation can be enabled. Both the Read Enable (\overline{R}) and Write Enable (\overline{W}) inputs must be in the high state during the period shown in the reset waveforms (i.e. TWHRSH before the rising edge of \overline{RS}) and should not change until TRSHWL after the rise time of the leading edge of \overline{RS} . The Half-Full flag (\overline{HF}) will be reset to high after Reset (\overline{RS}).

WRITE ENABLE (\overline{W})

A write cycle is initiated on the trailing edge of this input if the Full Flag (\overline{FF}) is not set. Data set-up and hold times must be maintained in the rise time of the leading edge of the Write Enable (\overline{W}). Data is stored sequentially in the Ram array, independently of any current read operation.

Once half the memory is filled, and during the trailing edge of the next write operation, the Half-Full Flag (\overline{HF}) will be set to low and remain in this state until the difference between the write and read pointers is less than or equal to half the total available memory in the device. The Half-Full Flag (\overline{HF}) is then reset by the leading edge of the read operation.

To prevent data overflow, the Full Flag (\overline{FF}) will go low, inhibiting further write operations. On completion of a valid read operation, the Full Flag (\overline{FF}) will go high after TRHFFH, allowing a valid write to begin. When the FIFO stack is full, the internal write pointer is blocked from \overline{W} , so that external changes to \overline{W} will have no effect on the full FIFO stack.

READ ENABLE (\overline{R})

A read cycle is initiated on the trailing edge of the Read Enable (\overline{R}) provided that the Empty Flag (\overline{EF}) is not set. The data is accessed on a first in/first out basis, notwithstanding any current write operations. After Read Enable (\overline{R}) goes high, the Data Outputs (Q0 - Q8) will return to a high impedance state until the next Read operation. When all of the data in the FIFO stack has been read, the Empty Flag (\overline{EF}) will go low, allowing the "final" read cycle, but inhibiting further read operations whilst the data outputs remain in a high impedance state. Once a valid write operation has been completed, the Empty Flag (\overline{EF}) will go high after TWHEFH and a valid read may then be initiated. When the FIFO stack is empty, the internal read pointer is blocked from \overline{R} , so that external changes to \overline{R} will have no effect on the empty FIFO stack.

FIRST LOAD/RETRANSMIT ($\overline{FL/RT}$)

This is a dual-purpose input. In the Depth Expansion Mode, this pin is connected to Ground to indicate that it is the first loaded (see Operating Modes). In the Single Device Mode, this pin acts as the retransmit input. The Single Device Mode is initiated by connecting the Expansion In (\overline{XI}) to Ground.

The M67201 can be made to retransmit data when the Retransmit Enable Control (\overline{RT}) input is pulsed low. A retransmit operation will set the internal read pointer to the first location and will not affect the write pointer. Read Enable (\overline{R}) and Write Enable (\overline{W}) must be in the high state during retransmit. This feature is useful if fewer than 512 writes are performed between resets. The retransmit feature is not compatible with the Depth Expansion Mode and will affect the Half-Full Flag (\overline{HF}), in accordance with the relative locations of the read and write pointers.

EXPANSION IN (\overline{XI})

This input is a dual-purpose pin. Expansion In (\overline{XI}) is connected to Ground to indicate an operation in the single device mode. Expansion In (\overline{XI}) is connected to Expansion Out (\overline{XO}) of the previous device in the Depth Expansion or Daisy Chain modes.



FIGURE 3(c) - CIRCUIT DESCRIPTION (CONTINUED)

OUTPUTS

FULL FLAG (\overline{FF})

The Full Flag (\overline{FF}) will go low, inhibiting further write operations when the write pointer is one location less than the read pointer, indicating that the device is full. If the read pointer is not moved after Reset (\overline{RS}), the Full Flag (\overline{FF}) will go low after 512 writes.

EMPTY FLAG (\overline{EF})

The Empty Flag (\overline{EF}) will go low, inhibiting further read operations when the read pointer is equal to the write pointer, indicating that the device is empty.

EXPANSION OUT/HALF-FULL FLAG ($\overline{XO}/\overline{HF}$)

This is a dual-purpose output. In the single device mode, when Expansion In (\overline{XI}) is connected to Ground, this output acts as an indication of a half-full memory.

After half the memory is filled, and on the trailing edge of the next write operation, the Half-Full Flag (\overline{HF}) will be set to low and will remain set until the difference between the write and read pointers is less than or equal to half of the total memory of the device. The Half-Full Flag (\overline{HF}) is then reset by the leading edge of the read operation.

In the Depth Expansion Mode, Expansion In (\overline{XI}) is connected to Expansion Out (\overline{XO}) of the previous device. This output acts as a signal to the next device in the Daisy Chain by providing a pulse to the next device when the previous device reaches the last memory location.

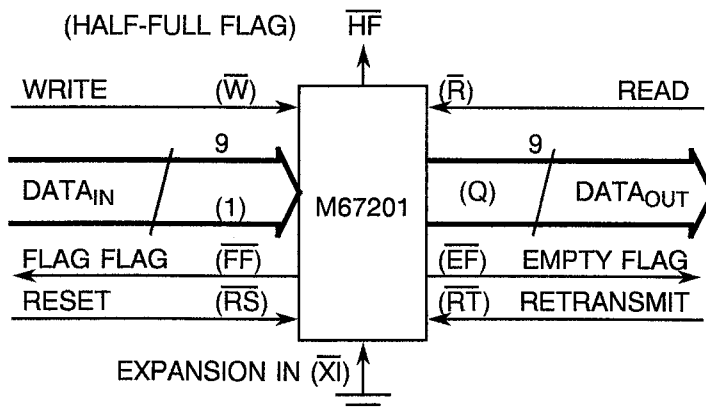
DATA OUTPUT (Q0 - Q8)

DATA output for 9-bit wide data. This data is in a high impedance condition whenever Read (\overline{R}) is in a high state.

OPERATING MODES

SINGLE DEVICE MODE

A single M67201 may be used when the application requirements are for 512 words or less. The M67201 is in a Single Device Configuration when the Expansion In (\overline{XI}) control input is Grounded. In this mode the Half-Full Flag (\overline{HF}), which is an active low output, is shared with Expansion Out (\overline{XO}).



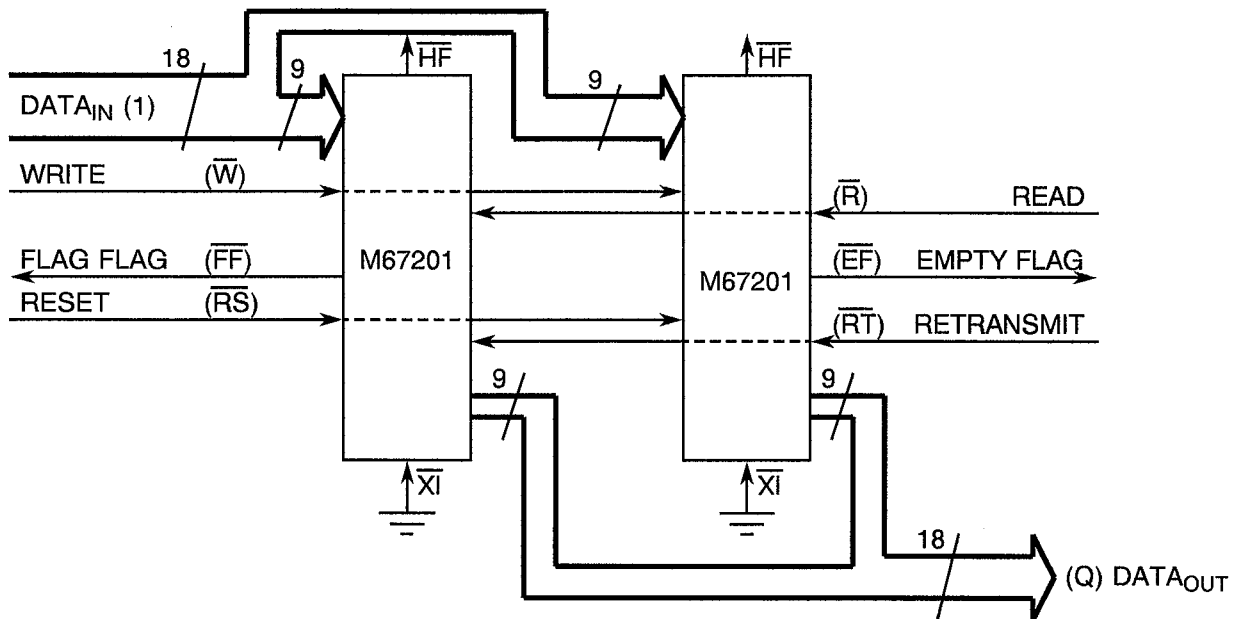
BLOCK DIAGRAM OF SINGLE 512x9 FIFO



FIGURE 3(c) - CIRCUIT DESCRIPTION (CONTINUED)

WIDTH EXPANSION MODE

Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Status flags (\overline{EF} , \overline{FF} and \overline{HF}) can be detected from any one device. The figure demonstrates an 18-bit word width by using $2 \times$ M67201s. Any word width can be attained by adding additional M67201s.



NOTES

1. Flag detection is accomplished by monitoring the \overline{FF} , \overline{EF} and \overline{HF} signals on either (any) device used in the width expansion configuration.
2. Do not connect any output control signals together

BLOCK DIAGRAM OF 512 x 18 FIFO MEMORY USED IN WIDTH EXPANSION MODE



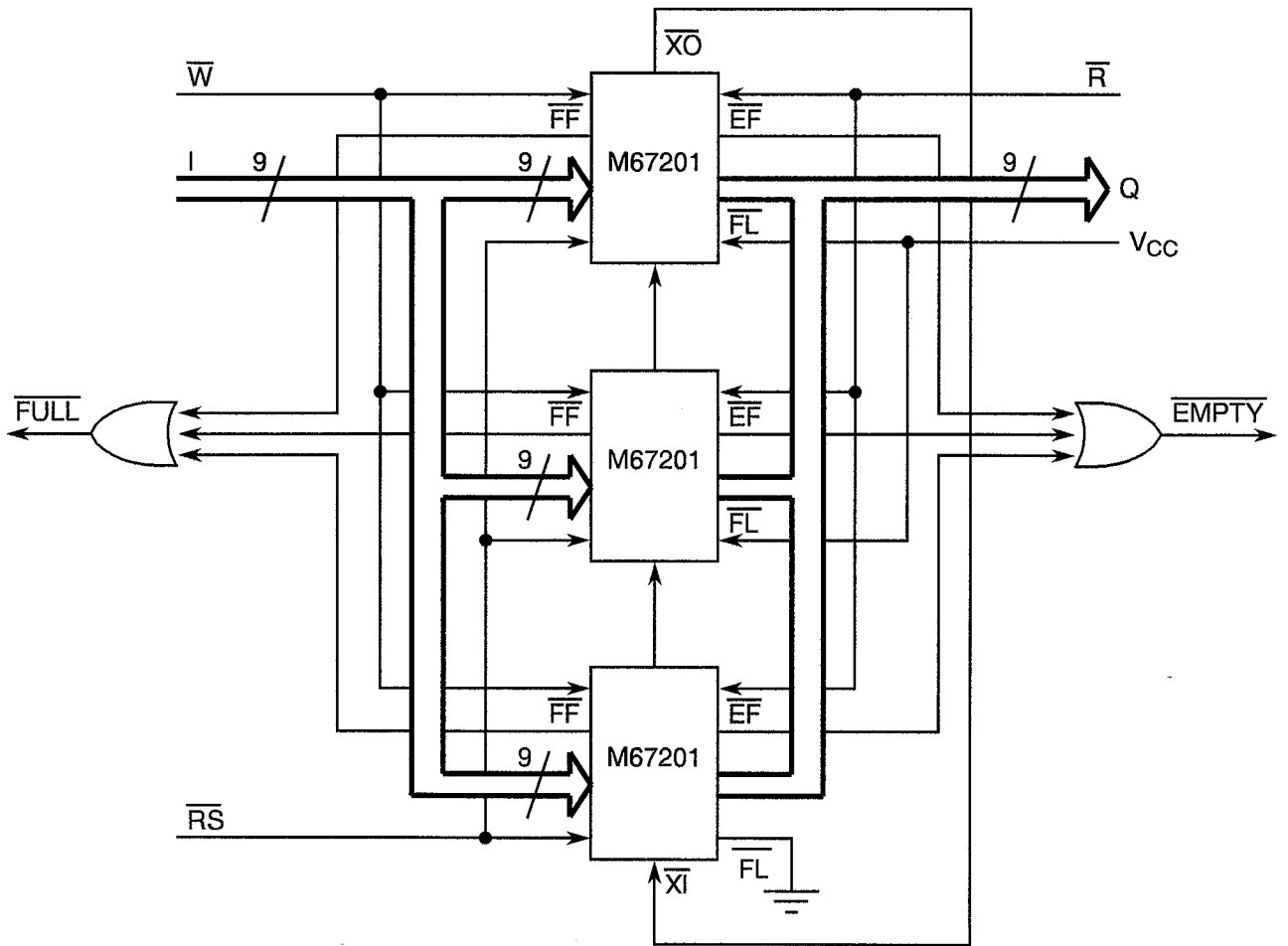
FIGURE 3(c) - CIRCUIT DESCRIPTION (CONTINUED)

DEPTH EXPANSION (DAISY CHAIN) MODE

The M67201 can be easily adapted for applications which require more than 512 words. The figure demonstrates Depth Expansion using 3 × M67201s. Any depth can be achieved by adding additional M67201s.

The M67201s operate in the Depth Expansion configuration if the following conditions are met:-

1. The first device must be designated by connecting the First Load (\overline{FL}) control input to Ground.
2. All other devices must have \overline{FL} in the high state.
3. The Expansion Out (\overline{XO}) pin of each device must be connected to the Expansion In (\overline{XI}) pin of the next device.
4. External logic is needed to generate a composite Full Flag (\overline{FF}) and Empty Flag (\overline{EF}). This requires that all \overline{EF} s and all \overline{FF} s be \emptyset Red (i.e. all must be set to generate the correct composite \overline{FF} or \overline{EF}).
5. The Retransmit (\overline{RT}) function and Half-Full Flag (\overline{HF}) are not available in the Depth Expansion Mode.



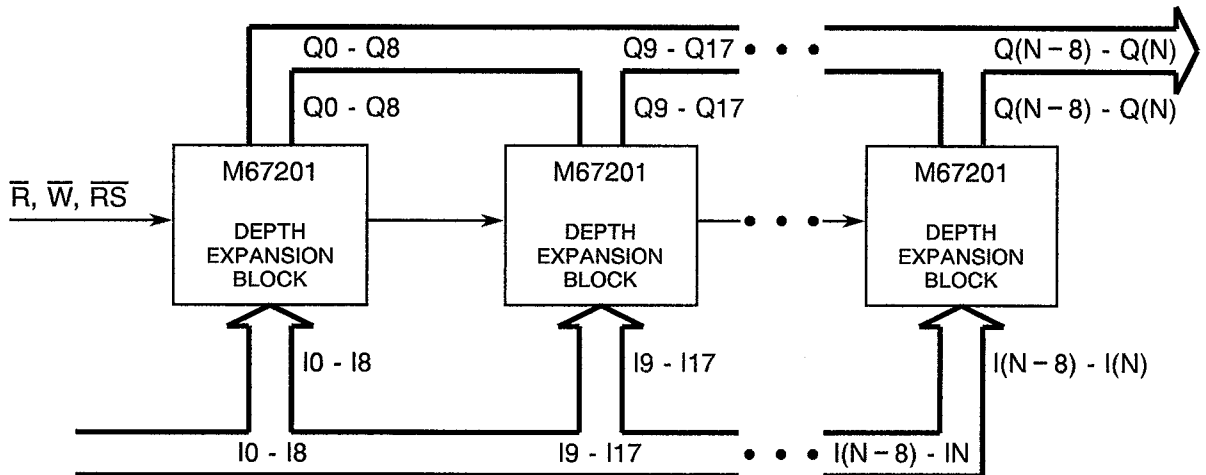
BLOCK DIAGRAM OF 1536 x 9 FIFO MEMORY (DEPTH EXPANSION)



FIGURE 3(c) - CIRCUIT DESCRIPTION (CONTINUED)

COMPOUND EXPANSION MODULE

It is quite simple to apply the 2 expansion techniques described above together to create large FIFO arrays.



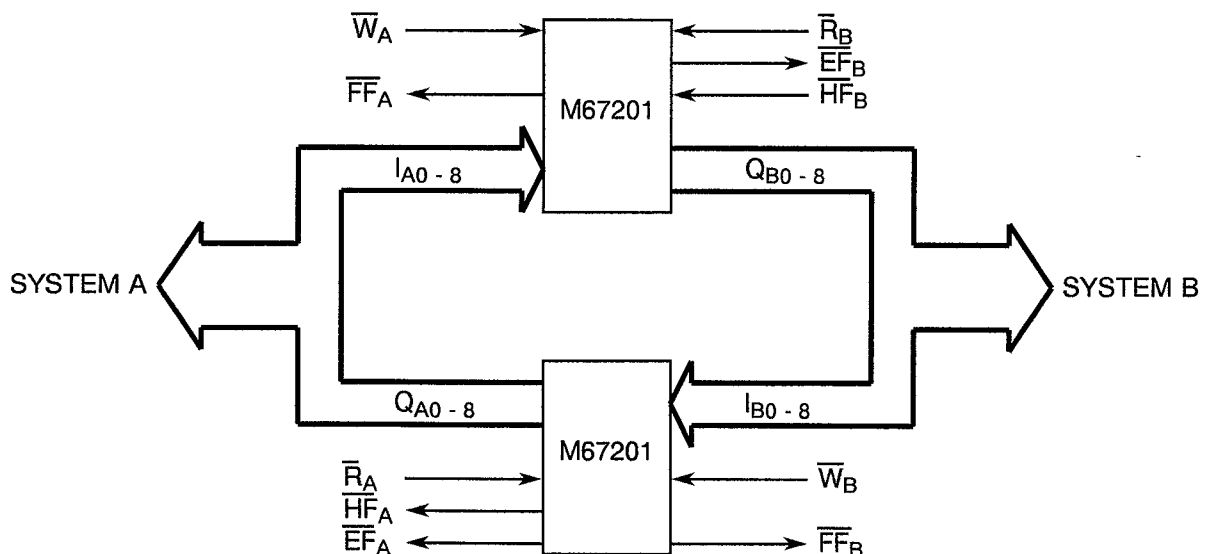
NOTES

1. For depth expansion block, see section on Depth Expansion.
2. For Flag detection, see section on Width Expansion.

COMPOUND FIFO EXPANSION

BI-DIRECTIONAL MODE

Applications which require data buffering between two systems (each system being capable of Read and Write operations) can be created by coupling M67201s. Care must be taken to ensure that the appropriate flag is monitored by each system (i.e. FF is monitored on the device on which W-bar is in use; EF is monitored on the device on which R-bar is in use). Both Depth Expansion and Width Expansion may be used in this mode.



BI-DIRECTIONAL FIFO MODE

**FIGURE 3(c) - CIRCUIT DESCRIPTION (CONTINUED)****DATA FLOW-THROUGH MODES**

2 types of flow-through modes are permitted: a read flow-through and a write flow-through mode.

In the read flow-through mode, the FIFO stack allows a single word to be read after 1 word has been written to an empty FIFO stack. The data is enabled on the bus at (TWHEFH + TRLQV) ns after the leading edge of \overline{W} , which is known as the first write edge and remains on the bus until the \overline{R} line is raised from low to high, after which the bus will go into a 3-State mode after TRHQZ ns. The \overline{EF} line will show a pulse indicating temporary reset and then will be set. In the interval in which \overline{R} is low, more words may be written to the FIFO stack (the subsequent writes after the first write edge will reset the Empty Flag); however, the same word (written on the first write edge) presented to the output bus as the read pointer will not be incremented if \overline{R} is low. On toggling \overline{R} , the remaining words written to the FIFO will appear on the output bus in accordance with the read cycle timings.

In the write flow-through mode, the FIFO stack allows a single word of data to be written immediately a single word of data has been read from a full FIFO stack. The \overline{R} line causes the \overline{FF} to be reset, but the \overline{W} line, being low, causes it to be set again in anticipation of a new data word. The new word is loaded into the FIFO stack on the leading edge of \overline{W} . The \overline{W} line must be toggled when \overline{FF} is not set in order to write new data into the FIFO stack and to increment the write pointer.

A - RESET AND RETRANSMIT**SINGLE DEVICE CONFIGURATION/WIDTH EXPANSION MODE**

MODE	INPUTS			INTERNAL STATUS		OUTPUTS		
	\overline{RS}	\overline{RT}	\overline{XI}	READ POINTER	WRITE POINTER	\overline{EF}	\overline{FF}	\overline{HF}
Reset	L	X	L	Location Zero	Location Zero	L	H	H
Retransmit	H	L	L	Location Zero	Unchanged	X	X	X
Read/Write	H	H	L	Increment (2)	Increment (2)	X	X	X

B - RESET AND FIRST LOAD**DEPTH EXPANSION/COMPOUND EXPANSION MODE**

MODE	INPUTS			INTERNAL STATUS		OUTPUTS	
	\overline{RS}	\overline{FL}	\overline{XI}	READ POINTER	WRITE POINTER	\overline{EF}	\overline{FF}
Reset first device	L	L	(3)	Location Zero	Location Zero	L	H
Reset all other devices	L	H	(3)	Location Zero	Location Zero	L	H
Read/Write	H	X	(3)	X	X	X	X

NOTES

- Logic Level Definitions: L = Low Level, H = High Level, X = Don't Care.
- Pointer will increment if flag is high.
- \overline{XI} is connected to \overline{XO} of previous device.
 \overline{RS} = Reset Input
 $\overline{FL}/\overline{RT}$ = first load/retransmit.
 \overline{EF} = Empty flag output.
 \overline{FF} = Full flag output.
 \overline{XI} = Expansion input.
 \overline{HF} = Half-full flag output.



FIGURE 3(d) - FUNCTIONAL DIAGRAM

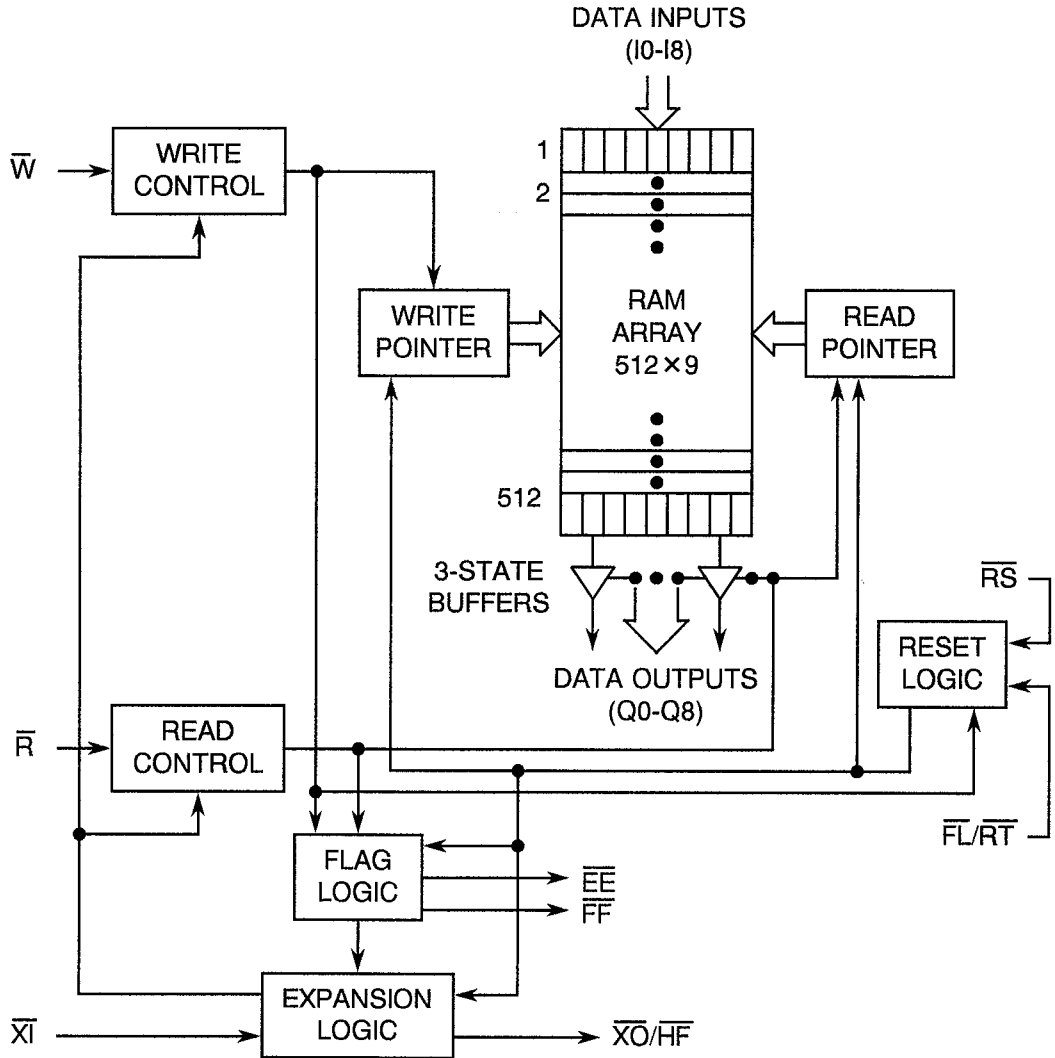
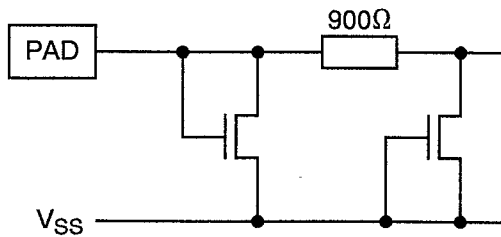
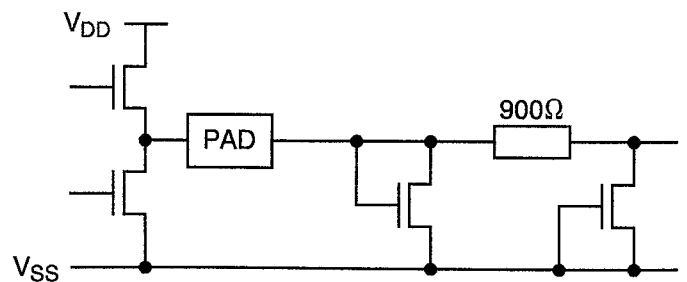


FIGURE 3(e) - INPUT/OUTPUT PROTECTION NETWORKS

EQUIVALENT OF EACH INPUT



EQUIVALENT OF EACH OUTPUT



**2. APPLICABLE DOCUMENTS**

The following documents form part of this specification and shall be read in conjunction with it:-

- (a) ESA/SCC Generic Specification No. 9000 for Integrated Circuits.
- (b) MIL-STD-883, Test Methods and Procedures for Micro-electronics.

3. TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESA/SCC Basic Specification No. 21300 shall apply. In addition, the following abbreviations are used:

V_{IC}	=	Input Clamp Voltage.
I_{DD1}	=	Average Power Supply Current.
I_{DD2}	=	Average Standby Current.
I_{DD3}	=	Power Down Current.
I_{OZH}	=	Output Leakage Current Third State (High Level Applied).
I_{OZL}	=	Output Leakage Current Third State (Low Level Applied).
C_{IN}	=	Input Capacitance.
C_{OUT}	=	Output Capacitance.
TRLRL	=	Read Cycle Time.
TRLQV	=	Access Time.
TRHRL	=	Read Recovery Time.
TRLRH	=	Read Pulse Width.
TRHQX	=	Data Valid from Read Pulse High.
TWLWL	=	Write Cycle Time.
TWLWH	=	Write Pulse Width.
TWHWL	=	Write Recovery Time.
TDVWH	=	Data Set-up Time.
TWHDX	=	Data Hold Time.
TRSLWL	=	Reset Cycle Time.
TRSLRSH	=	Reset Pulse Width.
TRSHWL	=	Reset Recovery Time.
TRTLWL	=	Retransmit Cycle Time.
TRTLRTH	=	Retransmit Pulse Width.
TRTHWL	=	Retransmit Recovery Time.
TRSLEFL	=	Reset to Empty Flag Low.
TRLEFL	=	Read Low to Empty Flag Low.
TRHFFH	=	Read High to Full Flag High.
TWHEFH	=	Write High to Empty Flag High.
TWLFFL	=	Write Low to Full Flag Low.
TRLQX	=	Read Pulse Low to Data Bus Low Impedance.
TWHQX	=	Write Pulse Low to Data Bus Low Impedance.
TRHQZ	=	Read Pulse High to Data Bus High Impedance.
TWHRSH	=	Reset Set-up Time.
TWHRTH	=	Retransmit Set-up Time.
TRSLHFH	=	Reset to Half Full Flag High.
TRSLFFH	=	Reset to Full Flag High.
TEFHRH	=	Read Pulse Width after EF High.
TWLHFL	=	Write High to Half Flag Low.
TRHFFH	=	Read High to Half Flag High.
TFHWH	=	Write Pulse Width after FF High.
TWLXOL	=	Read/Write to XO Low.
TWHXOH	=	Read/Write to XO High.
TXILXH	=	XI Pulse Width.
TXHXIL	=	XI Recovery Time.
TXILRL	=	XI Set-up Time.



4. REQUIREMENTS

4.1 GENERAL

The complete requirements for procurement of the integrated circuits specified herein are stated in this specification and ESA/SCC Generic Specification No. 9000 for Integrated Circuits. Deviations from the Generic Specification applicable to this specification only, are listed in Para. 4.2.

Deviations from the applicable Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESA/SCC requirements and do not affect the components' reliability, are listed in the appendices attached to this specification.

4.2 DEVIATIONS FROM GENERIC SPECIFICATION

4.2.1 Deviations from Special In-process Controls

- (a) Para. 5.2.2, Total Dose Irradiation Testing: Shall be performed during qualification and extension of qualification.
- (b) Para. 5.2.2, Total Dose Irradiation Testing: Shall be performed during procurement on a lot acceptance basis at the total dose irradiation level specified in the Purchase Order.

4.2.2 Deviations from Final Production Tests (Chart II)

None.

4.2.3 Deviations from Burn-in Tests (Chart III)

- (a) Para. 7.1.1(a), "High Temperature Reverse Bias" test and subsequent electrical measurements related to this test shall be omitted.

4.2.4 Deviations from Qualification Tests (Chart IV)

None.

4.2.5 Deviations from Lot Acceptance Tests (Chart V)

None.

4.3 MECHANICAL REQUIREMENTS

4.3.1 Dimension Check

The dimensions of the integrated circuits specified herein shall be checked. They shall conform to those shown in Figure 2.

4.3.2 Weight

The maximum weight of the integrated circuits specified herein shall be 3.5 grammes for the dual-in-line package, 2.0 grammes for the chip carrier package and 2.5 grammes for the flat package.



4.4 MATERIALS AND FINISHES

The materials shall be as specified herein. Where a definite material is not specified, a material which will enable the integrated circuits specified herein to meet the performance requirements of this specification shall be used. Acceptance or approval of any constituent material does not guarantee acceptance of the finished product.

4.4.1 Case

The case shall be hermetically sealed and have a ceramic body and the lids shall be welded, brazed, preform-soldered or glass-frit-sealed.

4.4.2 Lead Material and Finish

For dual-in-line and flat packages, the material shall be Type 'G' with Type '2' finish in accordance with the requirements of ESA/SCC Basic Specification No. 23500. For chip carrier packages the finish shall be Type '2' in accordance with the requirements of ESA/SCC Basic Specification No. 23500. (See Table 1(a) for Type Variants).

4.5 MARKING

4.5.1 General

The marking of all components delivered to this specification shall be in accordance with the requirements of ESA/SCC Basic Specification No. 21700 and the following paragraphs. When the component is too small to accommodate all of the marking specified, as much as space permits shall be marked and the marking information, in full, shall accompany the component in its primary package.

The information to be marked and the order of precedence, shall be as follows:-

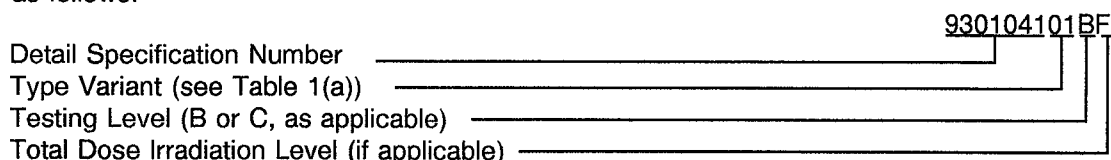
- (a) Lead Identification.
- (b) The SCC Component Number.
- (c) Traceability Information.

4.5.2 Lead Identification

For dual-in-line and flat packages, an index shall be located at the top of the package in the position defined in Note 1 to Figure 2 or, alternatively, a tab may be used to identify Pin No. 1. The pin numbering must be read with the index or tab on the left-hand side. For chip carrier packages, the index shall be as defined by Figure 2(b).

4.5.3 The SCC Component Number

Each component shall bear the SCC Component Number which shall be constituted and marked as follows:



The Total Dose Irradiation Level designation shall be added for those devices for which a sample has been successfully tested to the level in question. For these devices, a code letter shall be added in accordance with the requirements of ESA/SCC Basic Specification No. 22900.



4.5.4 Traceability Information

Each component shall be marked in respect of traceability information in accordance with the requirements of ESA/SCC Basic Specification No. 21700.

4.6 ELECTRICAL MEASUREMENTS

4.6.1 Electrical Measurements at Room Temperature

The parameters to be measured in respect of electrical characteristics are scheduled in Table 2. Unless otherwise specified, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.6.2 Electrical Measurements at High and Low Temperatures

The parameters to be measured at high and low temperatures are scheduled in Table 3. The measurements shall be performed at $T_{amb} = +125(+0-5)$ °C and $-55(+5-0)$ °C respectively.

4.6.3 Circuits for Electrical Measurements

Circuits for use in performing electrical measurements listed in Tables 2 and 3 of this specification are shown in Figure 4.

4.7 BURN-IN TESTS

4.7.1 Parameter Drift Values

The parameter drift values applicable to Power Burn-in are specified in Table 4 of this specification. Unless otherwise stated, measurements shall be performed at $T_{amb} = +22 \pm 3$ °C. The parameter drift values (Δ), applicable to the parameters scheduled, shall not be exceeded. In addition to these drift value requirements, the appropriate limit value specified for a given parameter in Table 2 shall not be exceeded.

4.7.2 Conditions for High Temperature Reverse Bias Burn-in

Not applicable.

4.7.3 Conditions for Power Burn-in

The requirements for Power Burn-in are specified in Section 7 of ESA/SCC Generic Specification No. 9000. The conditions for Power Burn-in shall be as specified in Table 5(b) of this specification.

4.7.4 Electrical Circuits for High Temperature Reverse Bias Burn-in

Not applicable.

4.7.5 Electrical Circuits for Power Burn-in

Circuits for use in performing the Power Burn-in tests are shown in Figure 5(b) of this specification.



TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
1 to 26	Functional Test 1 (Nominal Inputs)	-	3014	3(b)	Verify Truth Table. For Input/Output Conditions and Test Patterns, see Note 1	-	-	-
27 to 38	Functional Test 2 (Worst Case Inputs)	-	3014	3(b)	Verify Truth Table. For Input/Output Conditions and Test Patterns, see Note 1	-	-	-
39 to 40	Functional Test 3 (Worst Case Outputs)	-	3014	3(b)	Verify Truth Table. For Input/Output Conditions and Test Patterns, see Note 1	-	-	-
41 to 54	Input Current Low Level	I_{IL}	3009	4(a)	V_{IN} (Under Test) = 0V V_{IN} (Remaining Inputs) = 5.5V V_{DD} = 5.5V, V_{SS} = 0V (Pins D/F 1-2-3-4-5-6-7-15-22-23-24-25-26-27) (Pins C 2-3-4-5-6-7-8-18-25-26-28-29-30-31)	-	- 1.0	μ A
55 to 68	Input Current High Level	I_{IH}	3010	4(b)	V_{IN} (Under Test) = 5.5V V_{IN} (Remaining Inputs) = 0V V_{DD} = 5.5V, V_{SS} = 0V (Pins D/F 1-2-3-4-5-6-7-15-22-23-24-25-26-27) (Pins C 2-3-4-5-6-7-8-18-25-26-28-29-30-31)	-	1.0	μ A
69 to 80	Output Voltage Low Level	V_{OL}	3007	4(c)	V_{IL} = 0.8V, V_{IH} = 2.2V I_{OL} = 8.0mA V_{DD} = 4.5V, V_{SS} = 0V Note 2 (Pins D/F 8-9-10-11-12-13-16-17-18-19-20-21) (Pins C 9-10-11-13-14-15-19-20-21-22-23-24)	-	0.4	V

NOTES: See Page 30.



TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
81 to 92	Output Voltage High Level	V_{OH}	3007	4(d)	$V_{IL} = 0.8V, V_{IH} = 2.2V$ $I_{OH} = -2.0mA$ $V_{DD} = 4.5V, V_{SS} = 0V$ Note 2 (Pins D/F 8-9-10-11-12-13-16-17-18-19-20-21) (Pins C 9-10-11-13-14-15-19-20-21-22-23-24)	2.4	-	V
93 to 106	Input Clamp Voltage (to V_{SS})	V_{IC}	3008	4(e)	I_{IN} (Under Test) = $-200\mu A$ V_{IN} (Remaining Inputs) = $0V$ $V_{DD} = V_{SS} = 0V$ (Pins D/F 1-2-3-4-5-6-7-15-22-23-24-25-26-27) (Pins C 2-3-4-5-6-7-8-18-25-26-28-29-30-31)	-0.1	-1.9	V
107 to 115	Output Leakage Current Third State (Low Level Applied)	I_{OZL}	-	4(f)	$V_{IN}(\bar{R}) = 2.2V$ $V_{OUT} = 0V$ $V_{DD} = 5.5V, V_{SS} = 0V$ (Pins D/F 9-10-11-12-13-16-17-18-19) (Pins C 10-11-13-14-15-19-20-21-22)	-	-1.0	μA
116 to 124	Output Leakage Current Third State (High Level Applied)	I_{OZH}	-	4(f)	$V_{IN}(\bar{R}) = 2.2V$ $V_{OUT} = 5.5V$ $V_{DD} = 5.5V, V_{SS} = 0V$ (Pins D/F 9-10-11-12-13-16-17-18-19) (Pins C 10-11-13-14-15-19-20-21-22)	-	1.0	μA
125	Supply Current (Operating)	I_{DD1}	3005	4(g)	$V_{IL} = 0V, V_{IH} = 3.0V$ Pattern : ICCACT All Outputs Open $V_{DD} = 5.5V, V_{SS} = 0V$ Variants 1 to 3 : $f = 25MHz$ Variants 4 to 6 : $f = 20MHz$ Variants 7 to 9 : $f = 16.6MHz$ (Pin D/F 28) (Pin C 32)	-	140 120 100	mA

NOTES: See Page 30.

**TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS (CONT'D)**

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
126	Supply Current (Stand-by)	I _{DD2}	3005	4(g)	V _{IN(XI)} = 0V V _{IN(R, W, RS, FL/RT)} = 2.2V All Outputs Open V _{DD} = 5.5V, V _{SS} = 0V (Pin D/F 28) (Pin C 32)	-	1.5	mA
127	Supply Current (Power Down)	I _{DD3}	3005	4(g)	V _{IN(XI)} = 0V V _{IN(Remaining Inputs)} = 5.5V All Outputs Open V _{DD} = 5.5V, V _{SS} = 0V (Pin D/F 28) (Pin C 32)	-	80	μA

NOTES

- Functional test go-no-go with the following test sequences:

FUNCTIONAL TEST 1

Pattern	Rate (ns)	V _{DD} (V)	V _{SS} (V)	V _{IL} (V)	V _{IH} (V)	I _{OL} (mA)	I _{OH} (mA)	V _{OUT COMP} (V)
WRT-RD000	175	4.5 and 5.5	0	0	3.0	8.0	-2.0	1.5
WRT-RD1FF	175	4.5 and 5.5	0	0	3.0	8.0	-2.0	1.5
MARCH-000	175	4.5 and 5.5	0	0	3.0	8.0	-2.0	1.5
MARCH-155	175	4.5 and 5.5	0	0	3.0	8.0	-2.0	1.5
MARCH-1FF	175	4.5 and 5.5	0	0	3.0	8.0	-2.0	1.5
FIFO-000	175	4.5 and 5.5	0	0	3.0	8.0	-2.0	1.5
FIFO-155	175	4.5 and 5.5	0	0	3.0	8.0	-2.0	1.5
FIFO-1FF	175	4.5 and 5.5	0	0	3.0	8.0	-2.0	1.5
ADDRESS	175	4.5 and 5.5	0	0	3.0	8.0	-2.0	1.5
CKBD-000	175	4.5 and 5.5	0	0	3.0	8.0	-2.0	1.5
CKBD-1FF	175	4.5 and 5.5	0	0	3.0	8.0	-2.0	1.5
FLAGS	175	4.5 and 5.5	0	0	3.0	8.0	-2.0	1.5
Xi	175	4.5 and 5.5	0	0	3.0	8.0	-2.0	1.5

**TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE (CONTINUED)****FUNCTIONAL TEST 2**

Pattern	Rate (ns)	V _{DD} (V)	V _{SS} (V)	V _{IL} (V)	V _{IH} (V)	I _{OL} (mA)	I _{OH} (mA)	V _{OUT COMP} (V)
FIFO-155	175	4.5 and 5.5	0	0.8	V _{DD}	8.0	-2.0	1.5
FIFO-155	175	4.5 and 5.5	0	0	2.2	8.0	-2.0	1.5
FLAGS	175	4.5 and 5.5	0	0.8	V _{DD}	8.0	-2.0	1.5
FLAGS	175	4.5 and 5.5	0	0	2.2	8.0	-2.0	1.5
Xi	175	4.5 and 5.5	0	0.8	V _{DD}	8.0	-2.0	1.5
Xi	175	4.5 and 5.5	0	0	2.2	8.0	-2.0	1.5

FUNCTIONAL TEST 3

Pattern	Rate (ns)	V _{DD} (V)	V _{SS} (V)	V _{IL} (V)	V _{IH} (V)	I _{OL} (mA)	I _{OH} (mA)	V _{OUT COMP} (V)
FIFO-000	175	5.5	0	0	3.0	8.0	-2.0	0.4
FIFO-1FF	175	4.5	0	0	3.0	8.0	-2.0	2.4

- Measurements performed using MARCH-000H and MARCH-1FFH test patterns.
- Guaranteed but not tested. Characterised at initial design and after major process changes.

4. FUNCTIONAL TEST 4

Pattern	TRLRL (ns)	TRLRL (ns)	TRLRL (ns)	V _{DD} (V)	V _{SS} (V)	V _{IL} (V)	V _{IH} (V)	I _{OL} (mA)	I _{OH} (mA)	V _{OUT COMP} (V)
	Var. 1-2-3	Var. 4-5-6	Var. 7-8-9							
MARCH-000	40	50	60	4.5 and 5.5	0	0	3.0	8.0	-2.0	1.5
MARCH-155	40	50	60	4.5 and 5.5	0	0	3.0	8.0	-2.0	1.5
MARCH-1FF	40	50	60	4.5 and 5.5	0	0	3.0	8.0	-2.0	1.5
FIFO-000	40	50	60	4.5 and 5.5	0	0	3.0	8.0	-2.0	1.5
FIFO-155	40	50	60	4.5 and 5.5	0	0	3.0	8.0	-2.0	1.5
FIFO-1FF	40	50	60	4.5 and 5.5	0	0	3.0	8.0	-2.0	1.5
FLAGS	40	50	60	4.5 and 5.5	0	0	3.0	8.0	-2.0	1.5
Xi	40	50	60	4.5 and 5.5	0	0	3.0	8.0	-2.0	1.5

Output load = 1 TTL gate equivalent + C_L ≤ 100pF.
t_r = t_f = 5.0ns maximum.

- Parameter measured during Functional Test 4 using the following test pattern:-

For TRLRL and TRLQV : MARCH-000H.
For TDVWH and TWHDX : FIFO-1FFH.
For remainder : FLAGS.

- Parameters tested go-no-go during Functional Test 4.



TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
128 to 141	Input Capacitance	C _{IN}	3012	4(h)	V _{IN} (Not Under Test) = 0V V _{DD} = V _{SS} = 0V Note 3 (Pins D/F 1-2-3-4-5-6-7-15-22-23-24-25-26-27) (Pins C 2-3-4-5-6-7-8-18-25-26-28-29-30-31)	-	8.0	pF
142 to 153	Output Capacitance	C _{OUT}	3012	4(i)	V _{IN} (Not Under Test) = 0V V _{DD} = V _{SS} = 0V Note 3 (Pins D/F 8-9-10-11-12-13-16-17-18-19-20-21) (Pins C 9-10-11-13-14-15-19-20-21-22-23-24)	-	8.0	pF
154 to 155	Read Pulse Low to Data Bus Low Impedance	TRLQX	3004	4(j)	V _{DD} = 4.5V and 5.5V V _{SS} = 0V Note 3 Variants 1-2-3 Variants 4-5-6 Variants 7-8-9	5.0 5.0 10	- - -	ns
156 to 157	Write Pulse Low to Data Bus Low Impedance	TWHQX	3004	4(j)	V _{DD} = 4.5V and 5.5V V _{SS} = 0V Note 3 Variants 1-2-3 Variants 4-5-6 Variants 7-8-9	10 10 15	- - -	ns
158 to 159	Read Pulse High to Data Bus High Impedance	TRHQZ	3004	4(j)	V _{DD} = 4.5V and 5.5V V _{SS} = 0V Note 3 Variants 1-2-3 Variants 4-5-6 Variants 7-8-9	- - -	20 25 30	ns
160 to 161	Retransmit Set-up Time	TWHRTH	3004	4(j)	V _{DD} = 4.5V and 5.5V V _{SS} = 0V Note 3 Variants 1-2-3 Variants 4-5-6 Variants 7-8-9	30 40 50	- - -	ns

NOTES: See Page 30.



TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
162 to 163	Reset to Empty Flag Low	TRSLEFL	3004	4(j)	V _{DD} = 4.5V and 5.5V V _{SS} = 0V Note 3 Variants 1-2-3 Variants 4-5-6 Variants 7-8-9	- - -	40 50 60	ns
164 to 165	Read/Write to XO High	TWHXOH	3004	4(j)	V _{DD} = 4.5V and 5.5V V _{SS} = 0V Note 3 Variants 1-2-3 Variants 4-5-6 Variants 7-8-9	- - -	30 40 50	ns
166 to 181	Functional Test 4 (Nominal Inputs)	-	3004	3(b)	Verify Truth Table. For Input/Output Conditions and Test Patterns, see Note 4 V _{DD} = 4.5V and 5.5V V _{SS} = 0V	-	-	-
182 to 183	Read Cycle Time	TRLRL	3004	4(j)	V _{DD} = 4.5V and 5.5V V _{SS} = 0V Notes 4 and 5 Variants 1-2-3 Variants 4-5-6 Variants 7-8-9	40 50 65	- - -	ns
184 to 185	Access Time	TRLQV	3004	4(j)	V _{DD} = 4.5V and 5.5V V _{SS} = 0V Notes 4 and 5 Variants 1-2-3 Variants 4-5-6 Variants 7-8-9	- - -	30 40 50	ns
186 to 187	Data Set-up Time	TDVWH	3004	4(j)	V _{DD} = 4.5V and 5.5V V _{SS} = 0V Notes 4 and 5 Variants 1-2-3 Variants 4-5-6 Variants 7-8-9	18 20 30	- - -	ns
188 to 189	Data Hold Time	TWHDX	3004	4(j)	V _{DD} = 4.5V and 5.5V V _{SS} = 0V Notes 4 and 5 Variants 1-2-3 Variants 4-5-6 Variants 7-8-9	0 0 5.0	- - -	ns

NOTES: See Page 30.



TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
190 to 191	Read Low to Empty Flag Low	TRLEFL	3004	4(j)	$V_{DD} = 4.5V$ and $5.5V$ $V_{SS} = 0V$ Notes 4 and 5 Variants 1-2-3 Variants 4-5-6 Variants 7-8-9	-	30	ns
192 to 193	Write High to Empty Flag High	TWHEFH	3004	4(j)	$V_{DD} = 4.5V$ and $5.5V$ $V_{SS} = 0V$ Notes 4 and 5 Variants 1-2-3 Variants 4-5-6 Variants 7-8-9	-	30	ns
194 to 195	Read High to Full Flag High	TRHFFH	3004	4(j)	$V_{DD} = 4.5V$ and $5.5V$ $V_{SS} = 0V$ Notes 4 and 5 Variants 1-2-3 Variants 4-5-6 Variants 7-8-9	-	30	ns
196 to 197	Write Low to Full Flag Low	TWLFFL	3004	4(j)	$V_{DD} = 4.5V$ and $5.5V$ $V_{SS} = 0V$ Notes 4 and 5 Variants 1-2-3 Variants 4-5-6 Variants 7-8-9	-	30	ns
198 to 199	Write Low to Half Full Flag Low	TWLHFL	3004	4(j)	$V_{DD} = 4.5V$ and $5.5V$ $V_{SS} = 0V$ Notes 4 and 5 Variants 1-2-3 Variants 4-5-6 Variants 7-8-9	-	40	ns
200 to 201	Read Recovery Time	TRHRL	3004	4(j)	$V_{DD} = 4.5V$ and $5.5V$ $V_{SS} = 0V$ Notes 4 and 6 Variants 1-2-3 Variants 4-5-6 Variants 7-8-9	10	-	ns
202 to 203	Read Pulse Width	TRLRH	3004	4(j)	$V_{DD} = 4.5V$ and $5.5V$ $V_{SS} = 0V$ Notes 4 and 6 Variants 1-2-3 Variants 4-5-6 Variants 7-8-9	30	-	ns
						10	-	
						15	-	
						40	-	
						50	-	

NOTES: See Page 30.



TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
204 to 205	Data Valid from Read Pulse High	TRHQX	3004	4(j)	V _{DD} = 4.5V and 5.5V V _{SS} = 0V Notes 4 and 6	5.0	-	ns
206 to 207	Write Cycle Time	TWLWL	3004	4(j)	V _{DD} = 4.5V and 5.5V V _{SS} = 0V Notes 4 and 6 Variants 1-2-3 Variants 4-5-6 Variants 7-8-9	40 50 65	- - -	ns
208 to 209	Write Pulse Width	TWLWH	3004	4(j)	V _{DD} = 4.5V and 5.5V V _{SS} = 0V Notes 4 and 6 Variants 1-2-3 Variants 4-5-6 Variants 7-8-9	30 40 50	- - -	ns
210 to 211	Write Recovery Time	TWHWL	3004	4(j)	V _{DD} = 4.5V and 5.5V V _{SS} = 0V Notes 4 and 6 Variants 1-2-3 Variants 4-5-6 Variants 7-8-9	10 10 15	- - -	ns
212 to 213	Reset Cycle	TRSLWL	3004	4(j)	V _{DD} = 4.5V and 5.5V V _{SS} = 0V Notes 4 and 6 Variants 1-2-3 Variants 4-5-6 Variants 7-8-9	40 50 65	- - -	ns
214 to 215	Reset Pulse Width	TRSLRSH	3004	4(j)	V _{DD} = 4.5V and 5.5V V _{SS} = 0V Notes 4 and 6 Variants 1-2-3 Variants 4-5-6 Variants 7-8-9	30 40 50	- - -	ns
216 to 217	Reset Set-up Time	TWHRSH	3004	4(j)	V _{DD} = 4.5V and 5.5V V _{SS} = 0V Notes 4 and 6 Variants 1-2-3 Variants 4-5-6 Variants 7-8-9	30 40 50	- - -	ns

NOTES: See Page 30.



TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
218 to 219	Reset Recovery Time	TRSHWL	3004	4(j)	V _{DD} = 4.5V and 5.5V V _{SS} = 0V Notes 4 and 6 Variants 1-2-3 Variants 4-5-6 Variants 7-8-9	10 10 15	- - -	ns
220 to 221	Retransmit Cycle Time	TRTLWL	3004	4(j)	V _{DD} = 4.5V and 5.5V V _{SS} = 0V Notes 4 and 6 Variants 1-2-3 Variants 4-5-6 Variants 7-8-9	40 50 65	- - -	ns
222 to 223	Retransmit Pulse Width	TRTLRTH	3004	4(j)	V _{DD} = 4.5V and 5.5V V _{SS} = 0V Notes 4 and 6 Variants 1-2-3 Variants 4-5-6 Variants 7-8-9	30 40 50	- - -	ns
224 to 225	Retransmit Recovery Time	TRTHWL	3004	4(j)	V _{DD} = 4.5V and 5.5V V _{SS} = 0V Notes 4 and 6 Variants 1-2-3 Variants 4-5-6 Variants 7-8-9	10 10 15	- - -	ns
226 to 227	Reset to Half Full Flag High	TRSLHFH	3004	4(j)	V _{DD} = 4.5V and 5.5V V _{SS} = 0V Notes 4 and 6 Variants 1-2-3 Variants 4-5-6 Variants 7-8-9	- - -	40 50 60	ns
228 to 229	Reset to Full Flag High	TRSLFFH	3004	4(j)	V _{DD} = 4.5V and 5.5V V _{SS} = 0V Notes 4 and 6 Variants 1-2-3 Variants 4-5-6 Variants 7-8-9	- - -	40 50 60	ns
230 to 231	Read Pulse Width after EF High	TEFHRH	3004	4(j)	V _{DD} = 4.5V and 5.5V V _{SS} = 0V Notes 4 and 6 Variants 1-2-3 Variants 4-5-6 Variants 7-8-9	30 40 50	- - -	ns

NOTES: See Page 30.

**TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS (CONT'D)**

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
232 to 233	Read High to Half Flag High	TRHHFH	3004	4(j)	V _{DD} = 4.5V and 5.5V V _{SS} = 0V Notes 4 and 6 Variants 1-2-3 Variants 4-5-6 Variants 7-8-9	-	40	ns
234 to 235	Write Pulse Width after FF High	TFFHWH	3004	4(j)	V _{DD} = 4.5V and 5.5V V _{SS} = 0V Notes 4 and 6 Variants 1-2-3 Variants 4-5-6 Variants 7-8-9	30 40 50	-	ns
236 to 237	Read/Write to XO Low	TWLXOL	3004	4(j)	V _{DD} = 4.5V and 5.5V V _{SS} = 0V Notes 4 and 6 Variants 1-2-3 Variants 4-5-6 Variants 7-8-9	-	30 40 50	ns
238 to 239	XI Pulse Width	TXILXIH	3004	4(j)	V _{DD} = 4.5V and 5.5V V _{SS} = 0V Notes 4 and 6 Variants 1-2-3 Variants 4-5-6 Variants 7-8-9	30 40 50	-	ns
240 to 241	XI Recovery Time	TXIHXL	3004	4(j)	V _{DD} = 4.5V and 5.5V V _{SS} = 0V Notes 4 and 6	10	-	ns
242 to 243	XI Set-up Time	TXILRL	3004	4(j)	V _{DD} = 4.5V and 5.5V V _{SS} = 0V Notes 4 and 6 Variants 1-2-3 Variants 4-5-6 Variants 7-8-9	10 10 15	-	ns

NOTES: See Page 30.

**TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES,
d.c. PARAMETERS**

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
1 to 26	Functional Test 1 (Nominal Inputs)	-	3014	3(b)	Verify Truth Table. For Input/Output Conditions and Test Patterns, see Note 1	-	-	-
27 to 38	Functional Test 2 (Worst Case Inputs)	-	3014	3(b)	Verify Truth Table. For Input/Output Conditions and Test Patterns, see Note 1	-	-	-
39 to 40	Functional Test 3 (Worst Case Outputs)	-	3014	3(b)	Verify Truth Table. For Input/Output Conditions and Test Patterns, see Note 1	-	-	-
41 to 54	Input Current Low Level	I_{IL}	3009	4(a)	V_{IN} (Under Test) = 0V V_{IN} (Remaining Inputs) = 5.5V V_{DD} = 5.5V, V_{SS} = 0V (Pins D/F 1-2-3-4-5-6-7-15-22-23-24-25-26-27) (Pins C 2-3-4-5-6-7-8-18-25-26-28-29-30-31)	-	-1.0	μ A
55 to 68	Input Current High Level	I_{IH}	3010	4(b)	V_{IN} (Under Test) = 5.5V V_{IN} (Remaining Inputs) = 0V V_{DD} = 5.5V, V_{SS} = 0V (Pins D/F 1-2-3-4-5-6-7-15-22-23-24-25-26-27) (Pins C 2-3-4-5-6-7-8-18-25-26-28-29-30-31)	-	1.0	μ A
69 to 80	Output Voltage Low Level	V_{OL}	3007	4(c)	V_{IL} = 0.8V, V_{IH} = 2.2V I_{OL} = 8.0mA V_{DD} = 4.5V, V_{SS} = 0V Note 2 (Pins D/F 8-9-10-11-12-13-16-17-18-19-20-21) (Pins C 9-10-11-13-14-15-19-20-21-22-23-24)	-	0.4	V

NOTES: See Page 30.

**TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES,
d.c. PARAMETERS (CONT'D)**

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
81 to 92	Output Voltage High Level	V_{OH}	3007	4(d)	$V_{IL} = 0.8V$, $V_{IH} = 2.2V$ $I_{OH} = -2.0mA$ $V_{DD} = 4.5V$, $V_{SS} = 0V$ Note 2 (Pins D/F 8-9-10-11-12-13-16-17-18-19-20-21) (Pins C 9-10-11-13-14-15-19-20-21-22-23-24)	2.4	-	V
93 to 106	Input Clamp Voltage (to V_{SS})	V_{IC}	3008	4(e)	I_{IN} (Under Test) = $-200\mu A$ V_{IN} (Remaining Inputs) = $0V$ $V_{DD} = V_{SS} = 0V$ (Pins D/F 1-2-3-4-5-6-7-15-22-23-24-25-26-27) (Pins C 2-3-4-5-6-7-8-18-25-26-28-29-30-31)	-0.1	-1.9	V
107 to 115	Output Leakage Current Third State (Low Level Applied)	I_{OZL}	-	4(f)	$V_{IN}(\bar{R}) = 2.2V$ $V_{OUT} = 0V$ $V_{DD} = 5.5V$, $V_{SS} = 0V$ (Pins D/F 9-10-11-12-13-16-17-18-19) (Pins C 10-11-13-14-15-19-20-21-22)	-	-1.0	μA
116 to 124	Output Leakage Current Third State (High Level Applied)	I_{OZH}	-	4(f)	$V_{IN}(\bar{R}) = 2.2V$ $V_{OUT} = 5.5V$ $V_{DD} = 5.5V$, $V_{SS} = 0V$ (Pins D/F 9-10-11-12-13-16-17-18-19) (Pins C 10-11-13-14-15-19-20-21-22)	-	1.0	μA
125	Supply Current (Operating)	I_{DD1}	3005	4(g)	$V_{IL} = 0V$, $V_{IH} = 3.0V$ Pattern : ICCACT All Outputs Open $V_{DD} = 5.5V$, $V_{SS} = 0V$ Variants 1 to 3 : $f = 25MHz$ Variants 4 to 6 : $f = 20MHz$ Variants 7 to 9 : $f = 16.6MHz$ (Pin D/F 28) (Pin C 32)	-	140 120 100	mA

NOTES: See Page 30.

**TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES,
d.c. PARAMETERS (CONT'D)**

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
126	Supply Current (Stand-by)	I_{DD2}	3005	4(g)	$V_{IN(XI)} = 0V$ $V_{IN(R, W, RS, FL/RT)} = 2.2V$ All Outputs Open $V_{DD} = 5.5V, V_{SS} = 0V$ (Pin D/F 28) (Pin C 32)	-	1.5	mA
127	Supply Current (Power Down)	I_{DD3}	3005	4(g)	$V_{IN(XI)} = 0V$ $V_{IN(Remaining\ Inputs)} = 5.5V$ All Outputs Open $V_{DD} = 5.5V, V_{SS} = 0V$ (Pin D/F 28) (Pin C 32)	-	80	μA

NOTES: See Page 30.



**TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES,
a.c. PARAMETERS**

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
128 to 141	Input Capacitance	C _{IN}	3012	4(h)	V _{IN} (Not Under Test) = 0V V _{DD} = V _{SS} = 0V Note 3 (Pins D/F 1-2-3-4-5-6-7-15-22-23-24-25-26-27) (Pins C 2-3-4-5-6-7-8-18-25-26-28-29-30-31)	-	8.0	pF
142 to 153	Output Capacitance	C _{OUT}	3012	4(i)	V _{IN} (Not Under Test) = 0V V _{DD} = V _{SS} = 0V Note 3 (Pins D/F 8-9-10-11-12-13-16-17-18-19-20-21) (Pins C 9-10-11-13-14-15-19-20-21-22-23-24)	-	8.0	pF
154 to 155	Read Pulse Low to Data Bus Low Impedance	TRLQX	3004	4(j)	V _{DD} = 4.5V and 5.5V V _{SS} = 0V Note 3 Variants 1-2-3 Variants 4-5-6 Variants 7-8-9	5.0 5.0 10	- - -	ns
156 to 157	Write Pulse Low to Data Bus Low Impedance	TWHQX	3004	4(j)	V _{DD} = 4.5V and 5.5V V _{SS} = 0V Note 3 Variants 1-2-3 Variants 4-5-6 Variants 7-8-9	10 10 15	- - -	ns
158 to 159	Read Pulse High to Data Bus High Impedance	TRHQZ	3004	4(j)	V _{DD} = 4.5V and 5.5V V _{SS} = 0V Note 3 Variants 1-2-3 Variants 4-5-6 Variants 7-8-9	- - -	20 25 30	ns
160 to 161	Retransmit Set-up Time	TWHRTH	3004	4(j)	V _{DD} = 4.5V and 5.5V V _{SS} = 0V Note 3 Variants 1-2-3 Variants 4-5-6 Variants 7-8-9	30 40 50	- - -	ns

NOTES: See Page 30.



**TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES,
a.c. PARAMETERS (CONT'D)**

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
162 to 163	Reset to Empty Flag Low	TRSLEFL	3004	4(j)	V _{DD} = 4.5V and 5.5V V _{SS} = 0V Note 3 Variants 1-2-3 Variants 4-5-6 Variants 7-8-9	-	40 50 60	ns
164 to 165	Read/Write to XO High	TWHXOH	3004	4(j)	V _{DD} = 4.5V and 5.5V V _{SS} = 0V Note 3 Variants 1-2-3 Variants 4-5-6 Variants 7-8-9	-	30 40 50	ns
166 to 181	Functional Test 4 (Nominal Inputs)	-	3004	3(b)	Verify Truth Table. For Input/Output Conditions and Test Patterns, see Note 4 V _{DD} = 4.5V and 5.5V V _{SS} = 0V	-	-	-
182 to 183	Read Cycle Time	TRLRL	3004	4(j)	V _{DD} = 4.5V and 5.5V V _{SS} = 0V Notes 4 and 5 Variants 1-2-3 Variants 4-5-6 Variants 7-8-9	40 50 65	- - -	ns
184 to 185	Access Time	TRLQV	3004	4(j)	V _{DD} = 4.5V and 5.5V V _{SS} = 0V Notes 4 and 5 Variants 1-2-3 Variants 4-5-6 Variants 7-8-9	-	30 40 50	ns
186 to 187	Data Set-up Time	TDVWH	3004	4(j)	V _{DD} = 4.5V and 5.5V V _{SS} = 0V Notes 4 and 5 Variants 1-2-3 Variants 4-5-6 Variants 7-8-9	18 20 30	- - -	ns
188 to 189	Data Hold Time	TWHDX	3004	4(j)	V _{DD} = 4.5V and 5.5V V _{SS} = 0V Notes 4 and 5 Variants 1-2-3 Variants 4-5-6 Variants 7-8-9	0 0 5.0	- - -	ns

NOTES: See Page 30.



**TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES,
a.c. PARAMETERS (CONT'D)**

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
190 to 191	Read Low to Empty Flag Low	TRLEFL	3004	4(j)	$V_{DD} = 4.5V$ and $5.5V$ $V_{SS} = 0V$ Notes 4 and 5 Variants 1-2-3 Variants 4-5-6 Variants 7-8-9	-	30	ns
192 to 193	Write High to Empty Flag High	TWHEFH	3004	4(j)	$V_{DD} = 4.5V$ and $5.5V$ $V_{SS} = 0V$ Notes 4 and 5 Variants 1-2-3 Variants 4-5-6 Variants 7-8-9	-	30 35 45	ns
194 to 195	Read High to Full Flag High	TRHFFH	3004	4(j)	$V_{DD} = 4.5V$ and $5.5V$ $V_{SS} = 0V$ Notes 4 and 5 Variants 1-2-3 Variants 4-5-6 Variants 7-8-9	-	30 35 45	ns
196 to 197	Write Low to Full Flag Low	TWLFFL	3004	4(j)	$V_{DD} = 4.5V$ and $5.5V$ $V_{SS} = 0V$ Notes 4 and 5 Variants 1-2-3 Variants 4-5-6 Variants 7-8-9	-	30 35 45	ns
198 to 199	Write Low to Half Full Flag Low	TWLHFL	3004	4(j)	$V_{DD} = 4.5V$ and $5.5V$ $V_{SS} = 0V$ Notes 4 and 5 Variants 1-2-3 Variants 4-5-6 Variants 7-8-9	-	40 50 60	ns
200 to 201	Read Recovery Time	TRHRL	3004	4(j)	$V_{DD} = 4.5V$ and $5.5V$ $V_{SS} = 0V$ Notes 4 and 6 Variants 1-2-3 Variants 4-5-6 Variants 7-8-9	10 10 15	- - -	ns
202 to 203	Read Pulse Width	TRLRH	3004	4(j)	$V_{DD} = 4.5V$ and $5.5V$ $V_{SS} = 0V$ Notes 4 and 6 Variants 1-2-3 Variants 4-5-6 Variants 7-8-9	30 40 50	- - -	ns

NOTES: See Page 30.



**TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES,
a.c. PARAMETERS (CONT'D)**

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
204 to 205	Data Valid from Read Pulse High	TRHQX	3004	4(j)	V _{DD} = 4.5V and 5.5V V _{SS} = 0V Notes 4 and 6	5.0	-	ns
206 to 207	Write Cycle Time	TWLWL	3004	4(j)	V _{DD} = 4.5V and 5.5V V _{SS} = 0V Notes 4 and 6 Variants 1-2-3 Variants 4-5-6 Variants 7-8-9	40 50 65	- - -	ns
208 to 209	Write Pulse Width	TWLWH	3004	4(j)	V _{DD} = 4.5V and 5.5V V _{SS} = 0V Notes 4 and 6 Variants 1-2-3 Variants 4-5-6 Variants 7-8-9	30 40 50	- - -	ns
210 to 211	Write Recovery Time	TWHWL	3004	4(j)	V _{DD} = 4.5V and 5.5V V _{SS} = 0V Notes 4 and 6 Variants 1-2-3 Variants 4-5-6 Variants 7-8-9	10 10 15	- - -	ns
212 to 213	Reset Cycle	TRSLWL	3004	4(j)	V _{DD} = 4.5V and 5.5V V _{SS} = 0V Notes 4 and 6 Variants 1-2-3 Variants 4-5-6 Variants 7-8-9	40 50 65	- - -	ns
214 to 215	Reset Pulse Width	TRSLRSH	3004	4(j)	V _{DD} = 4.5V and 5.5V V _{SS} = 0V Notes 4 and 6 Variants 1-2-3 Variants 4-5-6 Variants 7-8-9	30 40 50	- - -	ns
216 to 217	Reset Set-up Time	TWHRSH	3004	4(j)	V _{DD} = 4.5V and 5.5V V _{SS} = 0V Notes 4 and 6 Variants 1-2-3 Variants 4-5-6 Variants 7-8-9	30 40 50	- - -	ns

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**TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES,
a.c. PARAMETERS (CONT'D)**

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
218 to 219	Reset Recovery Time	TRSHWL	3004	4(j)	V _{DD} = 4.5V and 5.5V V _{SS} = 0V Notes 4 and 6 Variants 1-2-3 Variants 4-5-6 Variants 7-8-9	10 10 15	- - -	ns
220 to 221	Retransmit Cycle Time	TRTLWL	3004	4(j)	V _{DD} = 4.5V and 5.5V V _{SS} = 0V Notes 4 and 6 Variants 1-2-3 Variants 4-5-6 Variants 7-8-9	40 50 65	- - -	ns
222 to 223	Retransmit Pulse Width	TRTLRTH	3004	4(j)	V _{DD} = 4.5V and 5.5V V _{SS} = 0V Notes 4 and 6 Variants 1-2-3 Variants 4-5-6 Variants 7-8-9	30 40 50	- - -	ns
224 to 225	Retransmit Recovery Time	TRTHWL	3004	4(j)	V _{DD} = 4.5V and 5.5V V _{SS} = 0V Notes 4 and 6 Variants 1-2-3 Variants 4-5-6 Variants 7-8-9	10 10 15	- - -	ns
226 to 227	Reset to Half Full Flag High	TRSLHFH	3004	4(j)	V _{DD} = 4.5V and 5.5V V _{SS} = 0V Notes 4 and 6 Variants 1-2-3 Variants 4-5-6 Variants 7-8-9	- - -	40 50 60	ns
228 to 229	Reset to Full Flag High	TRSLFFH	3004	4(j)	V _{DD} = 4.5V and 5.5V V _{SS} = 0V Notes 4 and 6 Variants 1-2-3 Variants 4-5-6 Variants 7-8-9	- - -	40 50 60	ns
230 to 231	Read Pulse Width after EF High	TEFHRH	3004	4(j)	V _{DD} = 4.5V and 5.5V V _{SS} = 0V Notes 4 and 6 Variants 1-2-3 Variants 4-5-6 Variants 7-8-9	30 40 50	- - -	ns

NOTES: See Page 30.



**TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES,
a.c. PARAMETERS (CONT'D)**

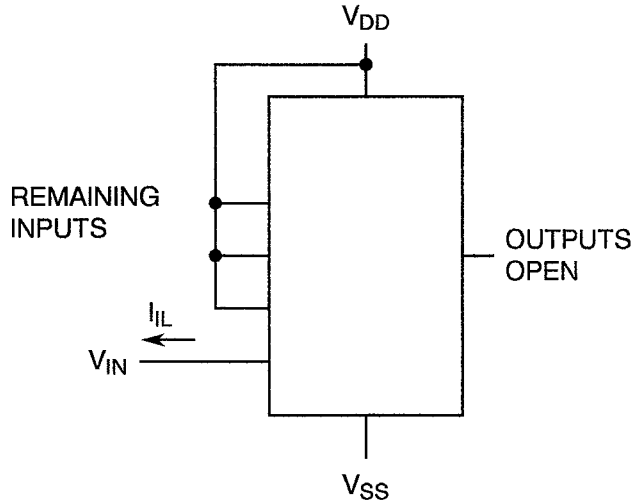
No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
232 to 233	Read High to Half Flag High	TRHHFH	3004	4(j)	V _{DD} = 4.5V and 5.5V V _{SS} = 0V Notes 4 and 6 Variants 1-2-3 Variants 4-5-6 Variants 7-8-9	-	40	ns
234 to 235	Write Pulse Width after FF High	TFFHWH	3004	4(j)	V _{DD} = 4.5V and 5.5V V _{SS} = 0V Notes 4 and 6 Variants 1-2-3 Variants 4-5-6 Variants 7-8-9	30 40 50	- - -	ns
236 to 237	Read/Write to XO Low	TWLXOL	3004	4(j)	V _{DD} = 4.5V and 5.5V V _{SS} = 0V Notes 4 and 6 Variants 1-2-3 Variants 4-5-6 Variants 7-8-9	-	30 40 50	ns
238 to 239	XI Pulse Width	TXILXIH	3004	4(j)	V _{DD} = 4.5V and 5.5V V _{SS} = 0V Notes 4 and 6 Variants 1-2-3 Variants 4-5-6 Variants 7-8-9	30 40 50	- - -	ns
240 to 241	XI Recovery Time	TXIHXIL	3004	4(j)	V _{DD} = 4.5V and 5.5V V _{SS} = 0V Notes 4 and 6	10	-	ns
242 to 243	XI Set-up Time	TXILRL	3004	4(j)	V _{DD} = 4.5V and 5.5V V _{SS} = 0V Notes 4 and 6 Variants 1-2-3 Variants 4-5-6 Variants 7-8-9	10 10 15	- - -	ns

NOTES: See Page 30.



FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS

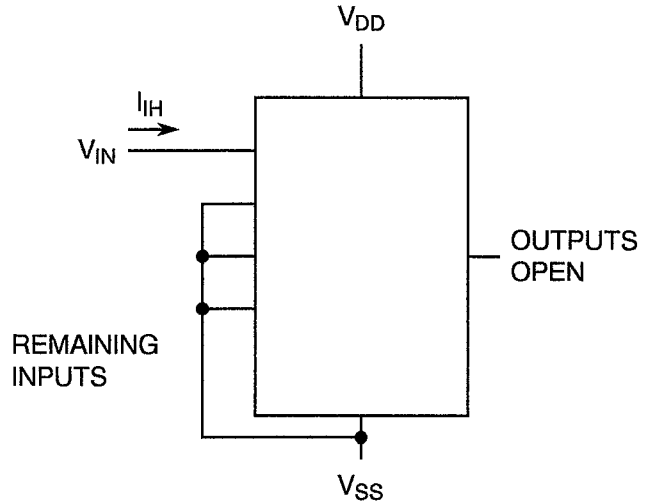
FIGURE 4(a) - INPUT CURRENT LOW LEVEL



NOTES

- 1. Each input to be tested separately.

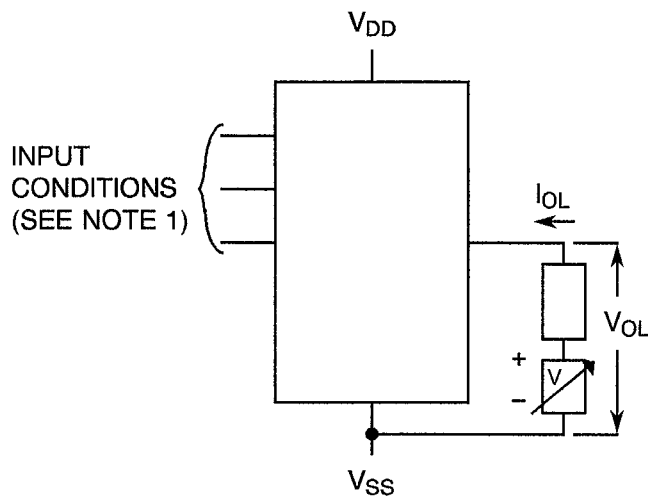
FIGURE 4(b) - INPUT CURRENT HIGH LEVEL



NOTES

- 1. Each input to be tested separately.

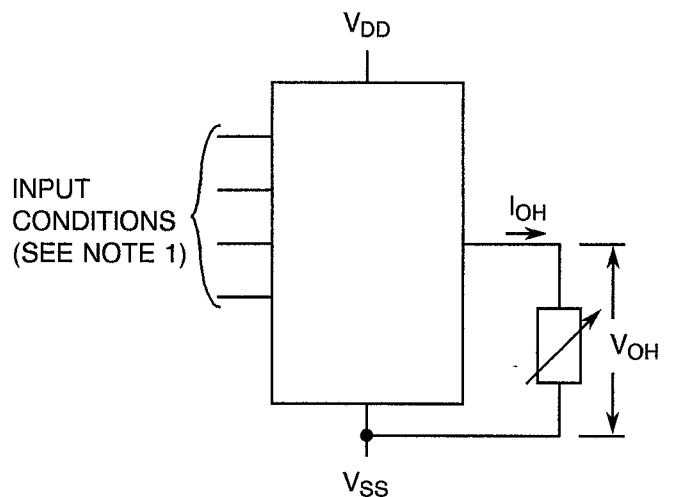
FIGURE 4(c) - OUTPUT VOLTAGE LOW LEVEL



NOTES

- 1. See Note 2 to Table 2.
- 2. Each output to be tested separately.

FIGURE 4(d) - OUTPUT VOLTAGE HIGH LEVEL



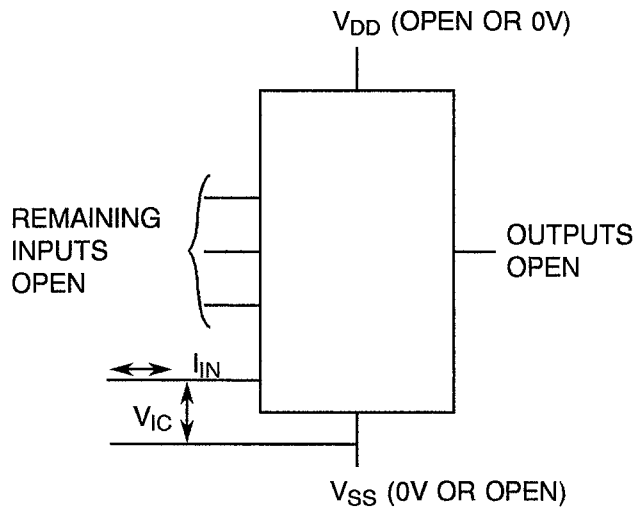
NOTES

- 1. See Note 2 to Table 2.
- 2. Each output to be tested separately.



FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

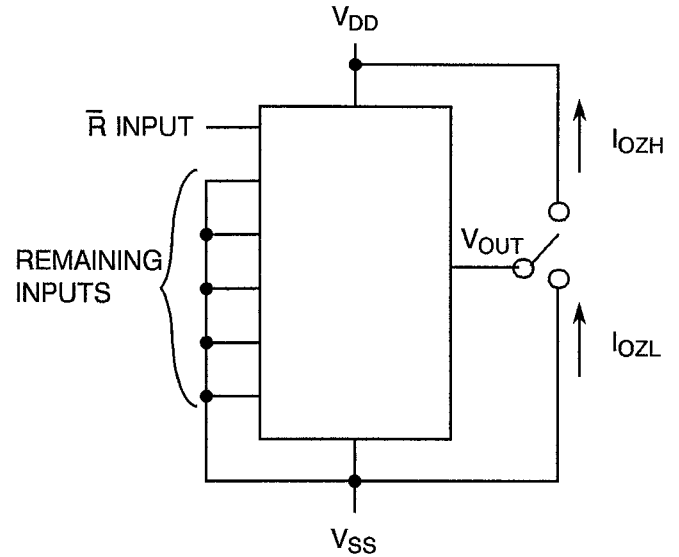
FIGURE 4(e) - INPUT CLAMP VOLTAGE



NOTES

- 1. Each input to be tested separately.

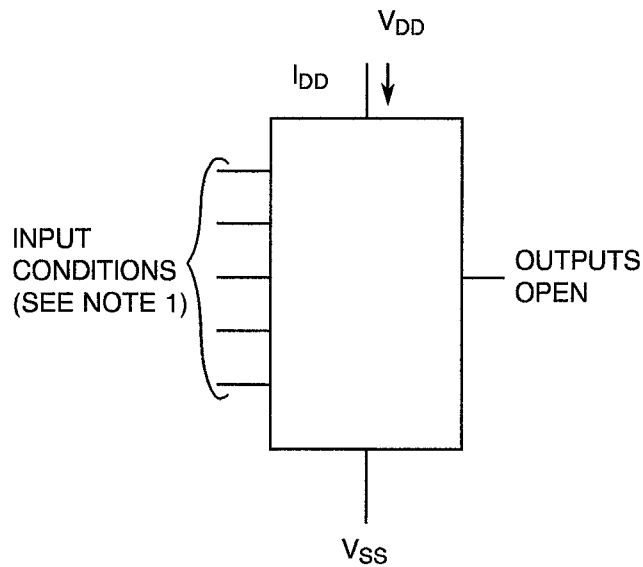
FIGURE 4(f) - OUTPUT LEAKAGE CURRENT THIRD STATE



NOTES

- 1. Each output to be tested separately.

FIGURE 4(g) - SUPPLY CURRENT



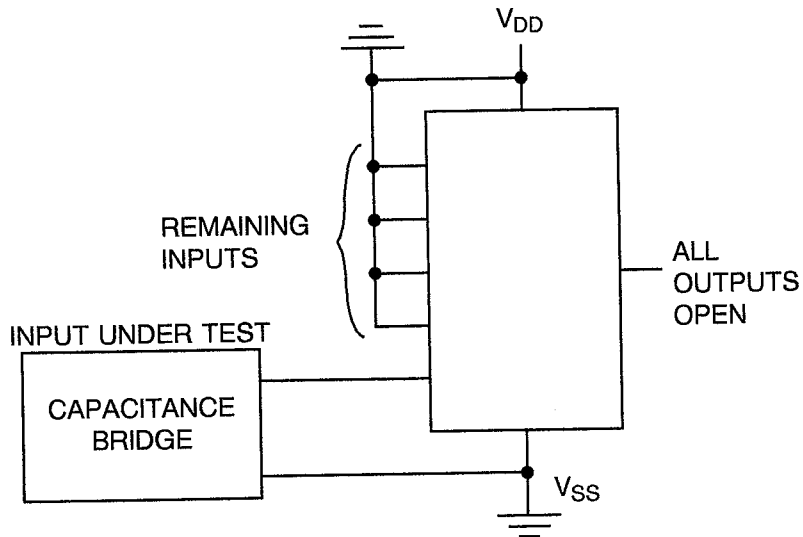
NOTES

- 1. As per Table 2 or 3.



FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

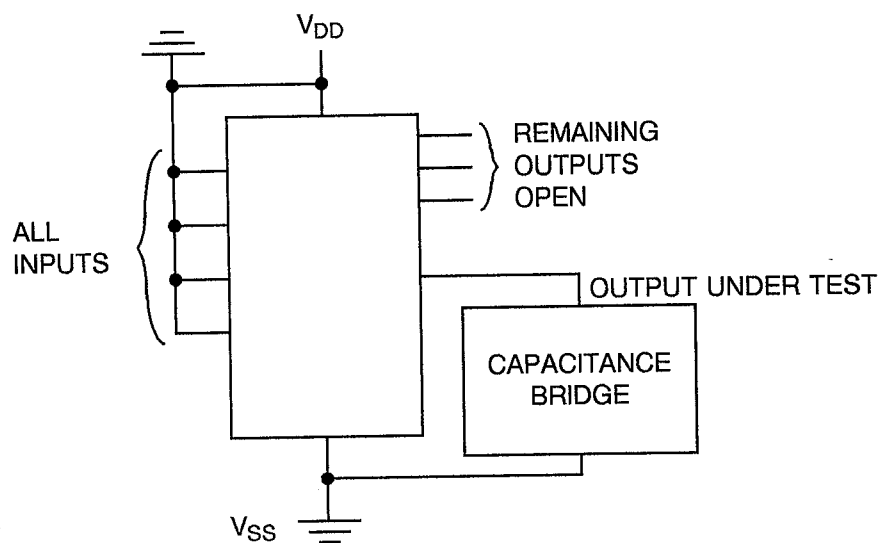
FIGURE 4(h) - INPUT CAPACITANCE



NOTES

1. Each input to be tested separately.
2. $f = 100\text{kHz}$ to 1MHz .

FIGURE 4(i) - OUTPUT CAPACITANCE



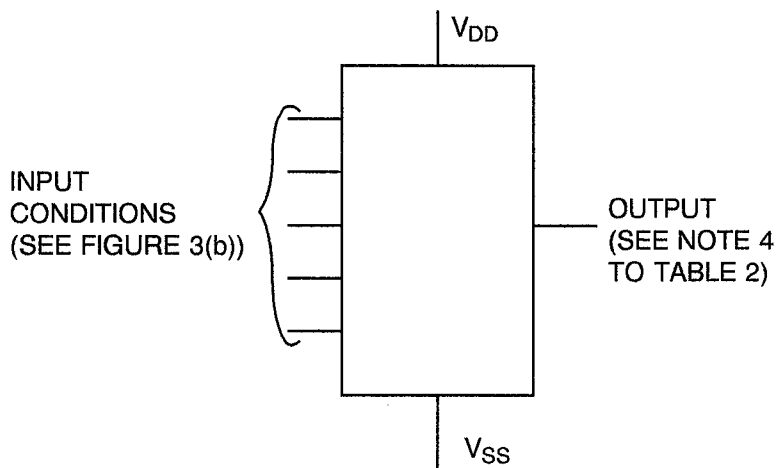
NOTES

1. Each output to be tested separately.
2. $f = 100\text{kHz}$ to 1MHz .



FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(i) - PROPAGATION DELAY



VOLTAGE WAVEFORMS

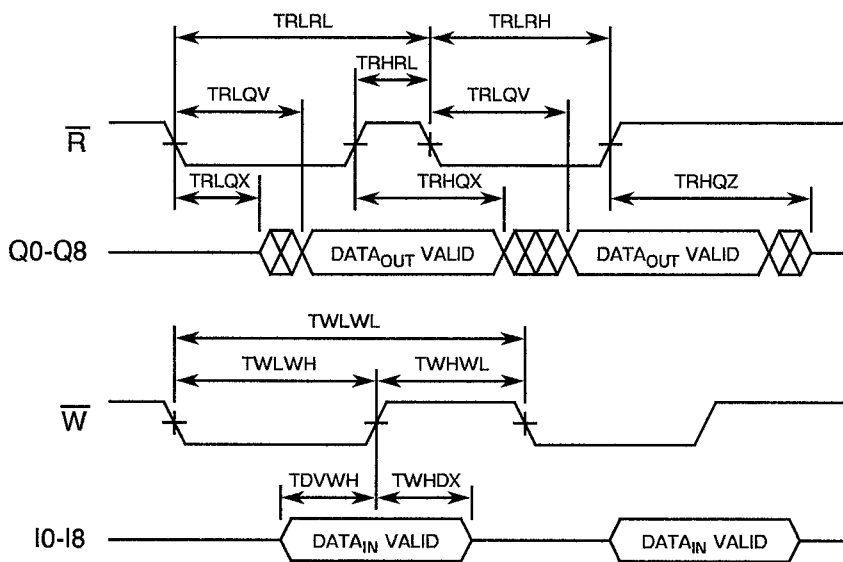
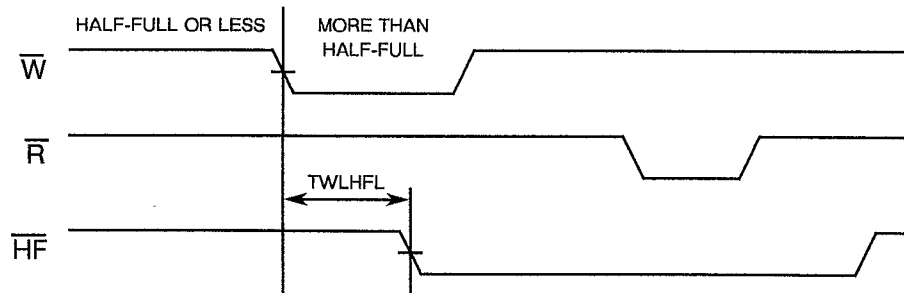
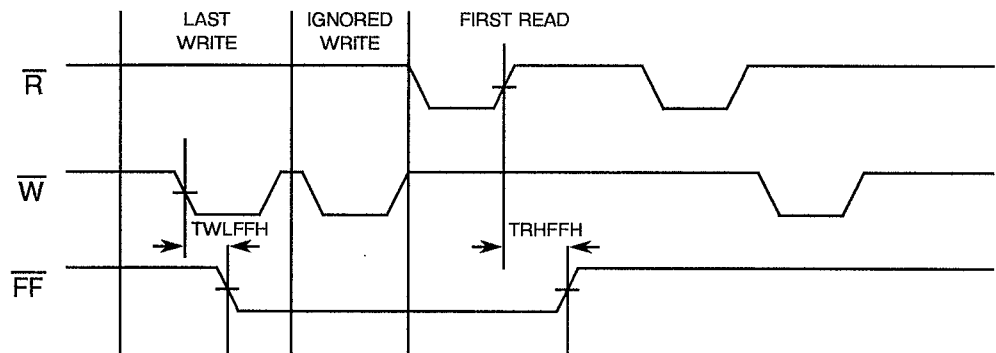
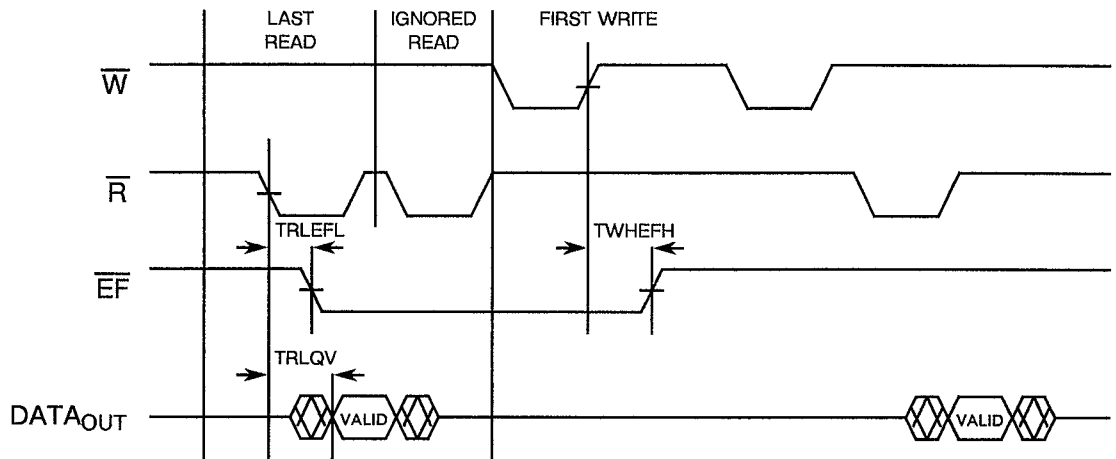




FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(j) - PROPAGATION DELAY (CONTINUED)

VOLTAGE WAVEFORMS (CONTINUED)



**TABLE 4 - PARAMETER DRIFT VALUES**

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	CHANGE LIMITS (Δ)	UNIT
41 to 54	Input Current Low Level	I_{IL}	As per Table 2	As per Table 2	± 100	nA
55 to 68	Input Current High Level	I_{IH}	As per Table 2	As per Table 2	± 100	nA
69 to 80	Output Voltage Low Level	V_{OL}	As per Table 2	As per Table 2	± 100	mV
81 to 92	Output Voltage High Level	V_{OH}	As per Table 2	As per Table 2	± 100	mV
107 to 115	Output Leakage Current Third State (Low Level Applied)	I_{OZL}	As per Table 2	As per Table 2	± 100	nA
116 to 124	Output Leakage Current Third State (High Level Applied)	I_{OZH}	As per Table 2	As per Table 2	± 100	nA
126	Supply Current (Standby)	I_{DD2}	As per Table 2	As per Table 2	± 150	μ A
127	Supply Current (Power Down)	I_{DD3}	As per Table 2	As per Table 2	± 8.0	μ A



TABLE 5(a) - CONDITIONS FOR HIGH TEMPERATURE REVERSE BIAS BURN-IN

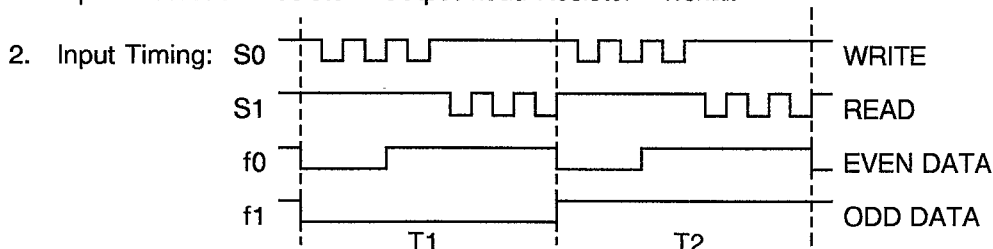
Not applicable.

TABLE 5(b) - CONDITIONS FOR POWER BURN-IN AND OPERATING LIFE TESTS

No.	CHARACTERISTICS	SYMBOL	CONDITION	UNIT
1	Ambient Temperature	T_{amb}	+125(+0-5)	°C
2	Outputs - (Pins D/F 8-9-10-11-12-13-16-17-18-19-20-21) - (Pins C 9-10-11-13-14-15-19-20-21-22-23-24)	V_{OUT}	V_{SS}	V
3	Inputs - (Pins D/F 22-23) - (Pins C 25-26)	V_{IN}	V_{DD}	V
4	Input - (Pin D/F 7) - (Pin C 8)	V_{IN}	V_{SS}	V
5	Input - (Pin D/F 1) - (Pin C 2)	V_{IN}	S0 (Note 2)	Vac
6	Input - (Pin D/F 15) - (Pin C 18)	V_{IN}	S1 (Note 2)	Vac
7	Inputs - (Pins D/F 2-4-6-25-27) - (Pins C 3-5-7-29-31)	V_{IN}	f0 (Note 2)	Vac
8	Inputs - (Pins D/F 3-5-24-26) - (Pins C 4-6-28-30)	V_{IN}	f1 (Note 2)	Vac
9	Pulse Voltage	V_{GEN}	0V to V_{DD}	Vac
10	Pulse Frequency Square Wave	f0 f1	275k ± 20% 137.5k ± 20% 50 ± 15% Duty Cycle	Hz
11	Positive Supply Voltage (Pin D/F 28) (Pin C 32)	V_{DD}	5.0(+0.5-0)	V
12	Negative Supply Voltage (Pin D/F 14) (Pin C 16)	V_{SS}	0	V

NOTES

1. Input Protection Resistor = Output Load Resistor = 1.0kΩ.



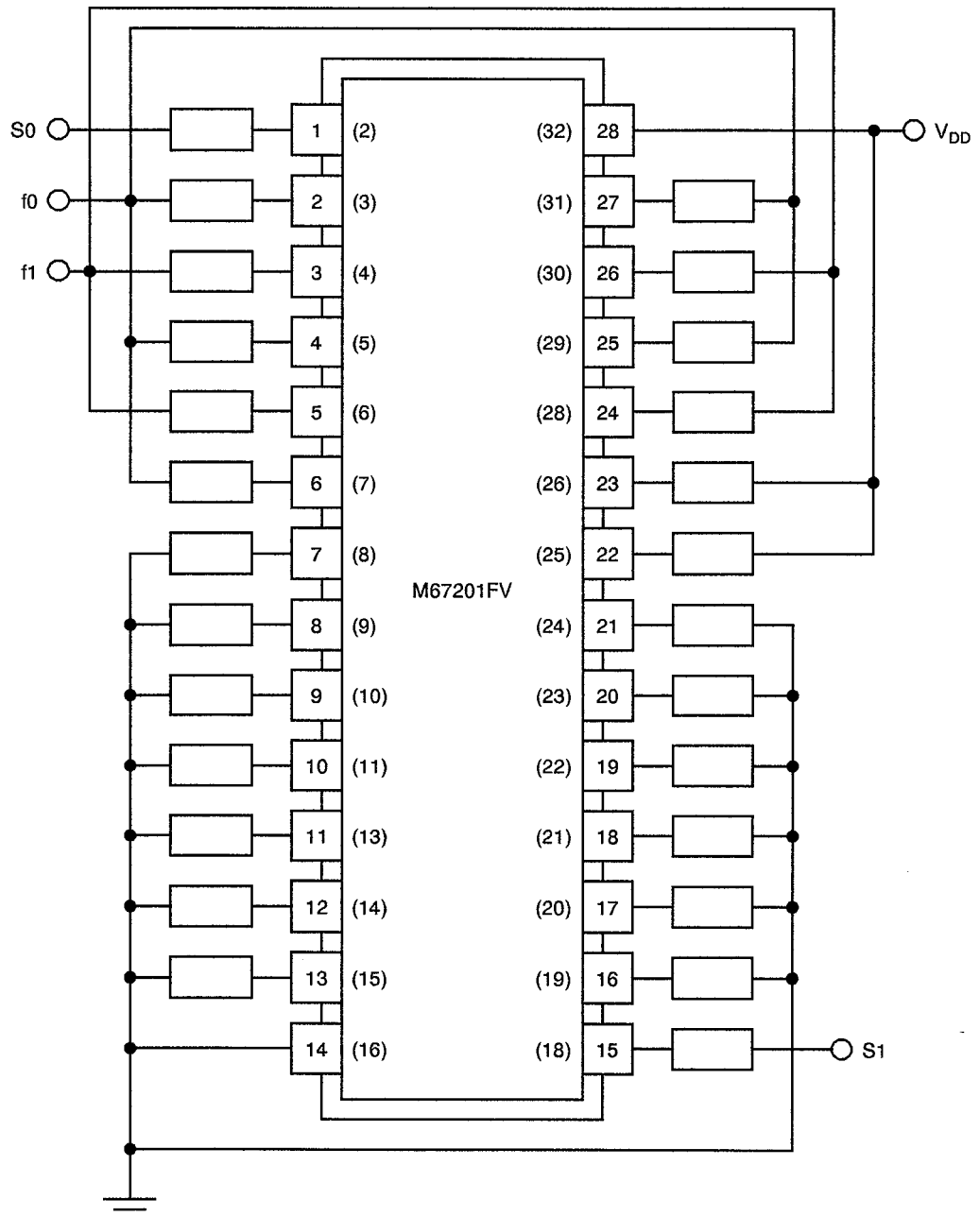
T1 = T2 = 3.6µs.



FIGURE 5(a) - ELECTRICAL CIRCUIT FOR HIGH TEMPERATURE REVERSE BIAS BURN-IN

Not applicable.

FIGURE 5(b) - ELECTRICAL CIRCUIT FOR POWER BURN-IN AND OPERATING LIFE TESTS



NOTES

1. Pin numbers in parenthesis are for the chip carrier package.



- 4.8 ENVIRONMENTAL AND ENDURANCE TESTS (CHARTS IV AND V OF ESA/SCC GENERIC SPECIFICATION No. 9000)
- 4.8.1 Electrical Measurements on Completion of Environmental Tests
The parameters to be measured on completion of environmental tests are scheduled in Table 6. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +22 \pm 3 \text{ }^\circ\text{C}$.
- 4.8.2 Electrical Measurements at Intermediate Points during Endurance Tests
The parameters to be measured at intermediate points during endurance testing are as scheduled in Table 6 of this specification. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +22 \pm 3 \text{ }^\circ\text{C}$.
- 4.8.3 Electrical Measurements on Completion of Endurance Tests
The parameters to be measured on completion of endurance testing are as scheduled in Table 6 of this specification. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +22 \pm 3 \text{ }^\circ\text{C}$.
- 4.8.4 Conditions for Operating Life Tests
The requirements for operating life testing are specified in Section 9 of ESA/SCC Generic Specification No. 9000. The conditions for operating life testing shall be as specified in Table 5(b) of this specification.
- 4.8.5 Electrical Circuits for Operating Life Tests
Circuits for use in performing the operating life tests are shown in Figure 5(b) of this specification.
- 4.8.6 Conditions for High Temperature Storage Test
The requirements for the high temperature storage test are specified in ESA/SCC Generic Specification No. 9000. The temperature to be applied shall be the maximum storage temperature specified in Table 1(b) of this specification.
- 4.9 TOTAL DOSE IRRADIATION TESTING
- 4.9.1 Application
If specified in Para. 4.2.1 of this specification, total dose irradiation testing shall be performed in accordance with the requirements of ESA/SCC Basic Specification No. 22900.
- 4.9.2 Bias Conditions
Continuous bias shall be applied during irradiation testing as shown in Figure 6 of this specification.
- 4.9.3 Electrical Measurements
The parameters to be measured prior to irradiation exposure are scheduled in Table 2 of this specification. Only devices which meet the requirements of Table 2 shall be included in the test sample.

The parameters to be measured during and on completion of irradiation testing are scheduled in Table 7 of this specification.

**TABLE 6 - ELECTRICAL MEASUREMENTS ON COMPLETION OF ENVIRONMENTAL TESTS AND AT INTERMEDIATE POINTS AND ON COMPLETION OF ENDURANCE TESTING**

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	CHANGE LIMITS (Δ)	ABSOLUTE LIMITS		UNIT
						MIN	MAX	
1 to 26	Functional Test 1 (Nominal Inputs)	-	As per Table 2	As per Table 2	-	-	-	-
27 to 38	Functional Test 2 (Worst Case Inputs)	-	As per Table 2	As per Table 2	-	-	-	-
39 to 40	Functional Test 3 (Worst Case Outputs)	-	As per Table 2	As per Table 2	-	-	-	-
41 to 54	Input Current Low Level	I_{IL}	As per Table 2	As per Table 2	± 0.1	-	-1.0	μA
55 to 68	Input Current High Level	I_{IH}	As per Table 2	As per Table 2	± 0.1	-	1.0	μA
69 to 80	Output Voltage Low Level	V_{OL}	As per Table 2	As per Table 2	± 0.1	-	0.4	V
81 to 92	Output Voltage High Level	V_{OH}	As per Table 2	As per Table 2	± 0.1	2.4	-	V
93 to 106	Input Clamp Voltage (to V_{SS})	V_{IC}	As per Table 2	As per Table 2	-	-0.1	-1.9	V
107 to 115	Output Leakage Current Third State (Low Level Applied)	I_{OZL}	As per Table 2	As per Table 2	± 0.1	-	-1.0	μA
116 to 124	Output Leakage Current Third State (High Level Applied)	I_{OZH}	As per Table 2	As per Table 2	± 0.1	-	1.0	μA
125	Supply Current (Operating)	I_{DD1}	As per Table 2	As per Table 2 Variants 1 to 3 Variants 4 to 6 Variants 7 to 9	- - -	- - -	140 120 100	mA
126	Supply Current (Standby)	I_{DD2}	As per Table 2	As per Table 2	± 0.15	-	1.5	mA
127	Supply Current (Power Down)	I_{DD3}	As per Table 2	As per Table 2	± 8.0	-	80	μA

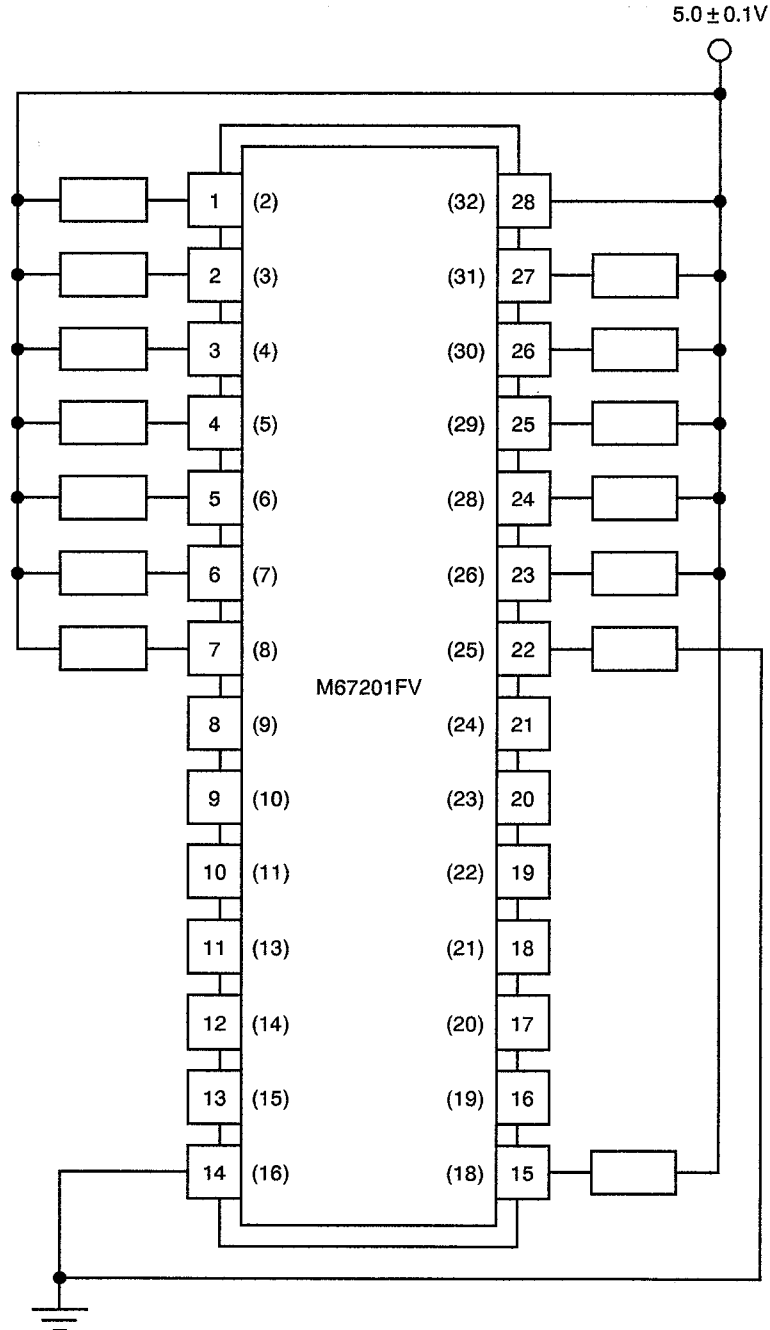


TABLE 6 - ELECTRICAL MEASUREMENTS ON COMPLETION OF ENVIRONMENTAL TESTS AND AT INTERMEDIATE POINTS AND ON COMPLETION OF ENDURANCE TESTING (CONT'D)

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	ABSOLUTE LIMITS		UNIT
					MIN	MAX	
166 to 181	Functional Test 4 (Nominal Inputs)	-	As per Table 2	As per Table 2	-	-	-
182 to 183	Read Cycle Time	TRLRL	As per Table 2	As per Table 2 Variants 1 to 3 Variants 4 to 6 Variants 7 to 9	40 50 65	- - -	ns
184 to 185	Access Time	TRLQV	As per Table 2	As per Table 2 Variants 1 to 3 Variants 4 to 6 Variants 7 to 9	- - -	30 40 50	ns
186 to 187	Data Set-up Time	TDVWH	As per Table 2	As per Table 2 Variants 1 to 3 Variants 4 to 6 Variants 7 to 9	18 20 30	- - -	ns
188 to 189	Data Hold Time	TWHDX	As per Table 2	As per Table 2 Variants 1 to 3 Variants 4 to 6 Variants 7 to 9	0 0 5.0	- - -	ns
190 to 191	Read Low to Empty Flag Low	TRLEFL	As per Table 2	As per Table 2 Variants 1 to 3 Variants 4 to 6 Variants 7 to 9	- - -	30 30 45	ns
192 to 193	Write High to Empty Flag High	TWHEFH	As per Table 2	As per Table 2 Variants 1 to 3 Variants 4 to 6 Variants 7 to 9	- - -	30 35 45	ns
194 to 195	Read High to Full Flag High	TRHFFH	As per Table 2	As per Table 2 Variants 1 to 3 Variants 4 to 6 Variants 7 to 9	- - -	30 35 45	ns
196 to 197	Write Low to Full Flag Low	TWLFFL	As per Table 2	As per Table 2 Variants 1 to 3 Variants 4 to 6 Variants 7 to 9	- - -	30 35 45	ns
198 to 199	Write Low to Half Full Flag Low	TWLHFL	As per Table 2	As per Table 2 Variants 1 to 3 Variants 4 to 6 Variants 7 to 9	- - -	40 50 60	ns



FIGURE 6 - BIAS CONDITIONS FOR IRRADIATION TESTING



NOTES

1. Input Protection Resistor = 1.0kΩ.
2. Pin numbers in parenthesis are for the chip carrier package.

**TABLE 7 - ELECTRICAL MEASUREMENTS DURING AND ON COMPLETION OF IRRADIATION TESTING**

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	ABSOLUTE LIMITS		UNIT
					MIN	MAX	
1 to 26	Functional Test 1 (Nominal Inputs)	-	As per Table 2	As per Table 2	-	-	-
41 to 54	Input Current Low Level	I_{IL}	As per Table 2	As per Table 2	-	-5.0	μA
55 to 68	Input Current High Level	I_{IH}	As per Table 2	As per Table 2	-	5.0	μA
69 to 80	Output Voltage Low Level	V_{OL}	As per Table 2	As per Table 2	-	0.4	V
81 to 92	Output Voltage High Level	V_{OH}	As per Table 2	As per Table 2	2.4	-	V
107 to 115	Output Leakage Current Third State (Low Level Applied)	I_{OZL}	As per Table 2	As per Table 2	-	-5.0	μA
116 to 124	Output Leakage Current Third State (High Level Applied)	I_{OZH}	As per Table 2	As per Table 2	-	5.0	μA
127	Supply Current (Power Down)	I_{DD3}	As per Table 2	As per Table 2	-	5.0	mA



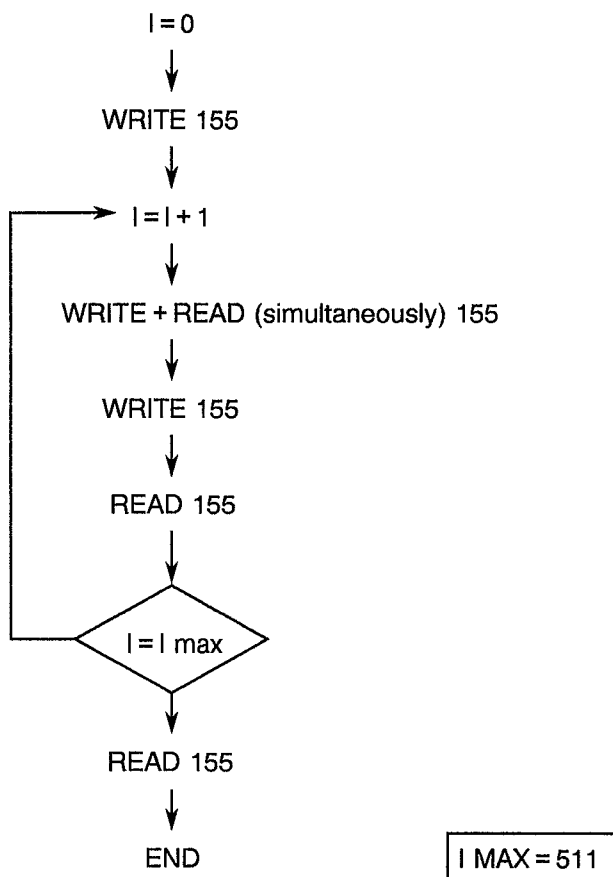
APPENDIX 'A'

AGREED DEVIATIONS FOR MATRA-MHS (F)

ITEMS AFFECTED	DESCRIPTION OF DEVIATIONS
Para. 4.2.2	Para. 9.9.3, "Electrical Measurements at Room Temperature". May be performed at High Temperature.
Para. 4.2.4 and 4.2.5	Para. 9.9.4, "Electrical Measurements at Room Temperature". May be performed in accordance with Table 2, but Parameter Drift Values must be calculated in accordance with Table 6 of this specification

The following test patterns may be used:-

1. ICCACT Pattern



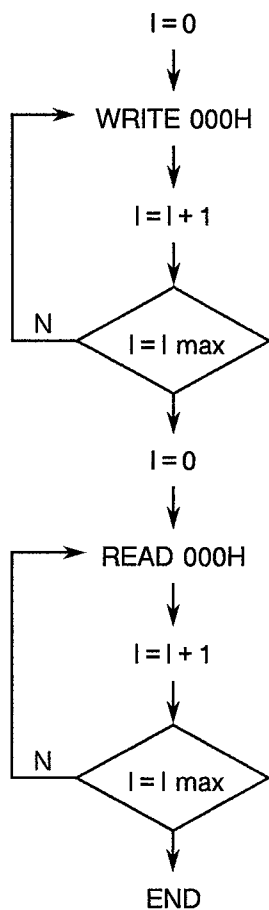
2. FLAG TEST

March pattern with control of flags.



APPENDIX 'A'

3. WRT-RD 000
WRT-RD 1FF

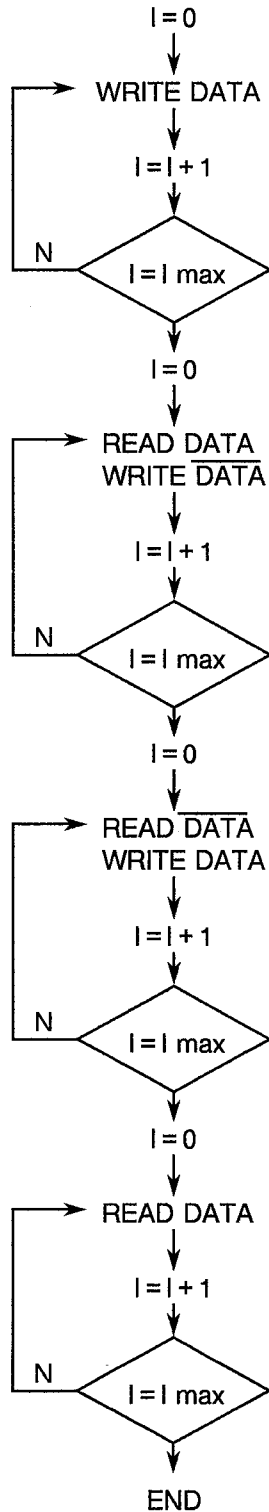


MEMORY SIZE	= 512
DATA	= 000 or 1FF
I MAX	= 511



APPENDIX 'A'

- 4. MARCH-000
- MARCH-155
- MARCH-1FF

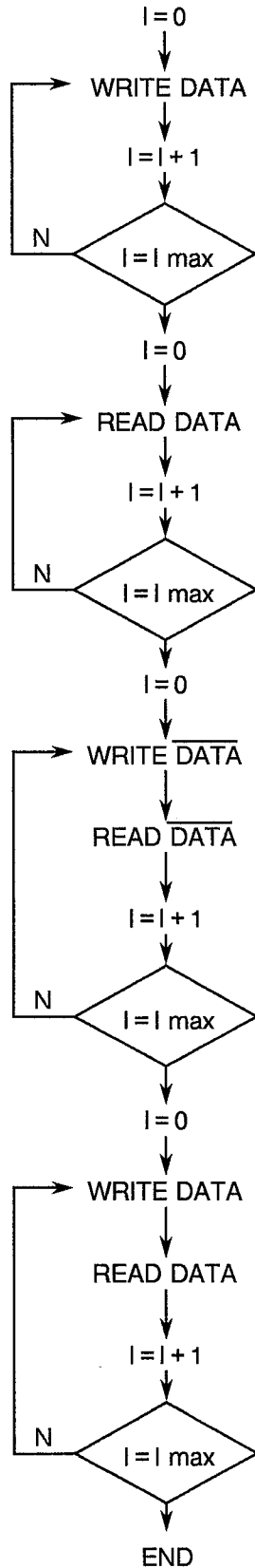


MEMORY SIZE	= 512
DATA	= 000 or 155 or 1FF
I MAX	= 511



APPENDIX 'A'

- 5. FIFO-000
- FIFO-155
- FIFO-1FF

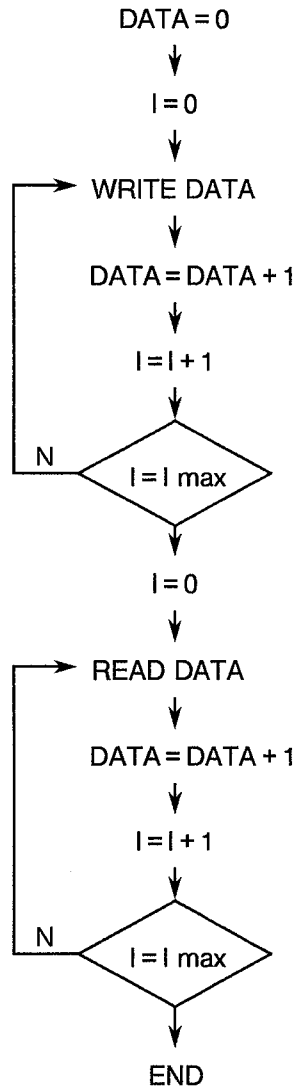


MEMORY SIZE	= 512
DATA	= 000 or 155 or 1FF
I MAX	= 511



APPENDIX 'A'

6. ADDRESS

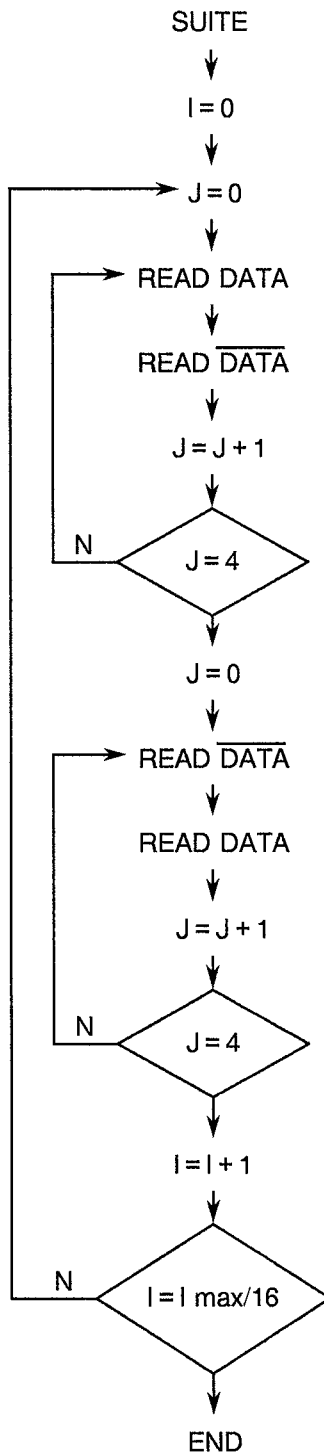
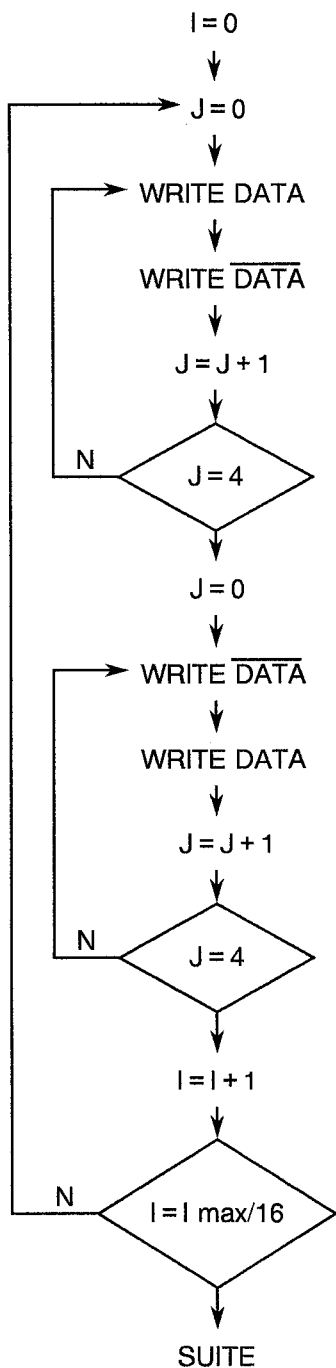


MEMORY SIZE = 512
I MAX = 511



APPENDIX 'A'

7. CKBD-000
CKBD-1FF



MEMORY SIZE	= 512
DATA	= 000 or 1FF
I MAX	= 511



APPENDIX 'A'

8. Xi PATTERN ALGORITHM

