INTEGRATED CIRCUITS, SILICON MONOLITHIC,

HIGH EFFICENCY LINEAR REGULATOR,

BASED ON TYPE UC1834

ESCC Detail Specification No. 9102/013

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Pages 1 to 50

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space components
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TABLE OF CONTENTS

Page

TABLES

FIGURES

APPENDICES (Applicable to specific Manufacturers only)

1. GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics, test and inspection data for a silicon monolithic, High Efficiency Linear Regulator, based on Type UC1834. It shall be read in conjunction with ESA/SCC Generic Specification No. 9000, the requirements of which are supplemented herein.

1.2 COMPONENT TYPE VARIANTS

Variants of the basic type integrated circuits specified herein, which are also covered by this specification, are given in Table 1(a).

1.3 MAXIMUM RATINGS

The maximum ratings, which shall not be exceeded at any time during use or storage, applicable to the integrated circuits specified herein, are as scheduled in Table 1(b).

1.4 PARAMETER DERATING INFORMATION

The parameter derating information of the integrated circuits specified herein is shown in Figure 1.

1.5 PHYSICAL DIMENSIONS

The physical dimensions of the integrated circuits specified herein are shown in Figure 2.

1.6 PIN ASSIGNMENT

As per Figure 3(a).

1.7 TRUTH TABLE (FIGURE 3(b))

Not applicable.

1.8 CIRCUIT SCHEMATIC (FIGURE 3(c))

Not applicable.

1.9 FUNCTIONAL DIAGRAM

As per Figure 3(d).

1.10 HANDLING PRECAUTIONS

These devices are susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacture, testing, packaging, shipment and any handling.

These components are categorised as Class 2 with a Minimum Critical Path Failure Voltage of 2000 Volts.

TABLE 1(a) - TYPE VARIANTS

VARIANT	CASE	FIGURE	LEAD MATERIAL AND/OR FINISH
01	D.I.L.	2(a)	G4
02	CHIP CARRIER	2(b)	7
03	CHIP CARRIER	2(b)	4

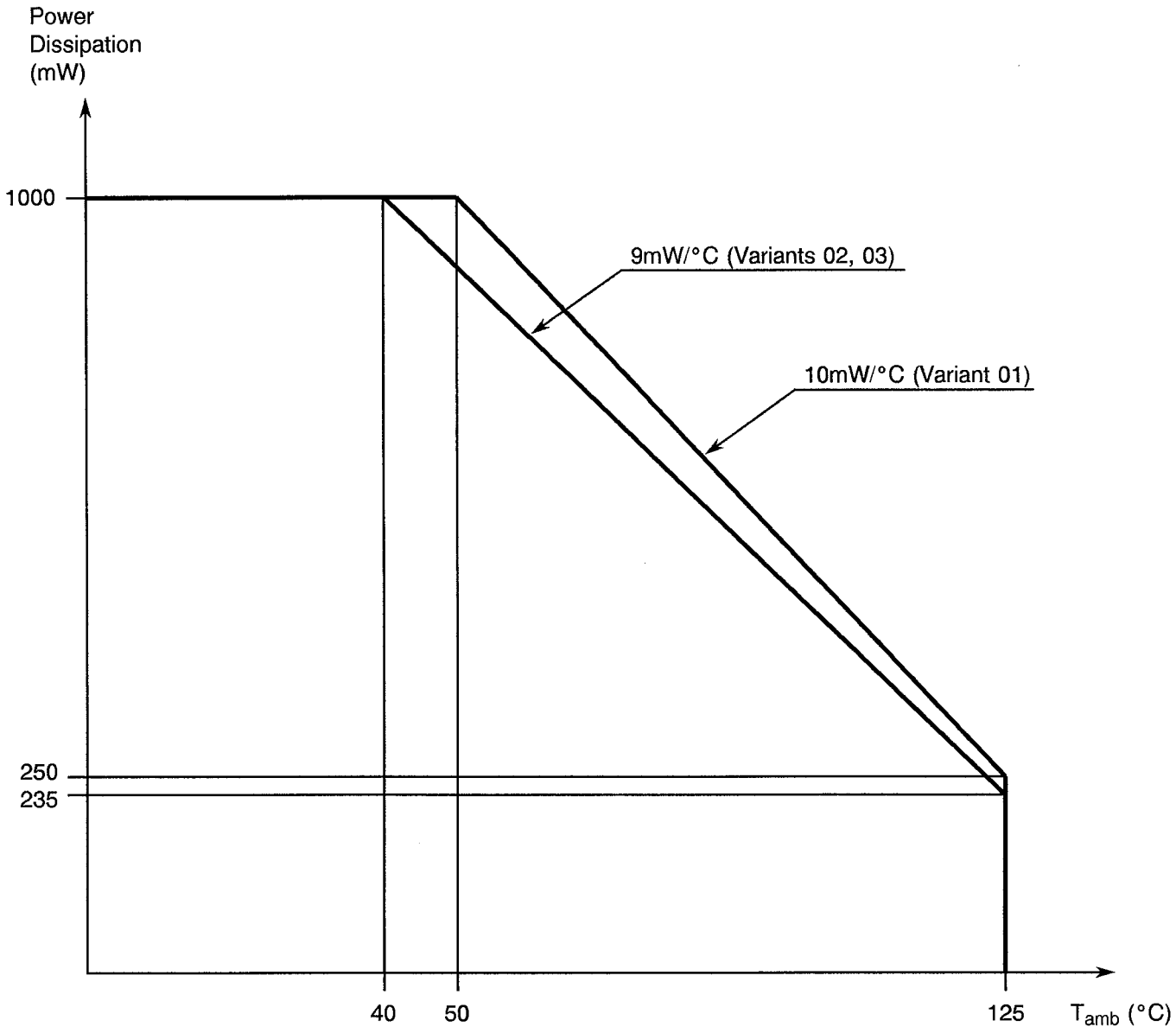
TABLE 1(b) - MAXIMUM RATINGS

No.	CHARACTERISTICS	SYMBOL	MAXIMUM RATINGS	UNIT	REMARKS
1	Input Supply Voltage	V_{IN+}	40	V	Note 1
2	Driver Source to Sink Voltage	V_{DSS}	40	V	Note 1
3	Fault Alert Voltage	V_{FA}	40	V	Note 1
4	Driver Current	I_D	400	mA	Note 2
5	Crowbar Current	I_{OCr}	−200	mA	Note 2
6	+1.5V Reference Current	I_{ORef}	−10	mA	Note 2
7	Fault Alert Current	I_{FA}	15	mA	Note 2
8	Device Power Dissipation (Continuous)	P_D	1.0	W	Note 3
9	Operating Temperature Range	T_{op}	−55 to +125	°C	T_{amb}
10	Storage Temperature Range	T_{stg}	−65 to +150	°C	-
11	Soldering Temperature For DIL For CCP	T_{sol}	 +265 +245	°C	 Note 4 Note 5
12	Junction Temperature	T_J	+150	°C	-
13	Thermal Resistance For DIL For CCP	$R_{TH(J-C)}$	 60 30	°C/W	-

NOTES

1. Voltages are referenced to V_{IN}.
2. Currents are positive into, negative out of the specified terminals.
3. At $T_{amb} \leq +50°C$ for Variant 01 and +40°C for Variants 02 and 03. For derating at $T_{amb} > +50°C$ and +40°C, see Figure 1.
4. Duration 10 seconds maximum at a distance of not less than 1.5mm from the device body and the same lead shall not be resoldered until 3 minutes have elapsed.
5. Duration 5 seconds maximum and the same terminal shall not be resoldered until 3 minutes have elapsed.

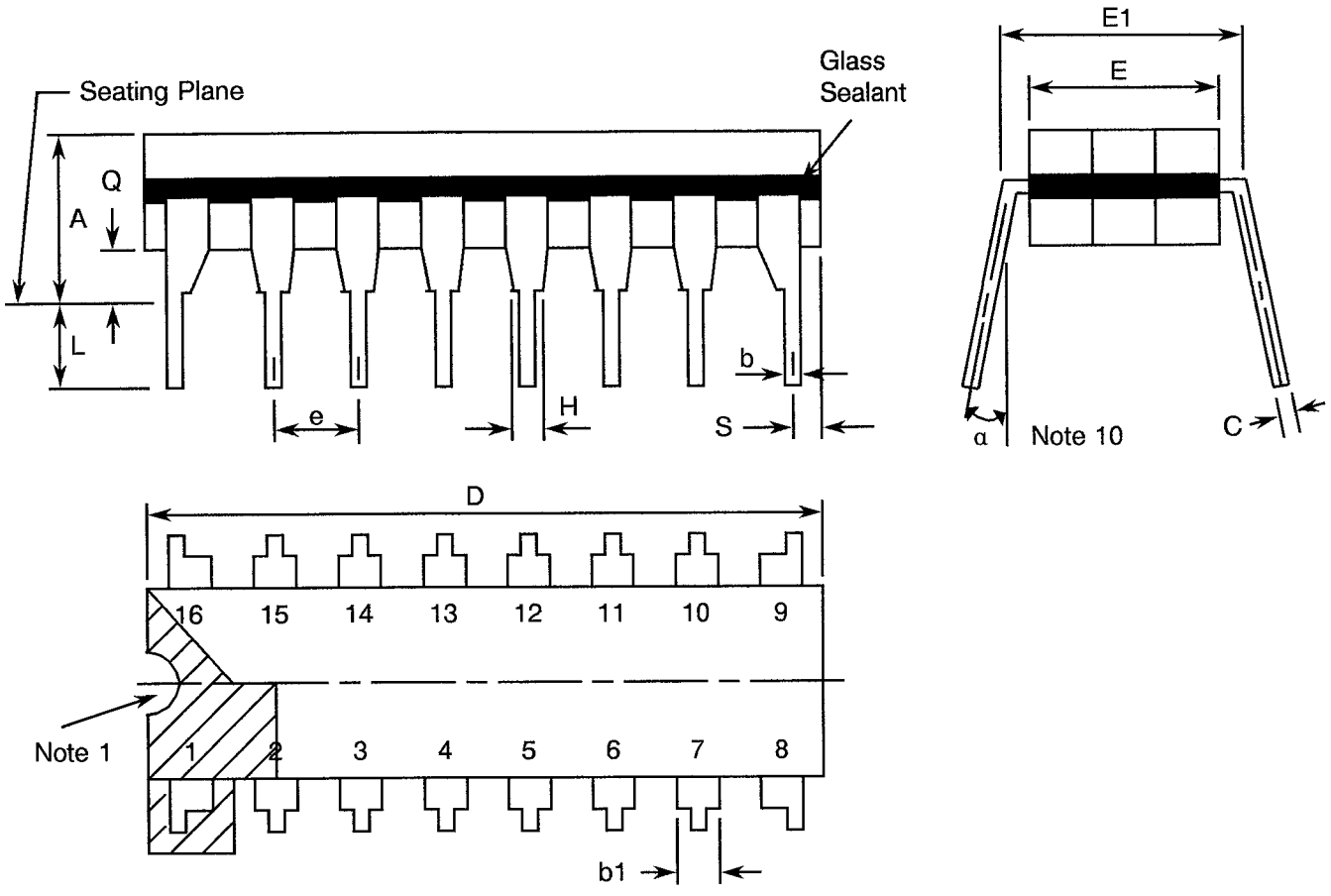
FIGURE 1 - PARAMETER DERATING INFORMATION



Power Dissipation versus Temperature

FIGURE 2 - PHYSICAL DIMENSIONS

FIGURE 2(a) - DUAL-IN-LINE PACKAGE, 16-PIN

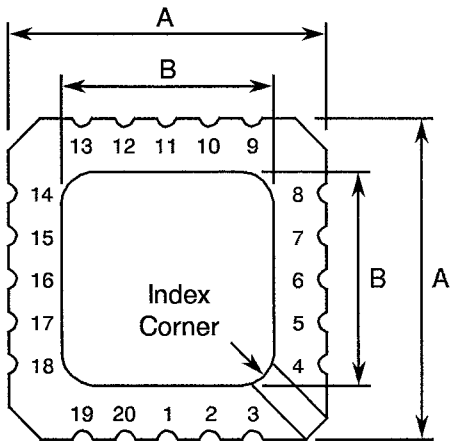


SYMBOL	MILLIMETRES		NOTES
	MIN	MAX	
A	-	5.08	-
b	0.38	0.66	8
b1	-	1.78	8
C	0.20	0.44	8
D	-	21.34	4
E	5.59	7.87	4
E1	7.37	8.13	-
e	2.54 TYPICAL		6, 9
H	0.76	-	-
L	3.18	5.08	8
Q	0.38	-	3
S	0.127	-	7
α	0°	15°	10

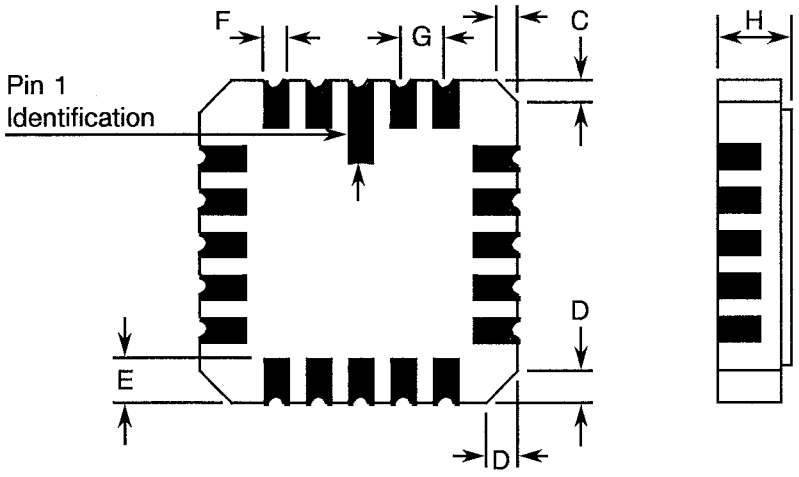
NOTES: See Page 10.

FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)

FIGURE 2(b) - CHIP CARRIER PACKAGE, 20 TERMINAL



20 Terminal



SYMBOL	MILLIMETRES		NOTES
	MIN.	MAX.	
A	8.69	9.09	-
B	7.80	9.09	-
C	0.25	0.51	11
D	0.89	1.14	12
E	1.14	1.40	8
F	0.56	0.71	8
G	1.27 TYPICAL		5, 9
H	1.63	2.54	-

NOTES: See Page 10.

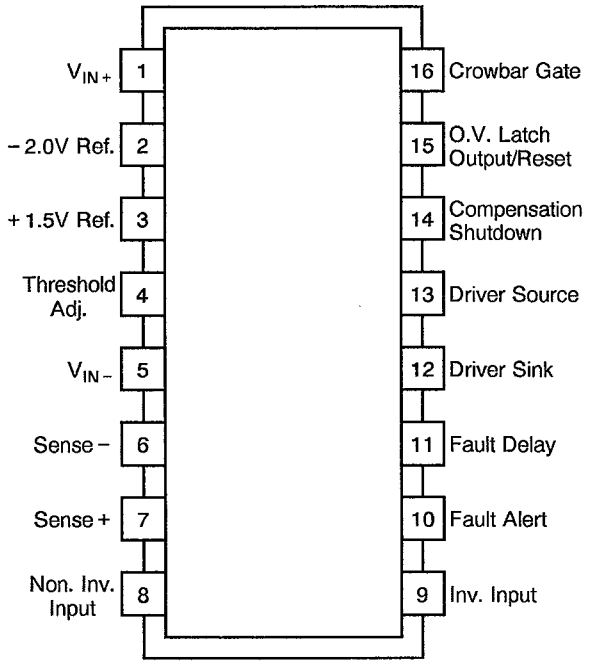
FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)

NOTES TO FIGURES 2(a) TO 2(b) INCLUSIVE

1. Index area: a notch or dot shall be located adjacent to Pin 1 and shall be within the shaded area shown. For chip carrier packages, the index shall be as shown in Figure 2(b).
2. Not applicable.
3. The dimension shall be measured from the seating plane to the base plane.
4. This dimension allows for off-centre lids, meniscus and glass overrun.
5. The true position pin or terminal spacing is 1.27mm between centrelines. Each pin centreline shall be located within ±0.13mm of its true longitudinal position relative to Pins 1 and the highest pin number.
6. The true position pin spacing is 2.54mm between centrelines. Each pin centreline shall be located within ±0.25mm of its true longitudinal position relative to Pins 1 and the highest pin number.
7. Applies to all 4 corners.
8. All leads or terminals.
9. 14 spaces for dual-in-line packages.
   16 spaces for chip carrier packages.
10. Lead centre when α is 0°.
11. 3 non-index corners - 6 dimensions.
12. Index corner only - 2 dimensions.

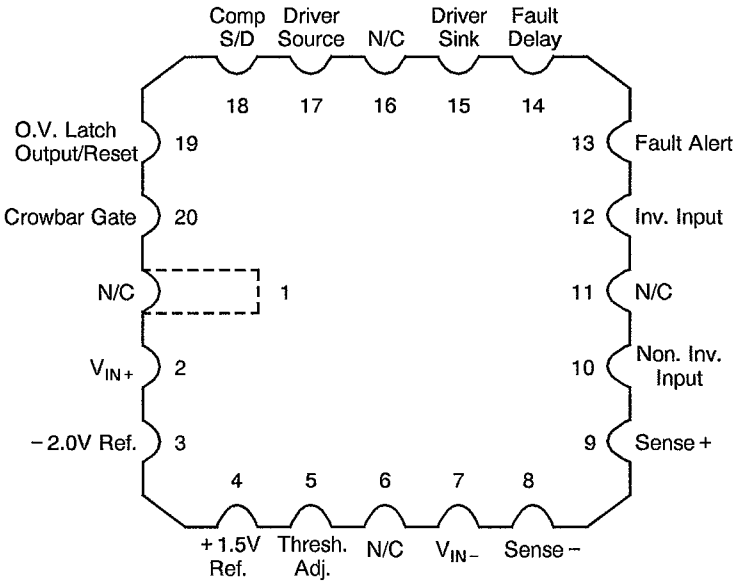
FIGURE 3(a) - PIN ASSIGNMENT

DUAL-IN-LINE PACKAGE



(TOP VIEW)

CHIP CARRIER PACKAGE



(TOP VIEW)

DUAL-IN-LINE TO CHIP CARRIER PIN ASSIGNMENT

DUAL-IN-LINE PIN OUTS	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
CHIP CARRIER PIN OUTS	2	3	4	5	7	8	9	10	12	13	14	15	17	18	19	20

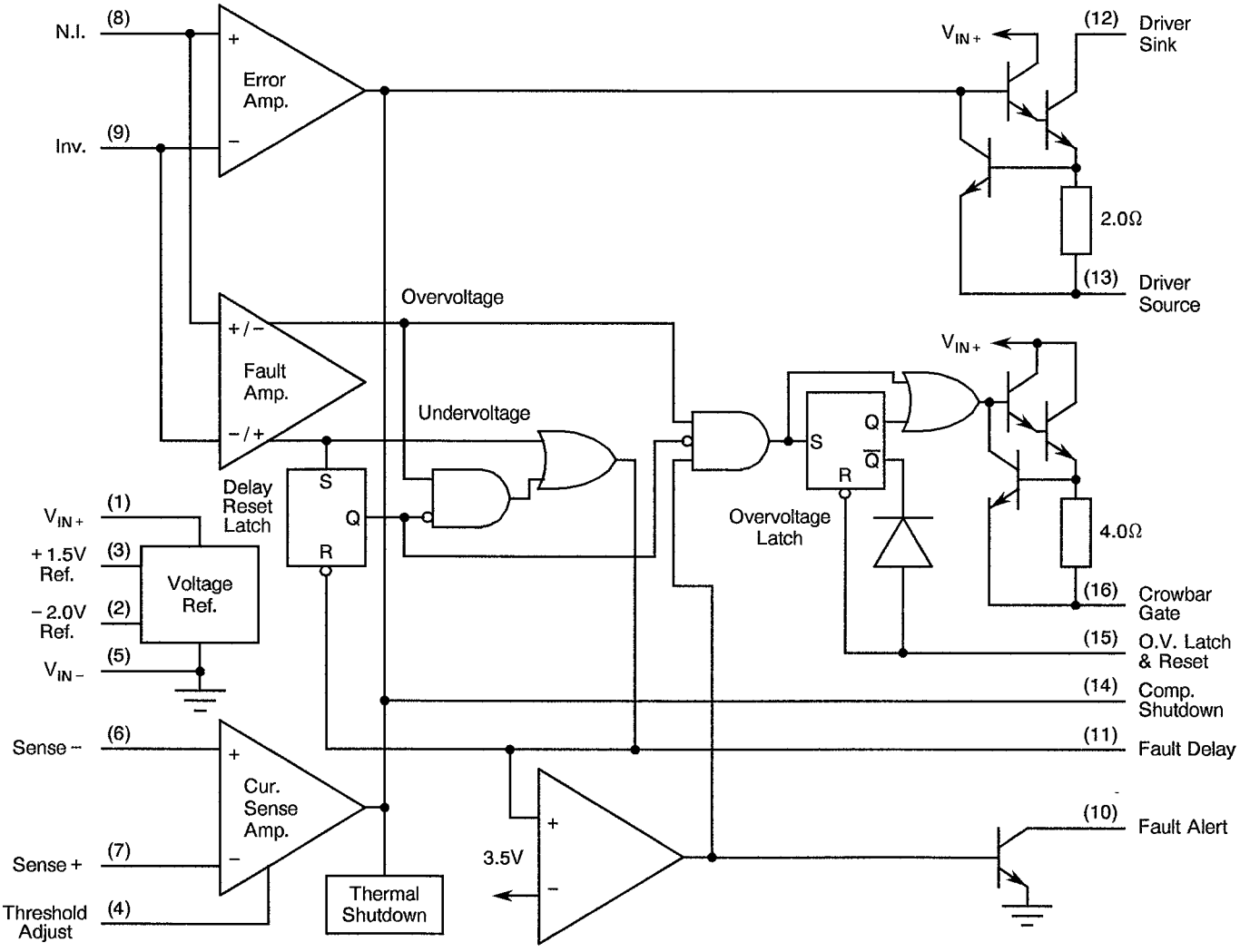
FIGURE 3(b) - TRUTH TABLE

Not applicable.

FIGURE 3(c) - CIRCUIT SCHEMATIC

Not applicable.

FIGURE 3(d) - FUNCTIONAL DIAGRAM



NOTES

1. DIL package references only are given.

2. APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:-

(a) ESA/SCC Generic Specification No. 9000 for Integrated Circuits.

(b) MIL-STD-883, Test Methods and Procedures for Micro-electronics.

3. TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESA/SCC Basic Specification No. 21300 shall apply. In addition, the following abbreviations are used:-

V_{IN+} = Supply Voltage.

4. REQUIREMENTS

4.1 GENERAL

The complete requirements for procurement of the integrated circuits specified herein are stated in this specification and ESA/SCC Generic Specification No. 9000 for Integrated Circuits. Deviations from the Generic Specification applicable to this specification only, are listed in Para. 4.2.

Deviations from the applicable Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESA/SCC requirements and do not affect the components' reliability, are listed in the appendices attached to this specification.

4.2 DEVIATIONS FROM GENERIC SPECIFICATION

4.2.1 Deviations from Special In-process Controls

None.

4.2.2 Deviations from Final Production Tests (Chart II)

None.

4.2.3 Deviations from Burn-in and Electrical Measurements (Chart III)

(a) Para. 7.1.1(a), "High Temperature Reverse Bias" tests and subsequent electrical measurements related to this test shall be omitted.

4.2.4 Deviations from Qualification Tests (Chart IV)

None.

4.2.5 Deviations from Lot Acceptance Tests (Chart V)

None.

4.3 MECHANICAL REQUIREMENTS

4.3.1 Dimension Check

The dimensions of the integrated circuits specified herein shall be checked. They shall conform to those shown in Figure 2.

4.3.2 Weight

The maximum weight of the integrated circuits specified herein shall be 3.0 grammes for the dual-in-line package and 2.5 grammes for the chip carrier package.

4.4 MATERIALS AND FINISHES

The materials and finishes shall be as specified herein. Where a definite material is not specified, a material which will enable the integrated circuits specified herein to meet the performance requirements of this specification shall be used. Acceptance or approval of any constituent material does not guarantee acceptance of the finished product.

4.4.1 Case

The case shall be hermetically sealed and have a ceramic body and the lids shall be welded, brazed or preform-soldered or glass frit-sealed.

4.4.2 Lead Material and Finish

For dual-in-line packages, the lead material shall be Type 'G' with Type '4' finish in accordance with the requirements of ESA/SCC Basic Specification No. 23500. For chip carrier packages, the finish shall be Type '4' or Type '7' in accordance with the requirements of ESA/SCC Basic Specification No. 23500.

4.5 MARKING

4.5.1 General

The marking of components delivered to this specification shall be in accordance with the requirements of ESA/SCC Basic Specification No. 21700 and the following paragraphs. When the component is too small to accommodate all of the marking as specified, as much as space permits shall be marked and the marking information, in full, shall accompany the component in its primary package.

The information to be marked and the order of precedence, shall be as follows:-

(a) Lead Identification.

(b) The SCC Component Number.

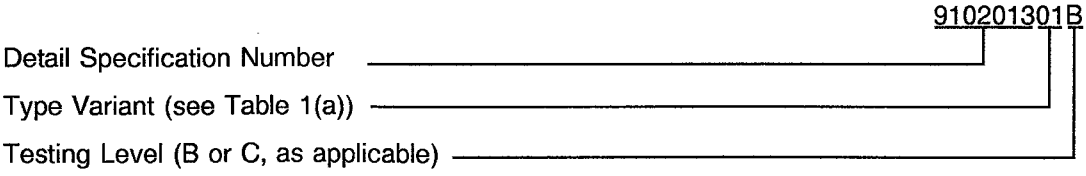
(c) Traceability Information.

4.5.2 Lead Identification

For dual-in-line packages, an index shall be located at the top of the package in the position defined in Note 1 to Figure 2 or, alternatively, a tab may be used to identify Pin No. 1. The pin numbering must be read with the index or tab on the left-hand side. For chip carrier packages, the index shall be as defined by Figure 2(b).

4.5.3 The SCC Component Number

Each component shall bear the SCC Component Number which shall be constituted and marked as follows:



4.5.4 Traceability Information

Each component shall be marked in respect of traceability information in accordance with the requirements of ESA/SCC Basic Specification No. 21700.

4.6 ELECTRICAL MEASUREMENTS

4.6.1 Electrical Measurements at Room Temperature

The parameters to be measured in respect of electrical characteristics are scheduled in Table 2. Unless otherwise specified, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.6.2 Electrical Measurements at High and Low Temperatures

The parameters to be measured at high and low temperatures are scheduled in Table 3. The measurements shall be performed at $T_{amb} = +125(+0-5)$ and $-55(+5-0)$ °C respectively.

4.6.3 Circuits for Electrical Measurements

Circuits for use in performing the electrical measurements listed in Tables 2 and 3 of this specification are shown in Figure 4.

4.7 BURN-IN TESTS

4.7.1 Parameter Drift Values

The parameter drift values applicable to burn-in are specified in Table 4 of this specification. Unless otherwise stated, measurements shall be performed at $T_{amb} = +22 \pm 3$ °C. The parameter drift values (Δ) applicable to the parameters scheduled, shall not be exceeded. In addition to these drift value requirements, the appropriate limit value specified for a given parameter in Table 2 shall not be exceeded.

4.7.2 Conditions for High Temperature Reverse Bias Burn-in (Table 5(a))

Not applicable.

4.7.3 Conditions for Power Burn-in

The requirements for power burn-in are specified in Section 7 of ESA/SCC Generic Specification No. 9000. The conditions for power burn-in shall be as specified in Table 5(b) of this specification.

4.7.4 Electrical Circuits for High Temperature Reverse Bias Burn-in (Figure 5(a))

Not applicable.

4.7.5 Electrical Circuits for Power Burn-in

Circuits for use in performing the power burn-in tests are shown in Figure 5(b) of this specification.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D = DIP, C = CCP)	LIMITS		UNIT
						MIN	MAX	
1	Supply Current (Standby)	I_{CC}	-	4(a)	V_{IN+} = 15V, V_{IN-} = 0V (Pin D 1) (Pin C 2)	-	7.0	mA
2	Output Voltage (Referenced to V_{IN-})	V_{REF1}	-	4(a)	V_{IN+} = 15V, V_{IN-} = 0V (Pin D 3) (Pin C 4)	1.485	1.515	V
3	Line Regulation	K_{LI1}	-	4(a)	V_{IN+} = 5.0V to 35V, V_{IN-} = 0V (Pin D 3) (Pin C 4)	-	10	mV
4	Load Regulation	K_{LO1}	-	4(a)	V_{IN+} = 15V, V_{IN-} = 0V I_{VREF} = 0mA to 2.0mA (Pin D 3) (Pin C 4)	-	10	mV
5	Output Voltage (Referenced to V_{IN+})	V_{REF2}	-	4(b)	V_{IN+} = 15V, V_{IN-} = 0V (Pin D 2) (Pin C 3)	−2.04	−1.96	V
6	Line Regulation	K_{LI2}	-	4(b)	V_{IN+} = 5.0V to 35V, V_{IN-} = 0V (Pin D 3) (Pin C 4)	-	15	mV
7	Input Offset Voltage	V_{IO}	4001	4(c)	V_{IN+} = 15V, V_{IN-} = 0V (Pins D 8-9) (Pins C 10-12)	-	6.0	mV
8 to 9	Input Bias Current	I_{IB}	4001	4(c)	V_{IN+} = 15V, V_{IN-} = 0V (Pins D 8-9) (Pins C 10-12)	−4.0	-	µA
10	Input Offset Current	I_{IO}	4001	4(c)	V_{IN+} = 15V, V_{IN-} = 0V (Pins D 8-9) (Pins C 10-12)	-	1.0	µA
11	Small Signal Open Loop Gain	A_{VOL}	4004	4(d)	V_{IN+} = 15V, V_{IN-} = 0V (Pins D 8-9-14) (Pins C 10-12-18)	50	-	dB
12	Common Mode Rejection Ratio	CMRR	4003	4(e)	V_{IN+} = 15V, V_{IN-} = 0V V_{CM} = 0.5V to 33V (Pins D 8-9-14) (Pins C 10-12-18)	60	-	dB
13	Power Supply Rejection Ratio	PSRR	4003	4(f)	V_{IN+} = 5.0V to 35V, V_{IN-} = 0V V_{CM} = 1.5V (Pins D 8-9-14) (Pins C 10-12-18)	70	-	dB

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D = DIP, C = CCP)	LIMITS		UNIT
						MIN	MAX	
14	Output Current (Maximum)	$I_{OUT(max)}$	-	4(g)	V_{IN+} = 15V, V_{IN-} = 0V (Pins D 12-13) (Pins C 15-17)	200	-	mA
15	Saturation Voltage	V_{SAT}	-	4(h)	V_{IN+} = 15V, V_{IN-} = 0V I_{OUT} = 100mA (Pins D 12-13) (Pins C 15-17)	-	1.2	V
16	Output Leakage Current Low Level	I_{OZL}	-	4(i)	V_{IN+} = 15V, V_{IN-} = 0V (Pins D 12-13) (Pins C 15-17)	-	50	µA
17	Shutdown Input Voltage	V_{SD}	-	4(j)	V_{IN+} = 15V, V_{IN-} = 0V $I_{OUT} \leq$ 100µA (Pin D 14) (Pin C 18)	0.4	-	V
18	Shutdown Input Current	I_{SD}	-	4(i)	V_{IN+} = 15V, V_{IN-} = 0V $I_{OUT} \leq$ 100µA (Pin D 14) (Pin C 18)	− 150	-	µA
19 to 20	Under and Over Voltage Fault Threshold	V_{THUO}	4001	4(k)	V_{IN+} = 15V, V_{IN-} = 0V V_{CM} = 1.5V (Pins D 8-9-11) (Pins C 10-12-14)	120	180	mV
21 to 22	Common Mode Sensitivity	CMS	4003	4(k)	V_{IN+} = 35V, V_{IN-} = 0V V_{CM} = 1.5V to 33V (Pins D 8-9-11) (Pins C 10-12-14)	− 0.8	-	%/V
23 to 24	Supply Voltage Sensitivity	SVS	4003	4(k)	V_{IN+} = 5.0V to 35V, V_{IN-} = 0V V_{CM} = 1.5V (Pins D 8-9-11) (Pins C 10-12-14)	− 1.0	-	%/V
25	Fault Alert Output Current	I_{Fault}	-	4(l)	V_{IN+} = 15V, V_{IN-} = 0V (Pin D 10) (Pin C 13)	2.0	-	mA
26	Fault Alert Saturation Voltage	$V_{SatFault}$	-	4(m)	V_{IN+} = 15V, V_{IN-} = 0V I_{OUT} = 1.0mA (Pin D 10) (Pin C 13)	-	0.5	V
27	Over Voltage Latch Output Current	$I_{OVLatch}$	-	4(n)	V_{IN+} = 15V, V_{IN-} = 0V (Pin D 15) (Pin C 19)	2.0	-	mA

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D = DIP, C = CCP)	LIMITS		UNIT
						MIN	MAX	
28	Over Voltage Latch Output Saturation Voltage	$V_{SatLatch}$	-	4(o)	V_{IN+} = 15V, V_{IN-} = 0V I_{OUT} = 1.0mA (Pin D 15) (Pin C 19)	-	1.3	V
29	Over Voltage Latch Output Reset Voltage	$V_{OVReset}$	-	4(p)	V_{IN+} = 15V, V_{IN-} = 0V (Pin D 15) (Pin C 19)	0.3	0.6	V
30	Crowbar Gate Current	I_{CB}	-	4(q)	V_{IN+} = 15V, V_{IN-} = 0V (Pin D 16) (Pin C 20)	-	−100	mA
31	Crowbar Gate Leakage Current	I_{CBLeak}	-	4(r)	V_{IN+} = 35V, V_{IN-} = 0V (Pin D 16) (Pin C 20)	−50	-	µA
32 to 33	Threshold Voltage 1	V_{TH1}	4001	4(s)	V_{IN+} = 15V, V_{IN-} = 0V V_{CM} = 15V and 0V (Pins D 6-7) (Pins C 8-9)	130	170	mV
34 to 35	Threshold Voltage 2	V_{TH2}	4001	4(t)	V_{IN+} = 15V, V_{IN-} = 0V V_{CM} = 15V and 0V V_{PIN4} = 0.5V (Pins D 6-7) (Pins C 8-9)	40	60	mV
36	Threshold Supply Sensitivity	S_{THS}	4003	4(u)	V_{IN+} = 5.0V or 35V, V_{IN-} = 0V V_{CM} = 0V (Pins D 6-7-14) (Pins C 8-9-18)	-	−0.3	%/V
37	Adjustment Input Current	I_{Adj}	-	4(t)	V_{IN+} = 15V, V_{IN-} = 0V V_{PIN4} = 0.5V (Pin D 4) (Pin C 5)	−10	-	µA
38 to 39	Input Bias Current (Sense)	I_{IBSC}	-	4(v)	V_{IN+} = 15V, V_{IN-} = 0V V_{CM} = 15V and 0V (Pins D 6-7) (Pins C 8-9)	−200	200	µA

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D = DIP, C = CCP)	LIMITS		UNIT
						MIN	MAX	
40	Fault Delay	$t_{d\ fault}$	-	4(w)	V_{IN+} = 15V, V_{IN-} = 0V (Pin D 11) (Pin C 14)	30	600	ms/µF

TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D = DIP, C = CCP)	LIMITS		UNIT
						MIN	MAX	
1	Supply Current (Standby)	I_{CC}	-	4(a)	V_{IN+} = 15V, V_{IN-} = 0V (Pin D 1) (Pin C 2)	-	7.0	mA
2	Output Voltage (Referenced to V_{IN-})	V_{REF1}	-	4(a)	V_{IN+} = 15V, V_{IN-} = 0V (Pin D 3) (Pin C 4)	1.470	1.530	V
3	Line Regulation	K_{LI1}	-	4(a)	V_{IN+} = 5.0V to 35V, V_{IN-} = 0V (Pin D 3) (Pin C 4)	-	10	mV
4	Load Regulation	K_{LO1}	-	4(a)	V_{IN+} = 15V, V_{IN-} = 0V I_{VREF} = 0mA to 2.0mA (Pin D 3) (Pin C 4)	-	10	mV
5	Output Voltage (Referenced to V_{IN+})	V_{REF2}	-	4(b)	V_{IN+} = 15V, V_{IN-} = 0V (Pin D 2) (Pin C 3)	−2.06	−1.94	V
6	Line Regulation	K_{LI2}	-	4(b)	V_{IN+} = 5.0V to 35V, V_{IN-} = 0V (Pin D 3) (Pin C 4)	-	15	mV
7	Input Offset Voltage	V_{IO}	4001	4(c)	V_{IN+} = 15V, V_{IN-} = 0V (Pins D 8-9) (Pins C 10-12)	-	6.0	mV
8 to 9	Input Bias Current	I_{IB}	4001	4(c)	V_{IN+} = 15V, V_{IN-} = 0V (Pins D 8-9) (Pins C 10-12)	−4.0	-	µA
10	Input Offset Current	I_{IO}	4001	4(c)	V_{IN+} = 15V, V_{IN-} = 0V (Pins D 8-9) (Pins C 10-12)	-	1.0	µA
11	Small Signal Open Loop Gain	A_{VOL}	4004	4(d)	V_{IN+} = 15V, V_{IN-} = 0V (Pins D 8-9-14) (Pins C 10-12-18)	50	-	dB
12	Common Mode Rejection Ratio	CMRR	4003	4(e)	V_{IN+} = 15V, V_{IN-} = 0V V_{CM} = 0.5V to 33V (Pins D 8-9-14) (Pins C 10-12-18)	60	-	dB
13	Power Supply Rejection Ratio	PSRR	4003	4(f)	V_{IN+} = 5.0V to 35V, V_{IN-} = 0V V_{CM} = 1.5V (Pins D 8-9-14) (Pins C 10-12-18)	70	-	dB

TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURE (CONT'D)

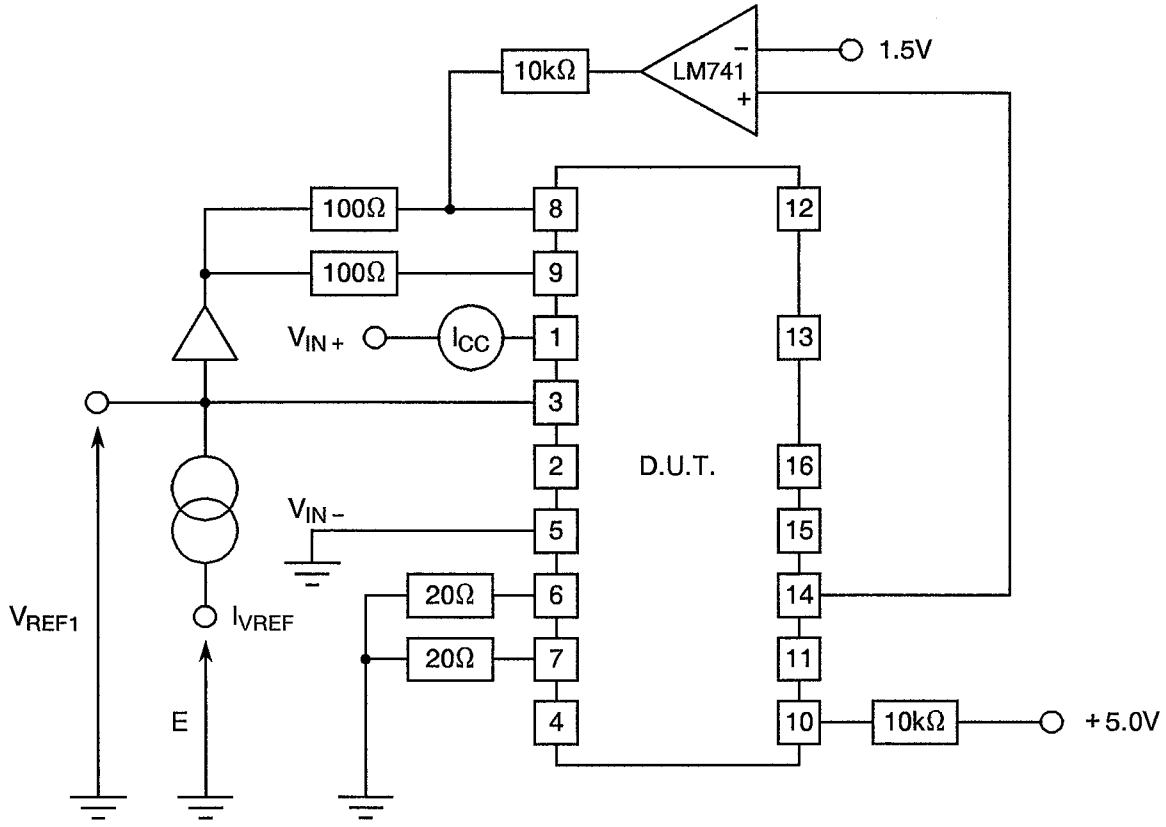
No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D = DIP, C = CCP)	LIMITS		UNIT
						MIN	MAX	
14	Output Current (Maximum)	$I_{OUT(max)}$	-	4(g)	V_{IN+} = 15V, V_{IN-} = 0V (Pins D 12-13) (Pins C 15-17)	200	-	mA
15	Saturation Voltage	V_{SAT}	-	4(h)	V_{IN+} = 15V, V_{IN-} = 0V I_{OUT} = 100mA (Pins D 12-13) (Pins C 15-17)	-	1.2	V
16	Output Leakage Current Low Level	I_{OZL}	-	4(i)	V_{IN+} = 15V, V_{IN-} = 0V (Pins D 12-13) (Pins C 15-17)	-	50	µA
17	Shutdown Input Voltage	V_{SD}	-	4(j)	V_{IN+} = 15V, V_{IN-} = 0V $I_{OUT} \leq$ 100µA (Pin D 14) (Pin C 18)	0.4	-	V
18	Shutdown Input Current	I_{SD}	-	4(i)	V_{IN+} = 15V, V_{IN-} = 0V $I_{OUT} \leq$ 100µA (Pin D 14) (Pin C 18)	−150	-	µA
19 to 20	Under and Over Voltage Fault Threshold	V_{THUO}	4001	4(k)	V_{IN+} = 15V, V_{IN-} = 0V V_{CM} = 1.5V (Pins D 8-9-11) (Pins C 10-12-14)	120	180	mV
21 to 22	Common Mode Sensitivity	CMS	4003	4(k)	V_{IN+} = 35V, V_{IN-} = 0V V_{CM} = 1.5V to 33V (Pins D 8-9-11) (Pins C 10-12-14)	−0.8	-	%/V
23 to 24	Supply Voltage Sensitivity	SVS	4003	4(k)	V_{IN+} = 5.0V to 35V, V_{IN-} = 0V V_{CM} = 1.5V (Pins D 8-9-11) (Pins C 10-12-14)	−1.0	-	%/V
25	Fault Alert Output Current	I_{Fault}	-	4(l)	V_{IN+} = 15V, V_{IN-} = 0V (Pin D 10) (Pin C 13)	2.0	-	mA
26	Fault Alert Saturation Voltage	$V_{SatFault}$	-	4(m)	V_{IN+} = 15V, V_{IN-} = 0V I_{OUT} = 1.0mA (Pin D 10) (Pin C 13)	-	0.5	V
27	Over Voltage Latch Output Current	$I_{OVLatch}$	-	4(n)	V_{IN+} = 15V, V_{IN-} = 0V (Pin D 15) (Pin C 19)	2.0	-	mA

TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURE (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D = DIP, C = CCP)	LIMITS		UNIT
						MIN	MAX	
28	Over Voltage Latch Output Saturation Voltage	$V_{SatLatch}$	-	4(o)	V_{IN+} = 15V, V_{IN-} = 0V I_{OUT} = 1.0mA (Pin D 15) (Pin C 19)	-	1.3	V
29	Over Voltage Latch Output Reset Voltage	$V_{OVReset}$	-	4(p)	V_{IN+} = 15V, V_{IN-} = 0V (Pin D 15) (Pin C 19)	0.3	0.6	V
30	Crowbar Gate Current	I_{CB}	-	4(q)	V_{IN+} = 15V, V_{IN-} = 0V (Pin D 16) (Pin C 20)	-	−100	mA
31	Crowbar Gate Leakage Current	I_{CBLeak}	-	4(r)	V_{IN+} = 35V, V_{IN-} = 0V (Pin D 16) (Pin C 20)	−50	-	µA
32 to 33	Threshold Voltage 1	V_{TH1}	4001	4(s)	V_{IN+} = 15V, V_{IN-} = 0V V_{CM} = 15V and 0V (Pins D 6-7) (Pins C 8-9)	130	170	mV
34 to 35	Threshold Voltage 2	V_{TH2}	4001	4(t)	V_{IN+} = 15V, V_{IN-} = 0V V_{CM} = 15V and 0V V_{PIN4} = 0.5V (Pins D 6-7) (Pins C 8-9)	40	60	mV
36	Threshold Supply Sensitivity	S_{THS}	4003	4(u)	V_{IN+} = 5.0V or 35V, V_{IN-} = 0V V_{CM} = 0V (Pins D 6-7-14) (Pins C 8-9-18)	-	−0.3	%/V
37	Adjustment Input Current	I_{Adj}	-	4(t)	V_{IN+} = 15V, V_{IN-} = 0V V_{PIN4} = 0.5V (Pin D 4) (Pin C 5)	−10	-	µA
38 to 39	Input Bias Current (Sense)	I_{IBSC}	-	4(v)	V_{IN+} = 15V, V_{IN-} = 0V V_{CM} = 15V and 0V (Pins D 6-7) (Pins C 8-9)	−200	200	µA
41 to 42	Threshold Voltage Temperature Stability from −55°C to +25°C from +25°C to +125°C	 STV1 STV2	-	4(s)	V_{IN+} = 15V, V_{IN-} = 0V V_{CM} = 15V and 0V (Pins D 6-7) (Pins C 8-9)	 - -	 111 111	µV/°C

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS

FIGURE 4(a) - STANDBY SUPPLY CURRENT AND " +1.5V REFERENCE SECTION", OUTPUT VOLTAGE, LINE REGULATION, LOAD REGULATION

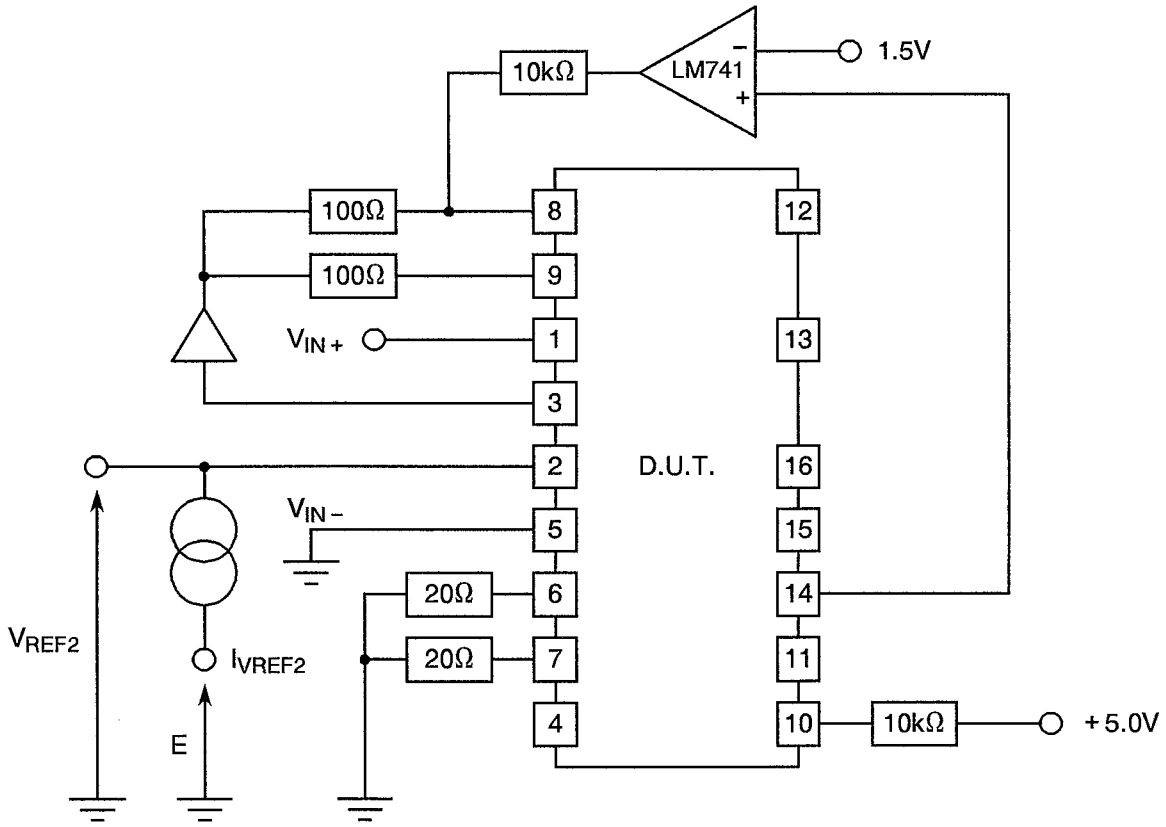


NOTES

1. Pin numbers refer to DIL package.
2. Test 1: Measure I_{CC} into pin 1. $I_{VREF} = 0A$.
3. Test 2: Measure V_{REF1} on pin 3. $I_{VREF} = 0A$.
4. Test 3: Measure $E = E_1$ on pin 3 when $V_{IN+} = 5.0V$ and $I_{VREF} = 0A$, and measure $E = E_2$ on pin 3 when $V_{IN+} = 35V$ and $I_{VREF} = 0A$. $K_{LI1} = E_2 - E_1$.
5. Test 4: Measure $E = E_3$ on pin 3 when $V_{IN+} = 15V$ and $I_{VREF} = 0A$, and measure $E = E_4$ on pin 3 when $V_{IN+} = 15V$ and $I_{VREF} = 2.0mA$. $K_{LO1} = E_4 - E_3$.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(b) - " − 2.0V REFERENCE SECTION", OUTPUT VOLTAGE, LINE REGULATION

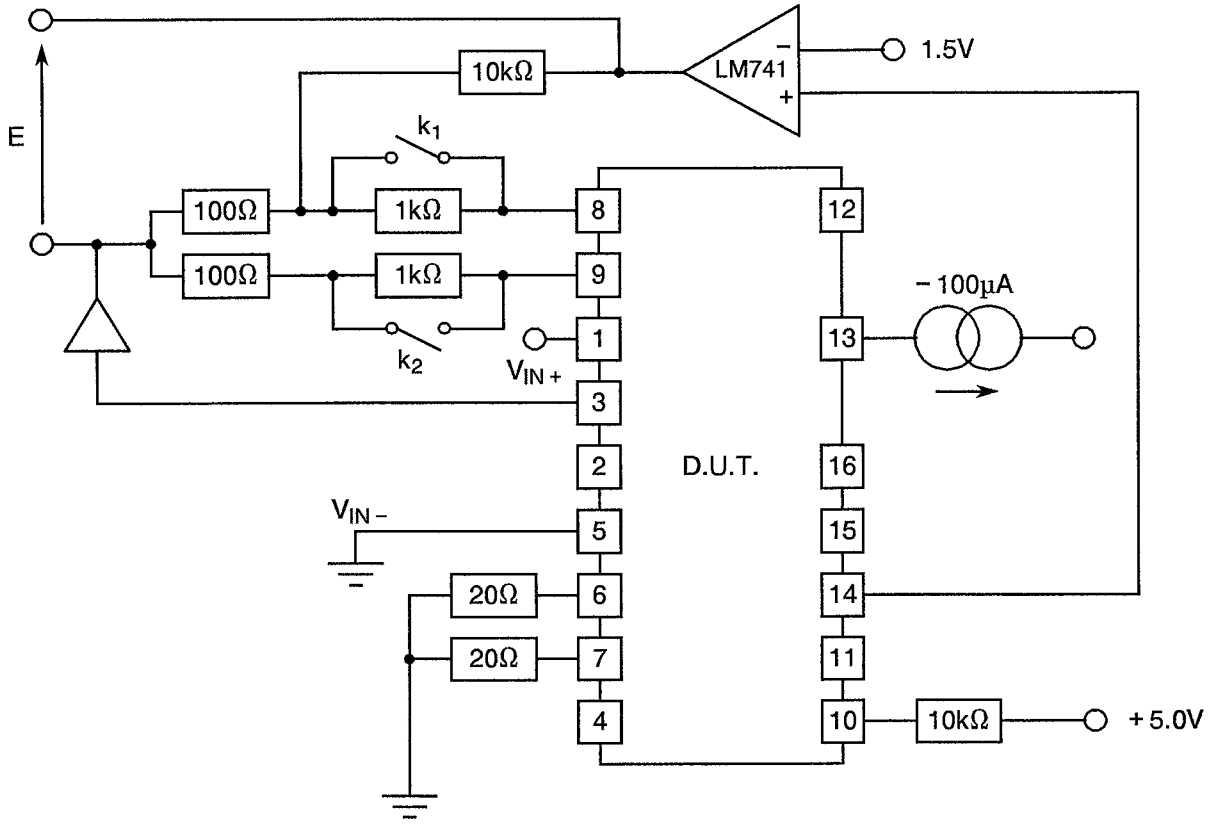


NOTES

1. Pin numbers refer to DIL package.
2. Test 5: Measure V_{REF2} between pin 2 (+) and pin 1 (−) when $V_{IN+} = 15V$ and $I_{VREF2} = 0A$.
3. Test 6: Measure $E = E_1$ between pin 2 (+) and pin 1 (−) when $V_{IN+} = 5.0V$ and $I_{VREF} = 0A$, and measure $E = E_2$ between pin 2 (+) and pin 1 (−) when $V_{IN+} = 35V$ and $I_{VREF} = 0A$. $K_{LI2} = E_2 - E_1$.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(c) - "ERROR AMPLIFIER SECTION", INPUT OFFSET VOLTAGE, INPUT BIAS CURRENT, INPUT OFFSET CURRENT



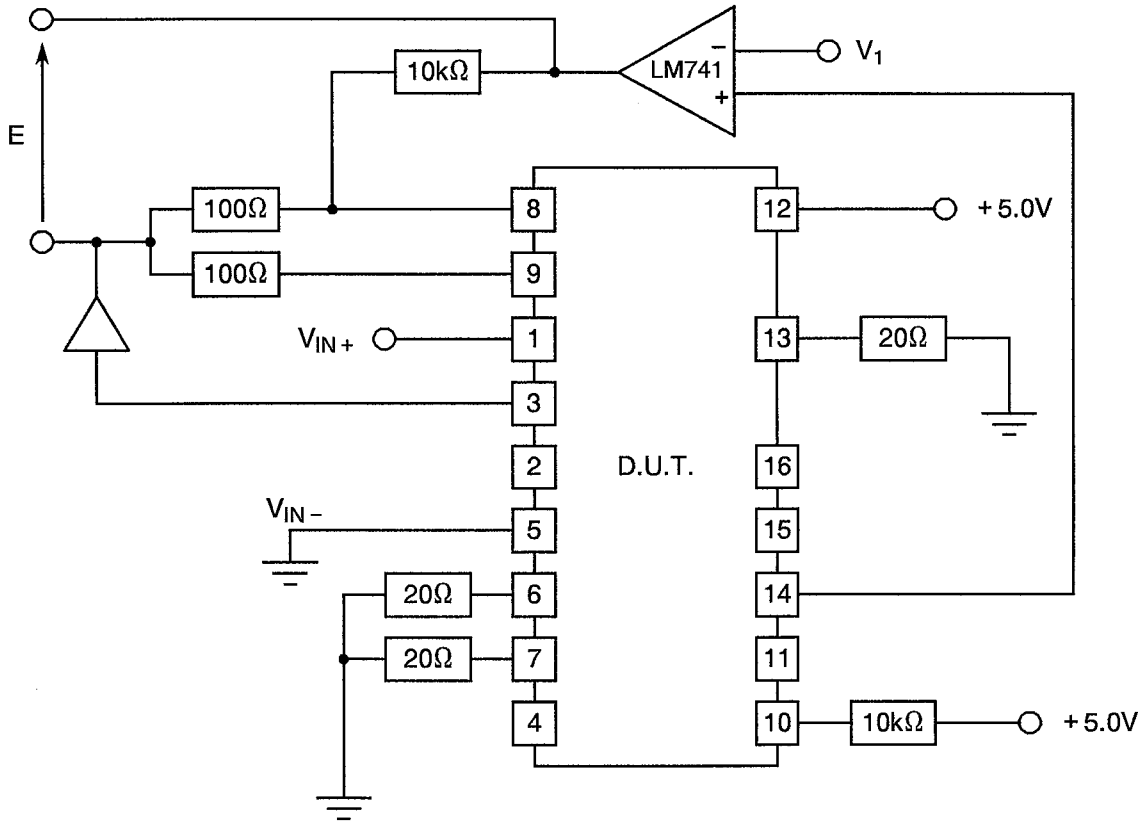
NOTES

1. Pin numbers refer to DIL package.
2. Test 7: Close K_1 and K_2, measure $E = E_1$. $V_{IO} = \frac{E_1}{101}$
3. Tests 8 to 10: Close K_1 close K_2, measure $E = E_2$.
   Close K_1 open K_2, measure $E = E_3$.
   Close K_1 close K_2, measure $E = E_4$.
   Open K_1 close K_2, measure $E = E_5$.

$$I_{IB} = \frac{\frac{E_3 - E_2}{10100} + \frac{E_5 - E_4}{10100}}{2} \qquad I_{IO} = \left| \frac{E_3 - E_2}{10100} - \frac{E_5 - E_4}{10100} \right|$$

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(d) - "ERROR AMPLIFIER SECTION", SMALL SIGNAL OPEN LOOP GAIN

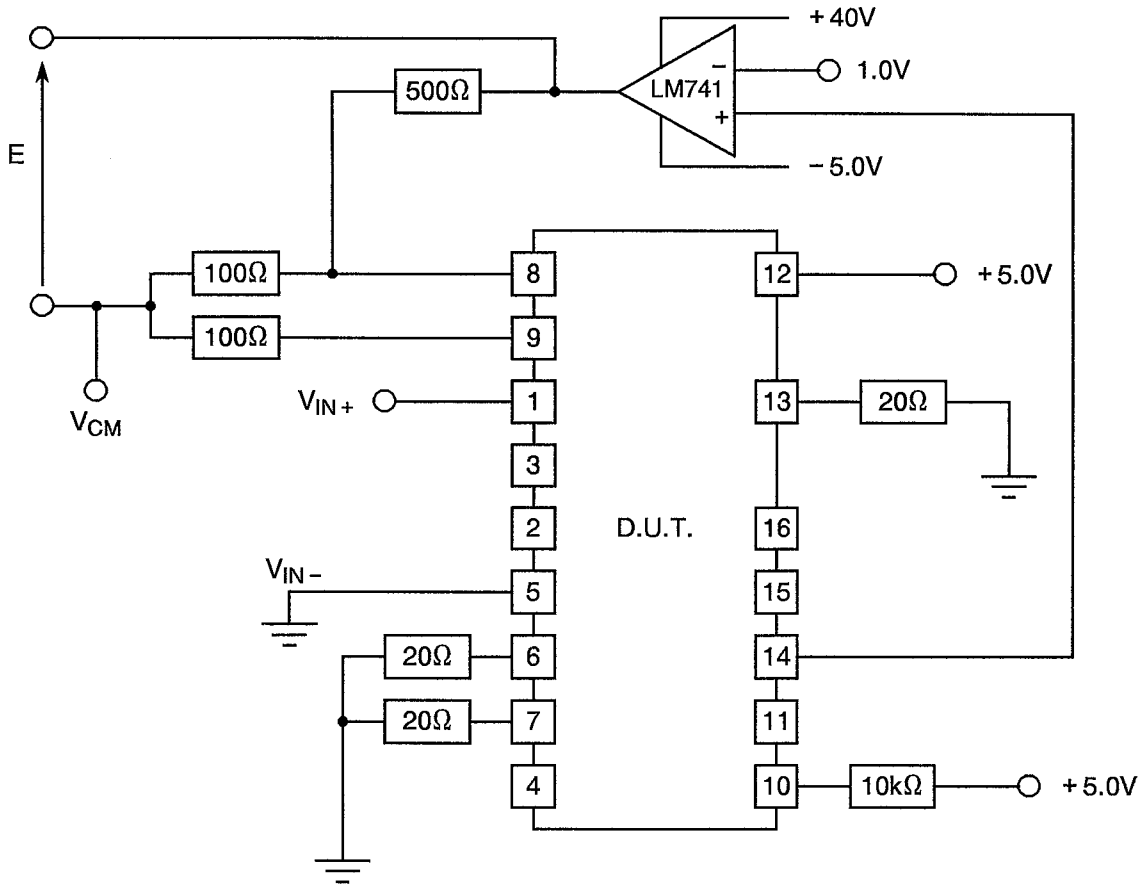


NOTES

1. Pin numbers refer to DIL package.
2. Test 11: Measure $E = E_1$ when $V_1 = 1.7V$ and $E = E_2$ when $V_1 = 2.5V$. $A_{VOL} = 20\text{Log}\left(\frac{800}{\frac{E_1 - E_2}{101}}\right)$

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(e) - "ERROR AMPLIFIER SECTION", COMMON MODE REJECTION RATIO



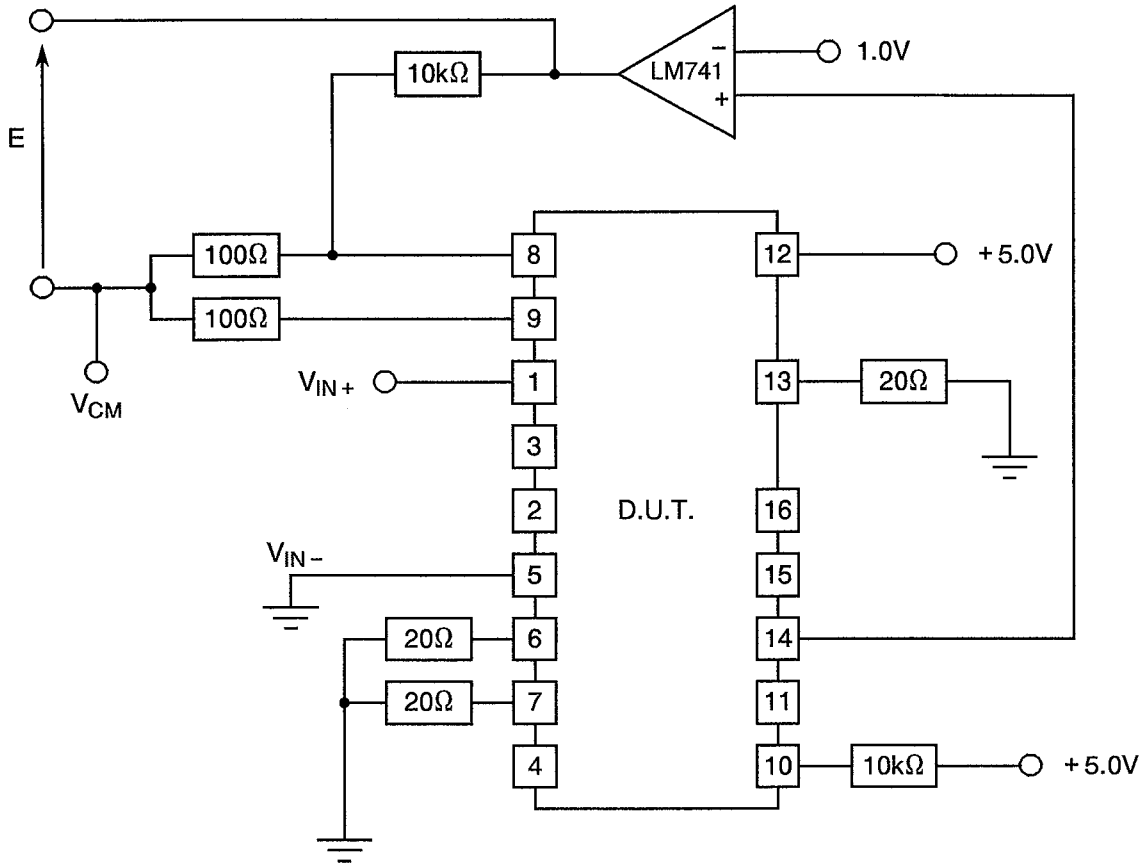
NOTES

1. Pin numbers refer to DIL package.
2. Test 12: With $V_{IN+} = 35V$, measure $E = E_1$ when $V_{CM} = 0.5V$ and $E = E_2$ when $V_{CM} = 33V$.

$$CMRR = 20Log \left(\frac{\frac{32.5}{E_1 - E_2}}{6} \right)$$

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(f) - "ERROR AMPLIFIER SECTION", POWER SUPPLY REJECTION RATIO



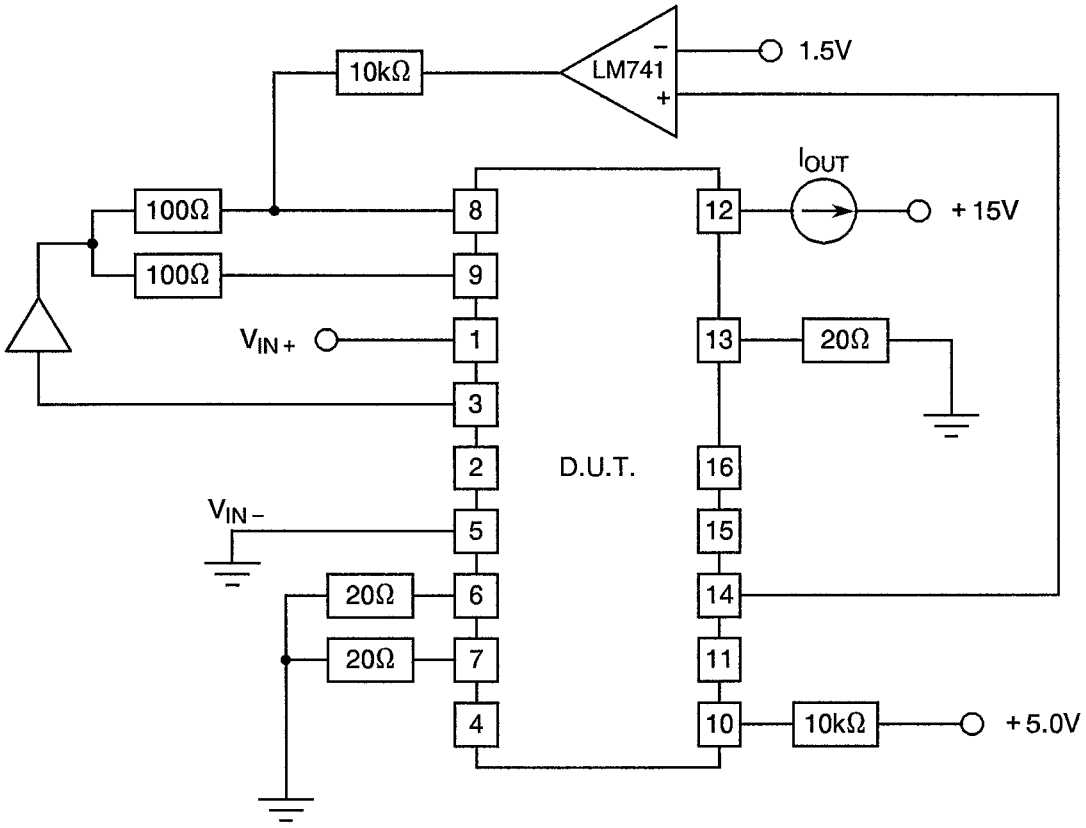
NOTES

1. Pin numbers refer to DIL package.
2. Test 13: With $V_{CM} = 1.5V$, measure $E = E_1$ when $V_{IN+} = 5.0V$ and $E = E_2$ when $V_{IN+} = 35V$.

$$PSRR = 20\text{Log}\left(\frac{30}{\frac{E_1 - E_2}{101}}\right)$$

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(g) - "DRIVER SECTION", MAXIMUM OUTPUT CURRENT

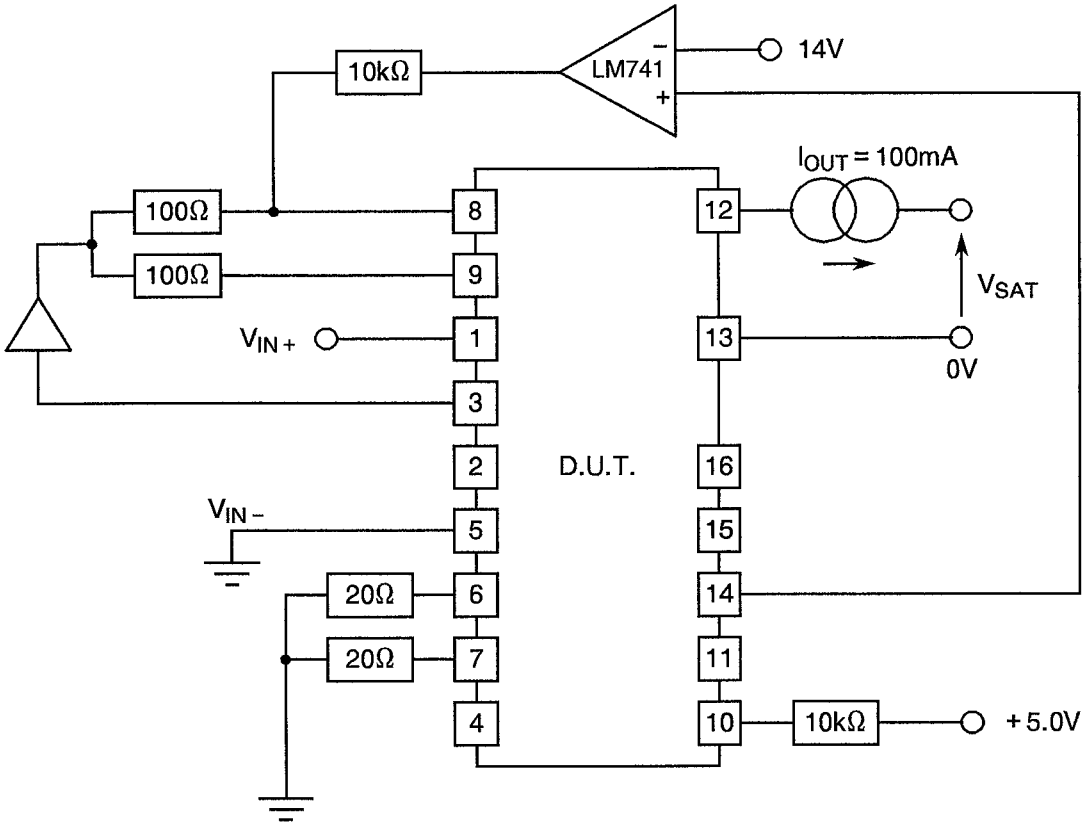


NOTES

1. Pin numbers refer to DIL package.
2. Test 14: Measure I_{OUT} into pin 12.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(h) - "DRIVER SECTION", SATURATION VOLTAGE

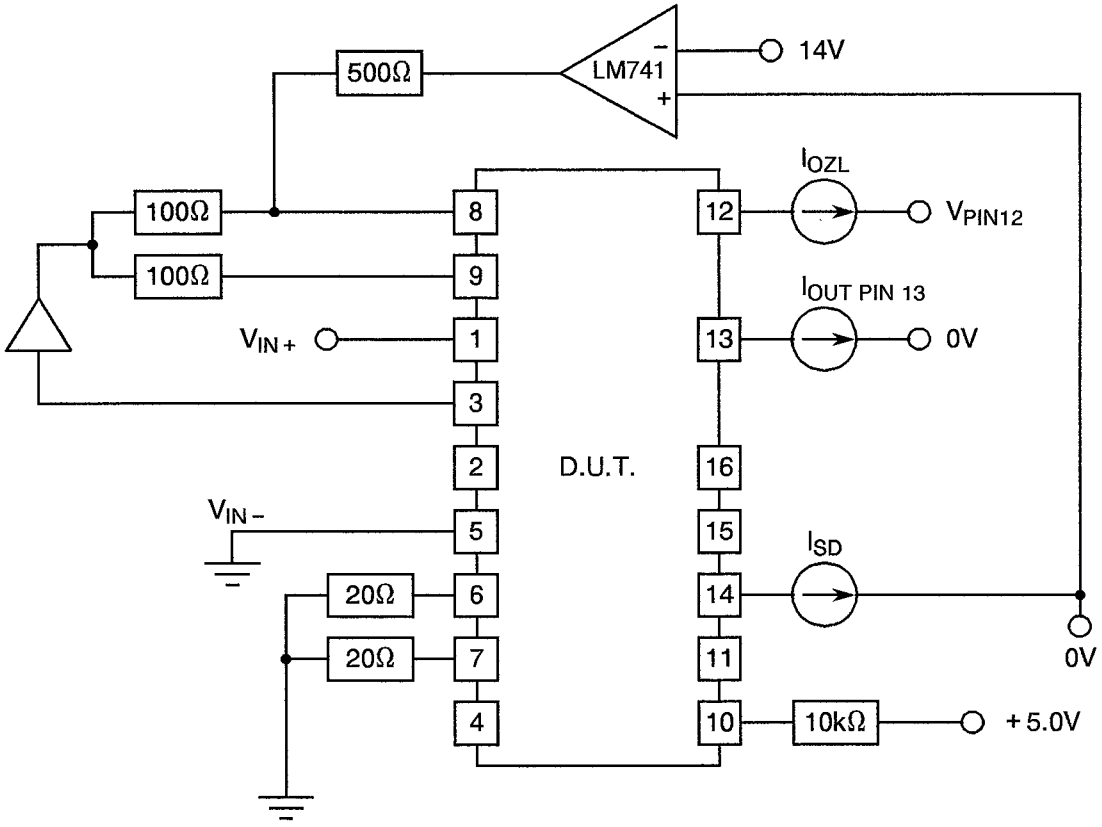


NOTES

1. Pin numbers refer to DIL package.
2. Test 15: Measure V_{SAT} at pin 12.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(i) - "DRIVER SECTION", OUTPUT LEAKAGE CURRENT, SHUTDOWN INPUT CURRENT

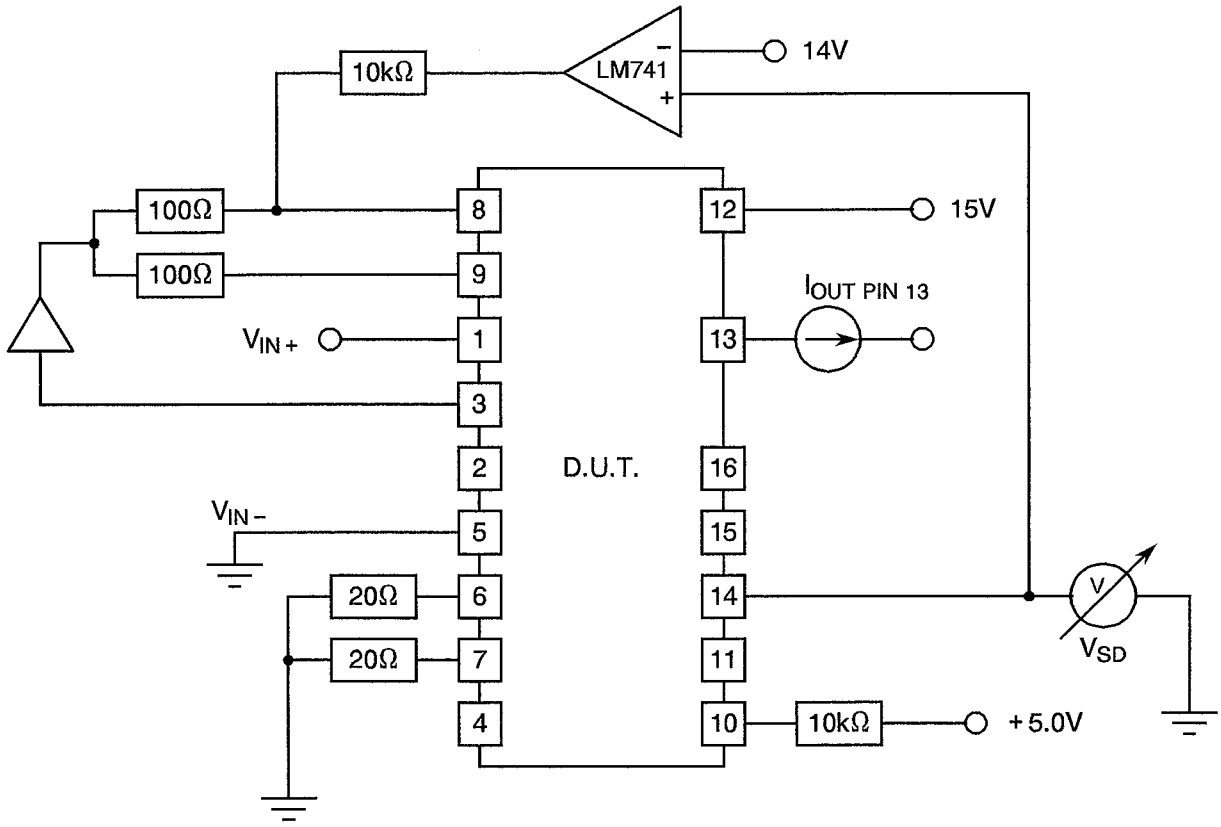


NOTES

1. Pin numbers refer to DIL package.
2. Test 16: Measure I_{OZL} into pin 12 when $V_{PIN12} = 35V$.
3. Test 18: Measure I_{SD} into pin 14 when $V_{PIN12} = 15V$ and $I_{OUT\ PIN\ 13} \leq 100\mu A$.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(j) - "DRIVER SECTION", SHUTDOWN INPUT VOLTAGE

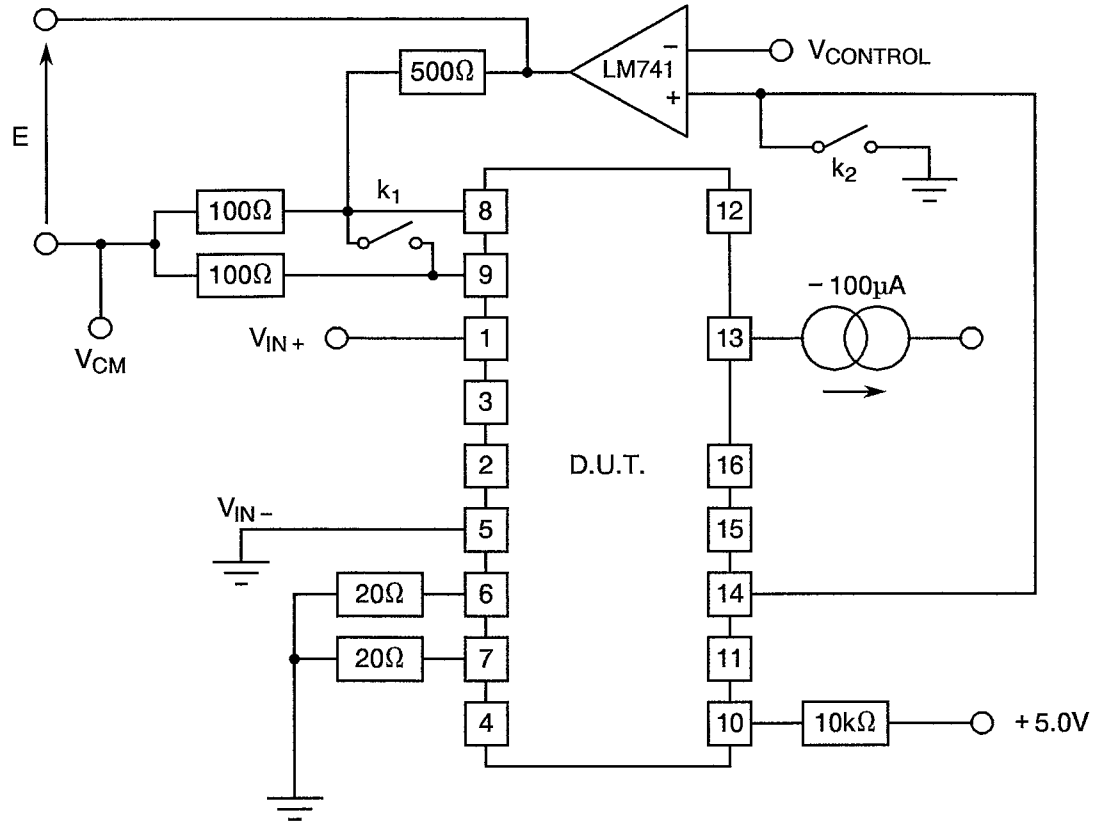


NOTES

1. Pin numbers refer to DIL package.
2. Test 17: Adjust pin 14 voltage (V_{SD}) until $I_{OUT\ PIN\ 13} \leq 100\mu A$.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(k) - "FAULT AMPLIFIER SECTION", UNDER AND OVER VOLTAGE FAULT THRESHOLD, COMMON MODE SENSITIVITY, SUPPLY VOLTAGE SENSITIVITY.



NOTES

1. Pin numbers refer to DIL package.
2. Tests 19, 20: When k_1 and k_2 open, measure $E = E_1$ when $V_{CONTROL} = 2.0V$. $V_{THU} = \frac{|E_1|}{6}$

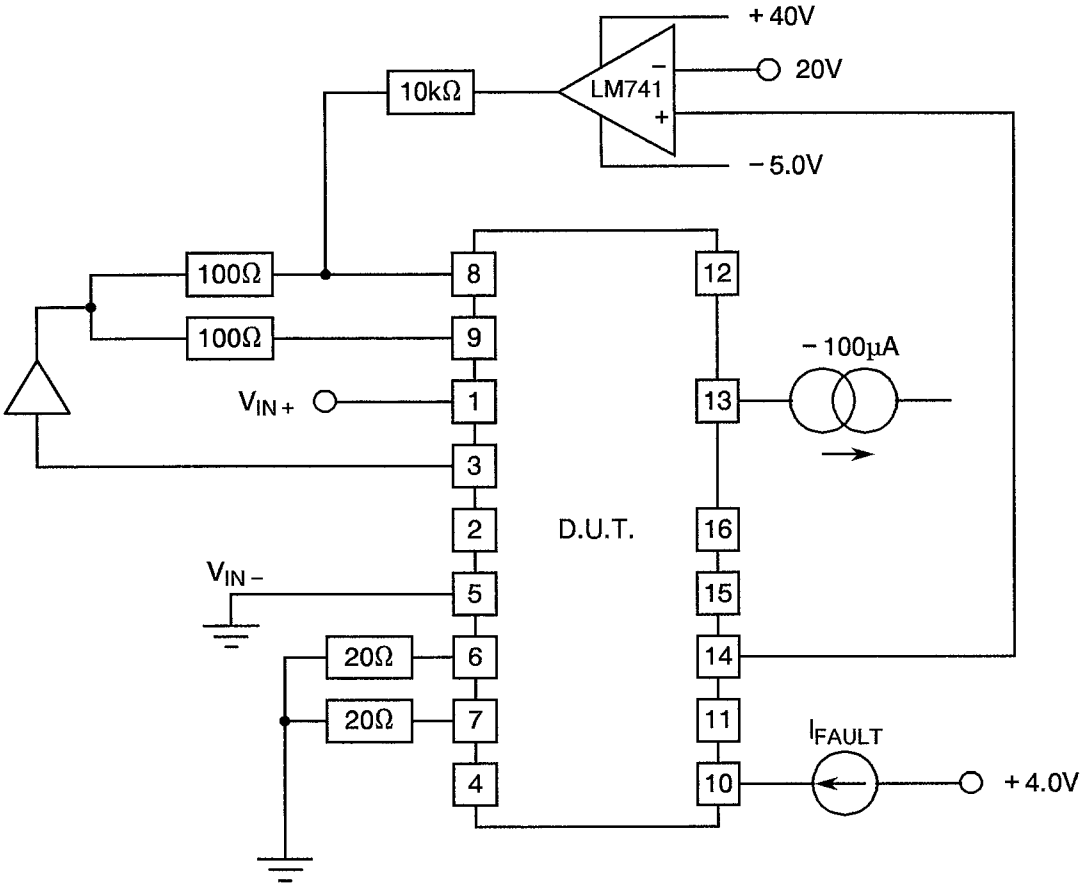
   When k_1 open and k_2 closed, start up test with $V_{CONTROL} = 6.0V$ then open k_2 (k_1 remains open) and set $V_{CONTROL} = 2.0V$, measure $E = E_2$ with $V_{CONTROL} = 2.0V$. $V_{THO} = \frac{|E_2|}{6}$
3. Tests 21, 22: When k_1 and k_2 open, measure $E = E_3$ when $V_{CM} = 1.5V$ and $E = E_4$ when $V_{CM} = 33V$. When k_1 closed and k_2 open, measure $E = E_5$ when $V_{CM} = 1.5V$ and measure $E = E_6$ when $V_{CM} = 33V$.

   $$CMS_1 = \frac{\frac{(E_3 - E_4) / 6}{V_{THU}}}{31.5} \qquad CMS_2 = \frac{\frac{(E_5 - E_6) / 6}{V_{THO}}}{31.5}$$
4. Tests 23, 24: When k_1 and k_2 open, measure $E = E_7$ when $V_{IN+} = 5.0V$ and $E = E_8$ when $V_{IN+} = 35V$. When k_1 closed, k_2 open and $V_{CM} = 1.5V$, measure $E = E_9$ when $V_{IN+} = 5.0V$ and measure $E = E_{10}$ when $V_{IN+} = 35V$.

   $$SVS_1 = \frac{\frac{(E_7 - E_8) / 6}{V_{THU}}}{30} \qquad SVS_2 = \frac{\frac{(E_9 - E_{10}) / 6}{V_{THO}}}{30}$$

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(l) - "FAULT AMPLIFIER SECTION", FAULT ALERT OUTPUT CURRENT

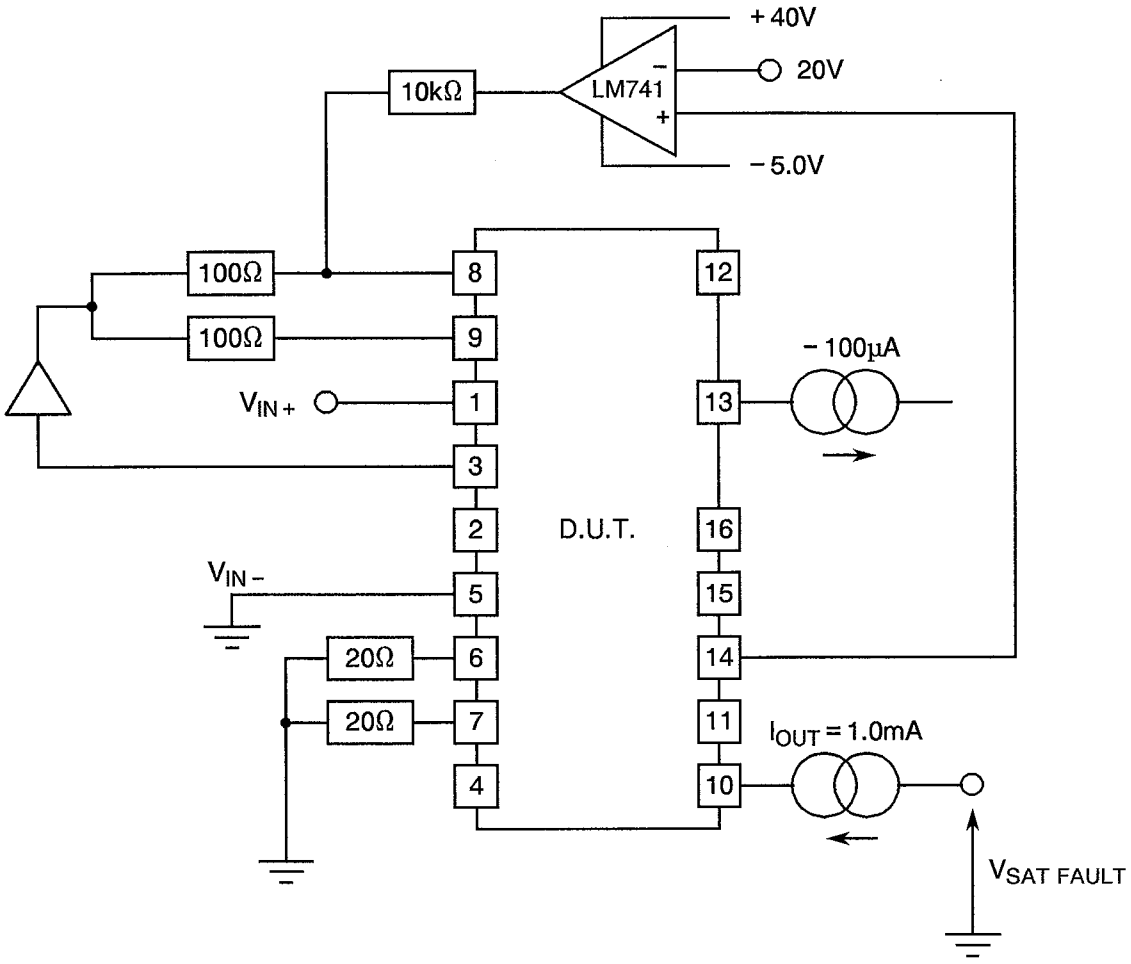


NOTES

1. Pin numbers refer to DIL package.
2. Test 25: Measure current (I_{FAULT}) into pin 10.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(m) - "FAULT AMPLIFIER SECTION", FAULT ALERT SATURATION VOLTAGE

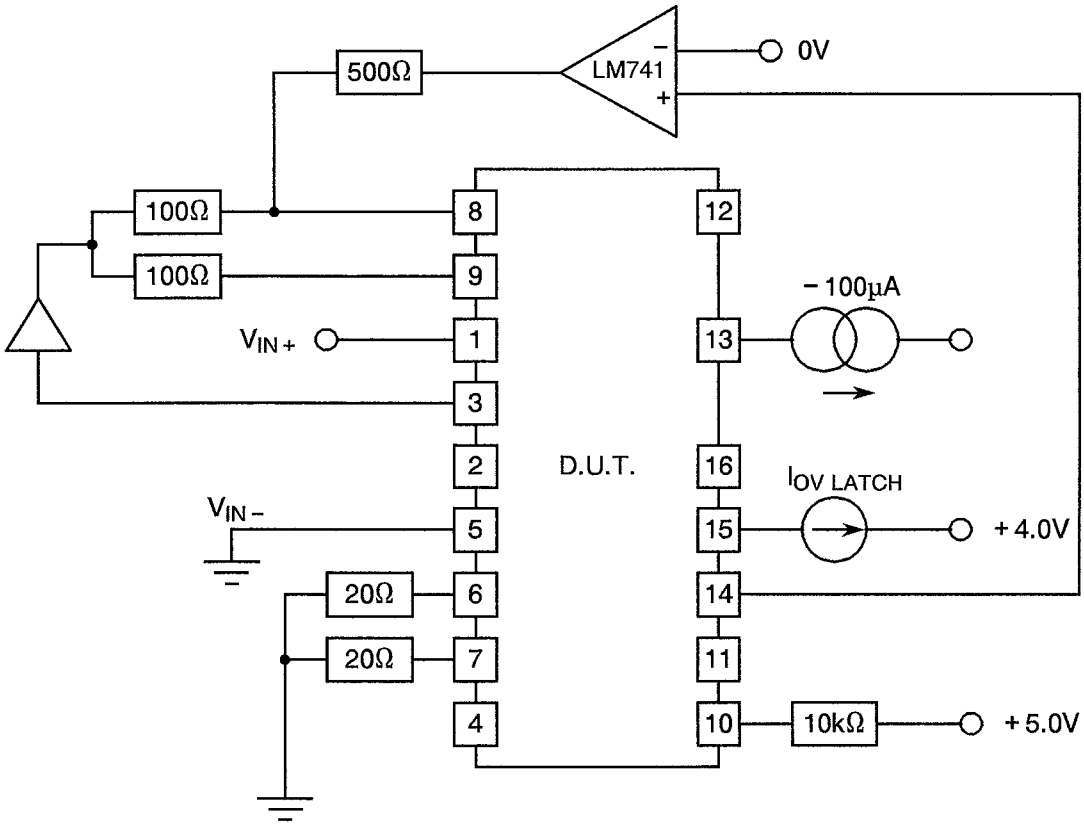


NOTES

1. Pin numbers refer to DIL package.
2. Test 26: Measure current ($V_{SAT\ FAULT}$) at pin 10.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(n) - "FAULT AMPLIFIER SECTION", OVER VOLTAGE LATCH OUTPUT CURRENT

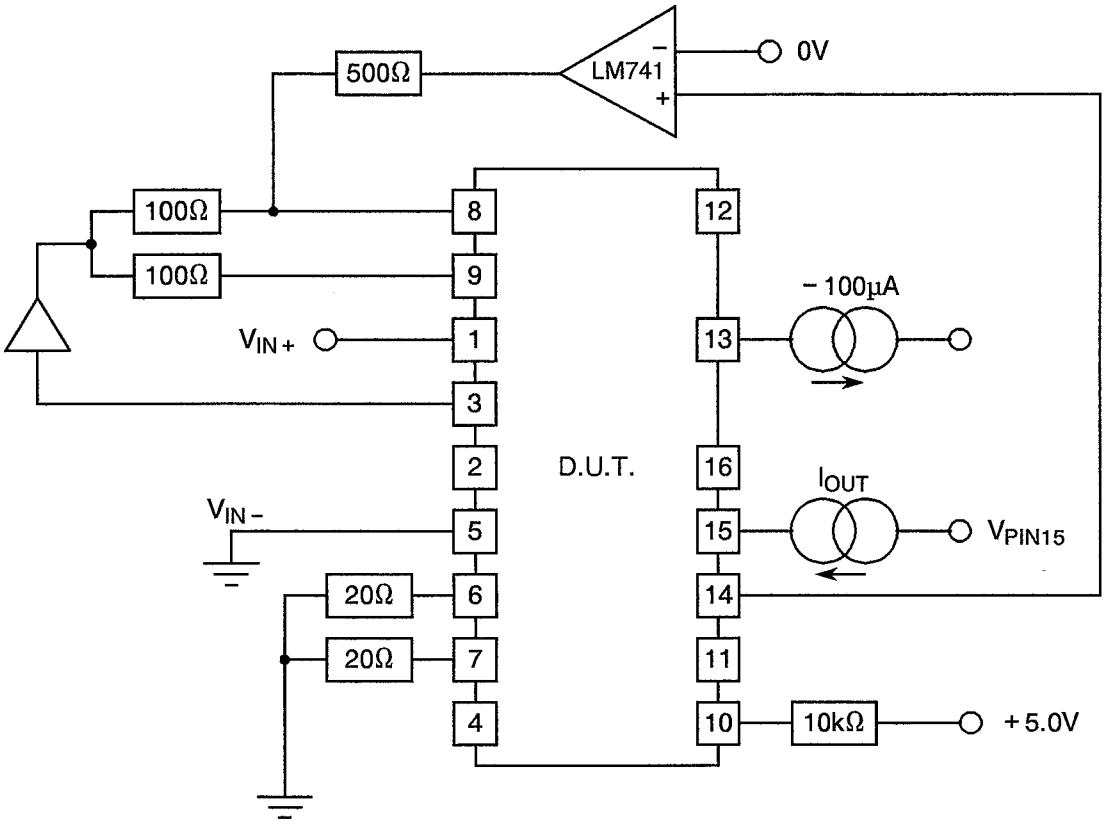


NOTES

1. Pin numbers refer to DIL package.
2. Test 27: Measure current ($I_{OV\ LATCH}$) into pin 15.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(o) - "FAULT AMPLIFIER SECTION", OVER VOLTAGE LATCH SATURATION VOLTAGE

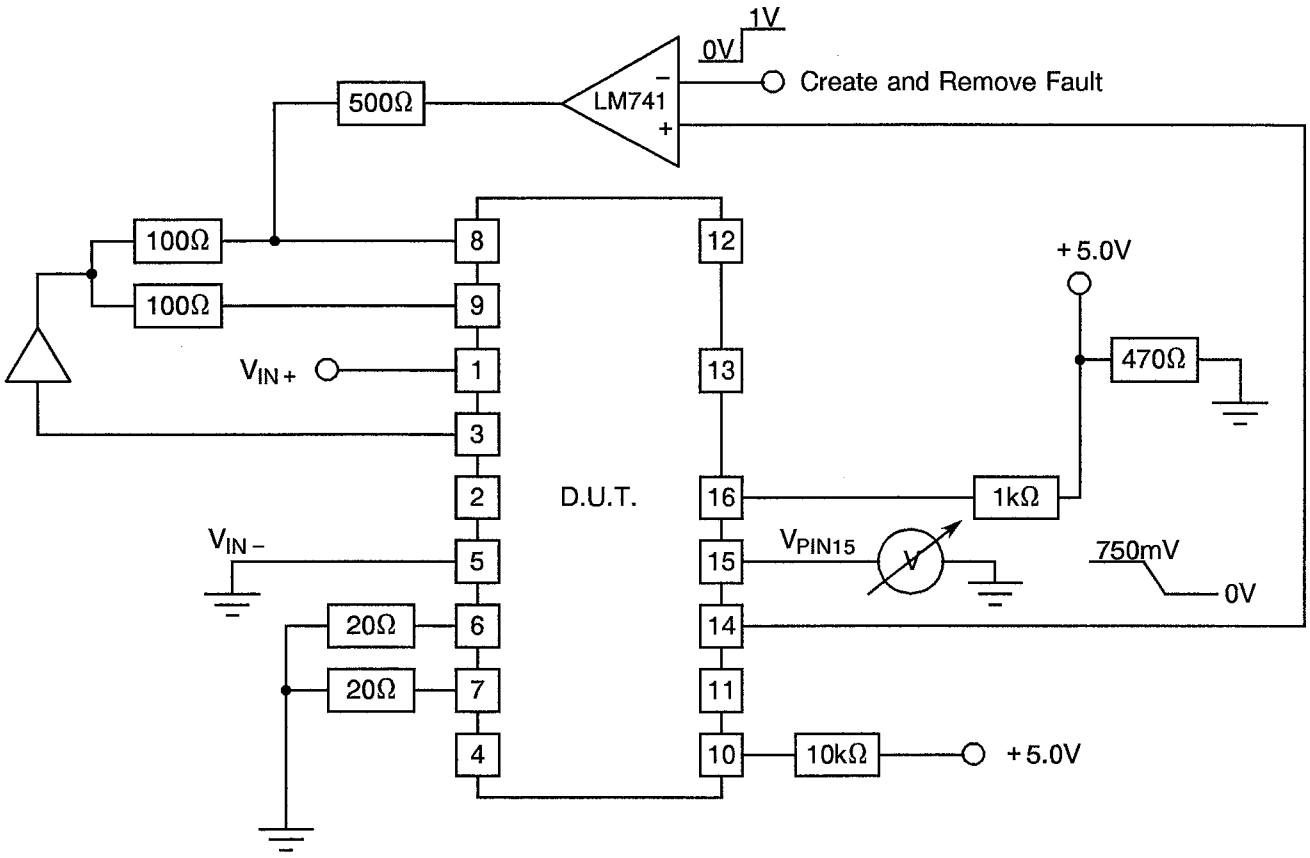


NOTES

1. Pin numbers refer to DIL package.
2. Test 28: Measure voltage ($V_{SAT\ LATCH}$) at pin 15 when I_{OUT} = 1.0mA.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(p) - "FAULT AMPLIFIER SECTION", OVER VOLTAGE LATCH OUTPUT RESET VOLTAGE

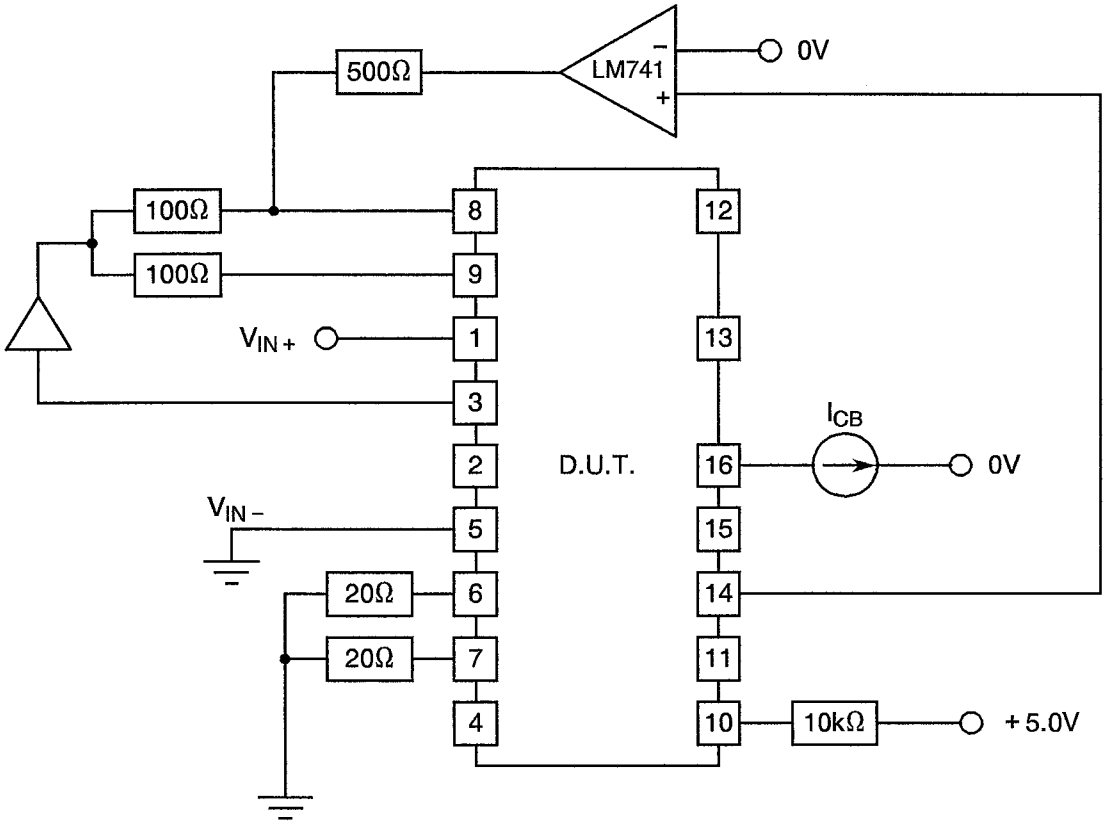


NOTES

1. Pin numbers refer to DIL package.
2. Test 29: Adjust pin 15 voltage ($V_{OV\ RESET}$) until pin 16 switches.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(q) - "FAULT AMPLIFIER SECTION", CROWBAR GATE CURRENT

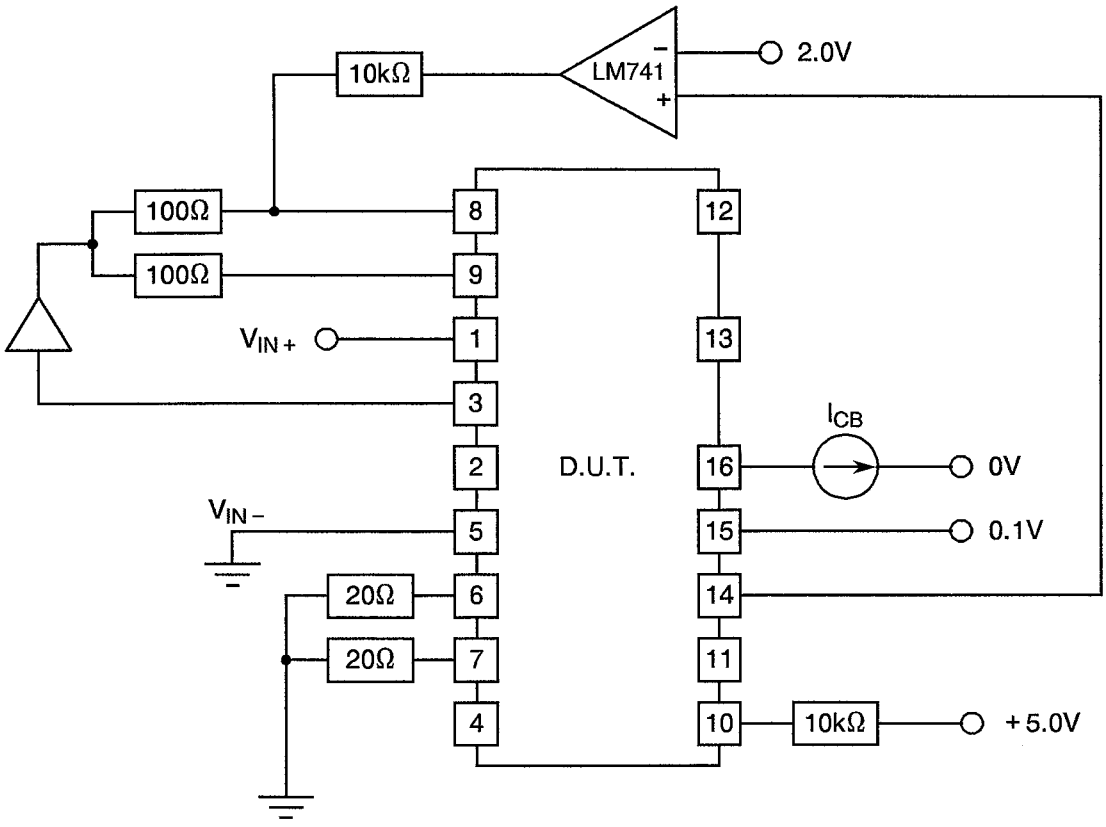


NOTES

1. Pin numbers refer to DIL package.
2. Test 30: Measure current (I_{CB}) into pin 16.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(r) - "FAULT AMPLIFIER SECTION", CROWBAR GATE LEAKAGE CURRENT

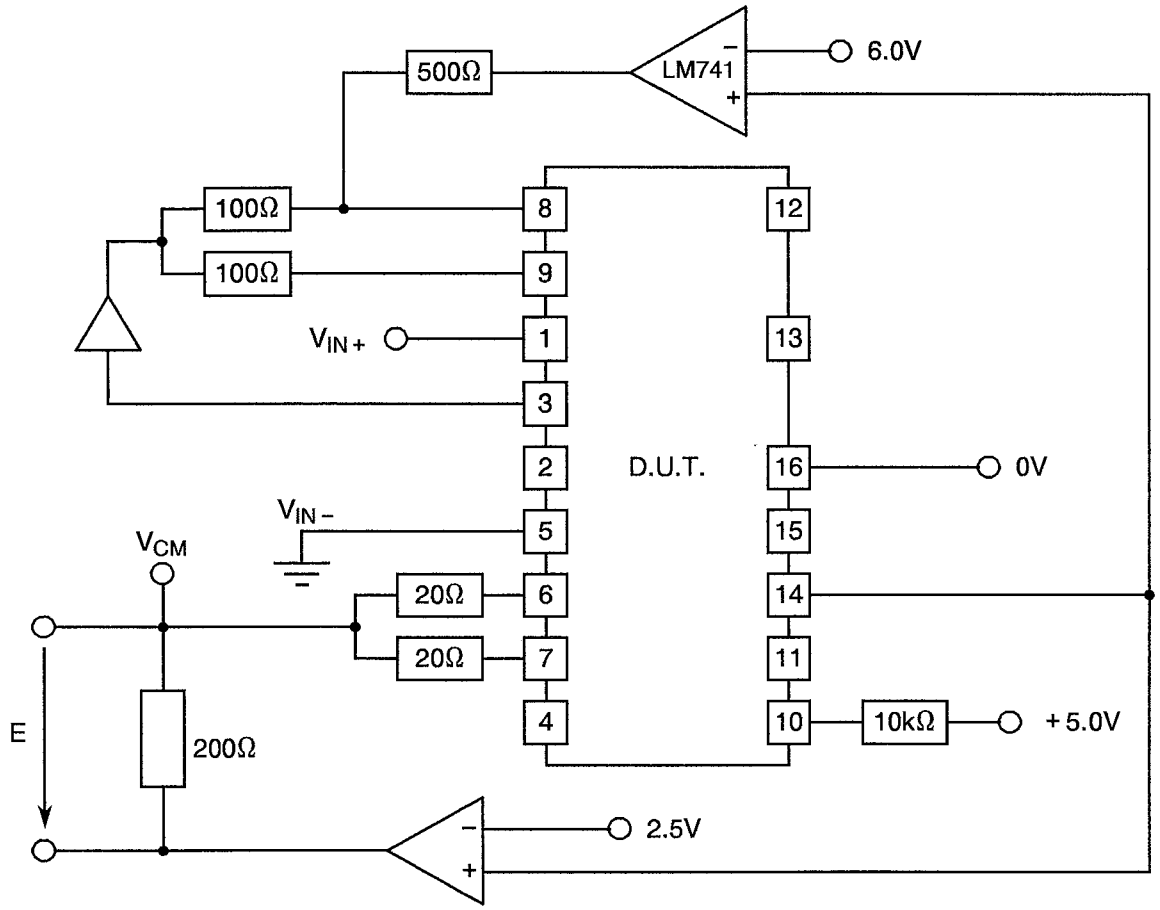


NOTES

1. Pin numbers refer to DIL package.
2. Test 31: Measure current ($I_{CB\ LEAK}$) into pin 16 with V_{IN+} = 35V.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(s) - "CURRENT SENSE AMPLIFIER SECTION", THRESHOLD VOLTAGE

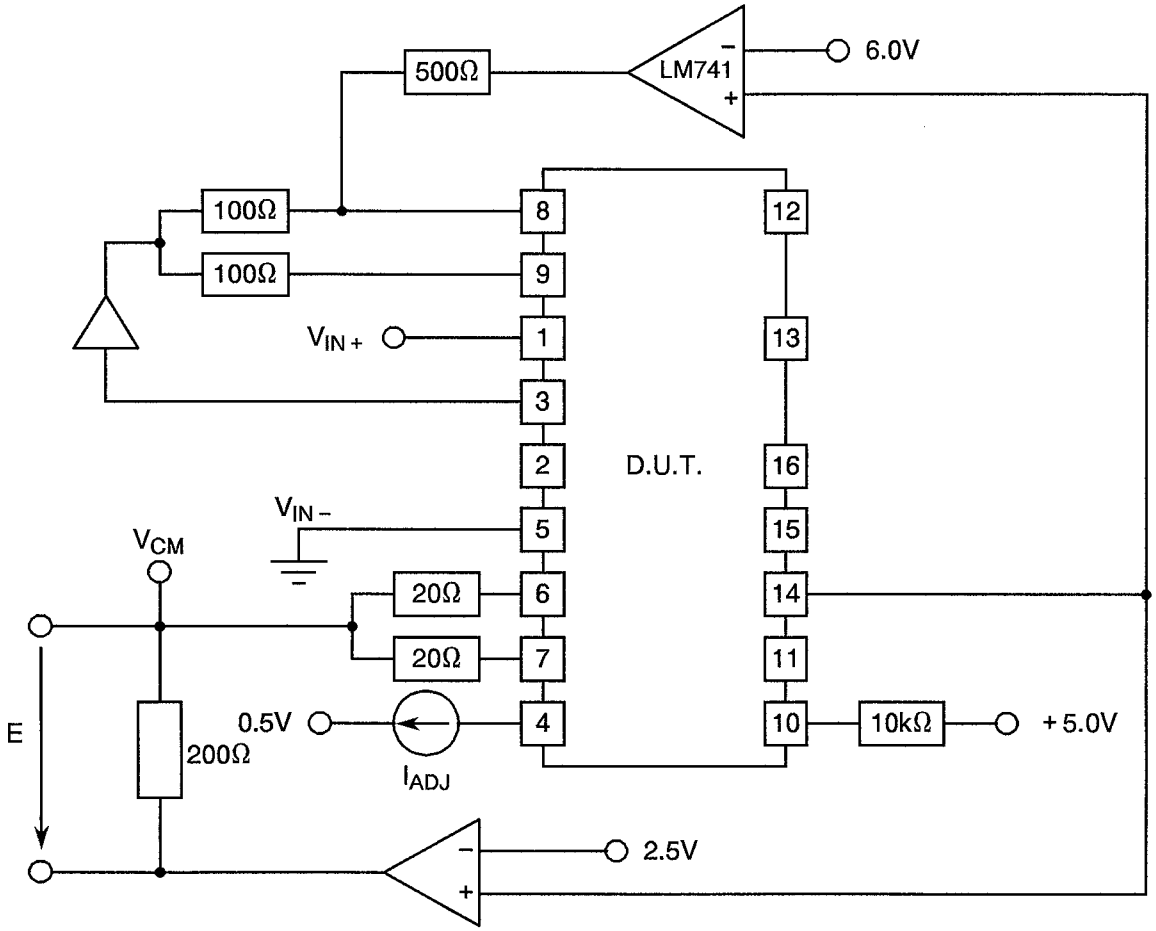


NOTES

1. Pin numbers refer to DIL package.
2. Tests 32, 33: Measure $E = E_1$ when $V_{CM} = 15V$ and $E = E_2$ when $V_{CM} = 0V$. $V_{TH1} = \frac{E_1}{11}$ and $V_{TH1} = \frac{E_2}{11}$
3. Tests 41, 42: STV1 is measured between −55°C and +25°C and STV2 is measured between +25°C and +125°C using V_{TH1} when V_{CM} = 15V or 0V.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(t) - "CURRENT SENSE AMPLIFIER SECTION", THRESHOLD VOLTAGE



NOTES

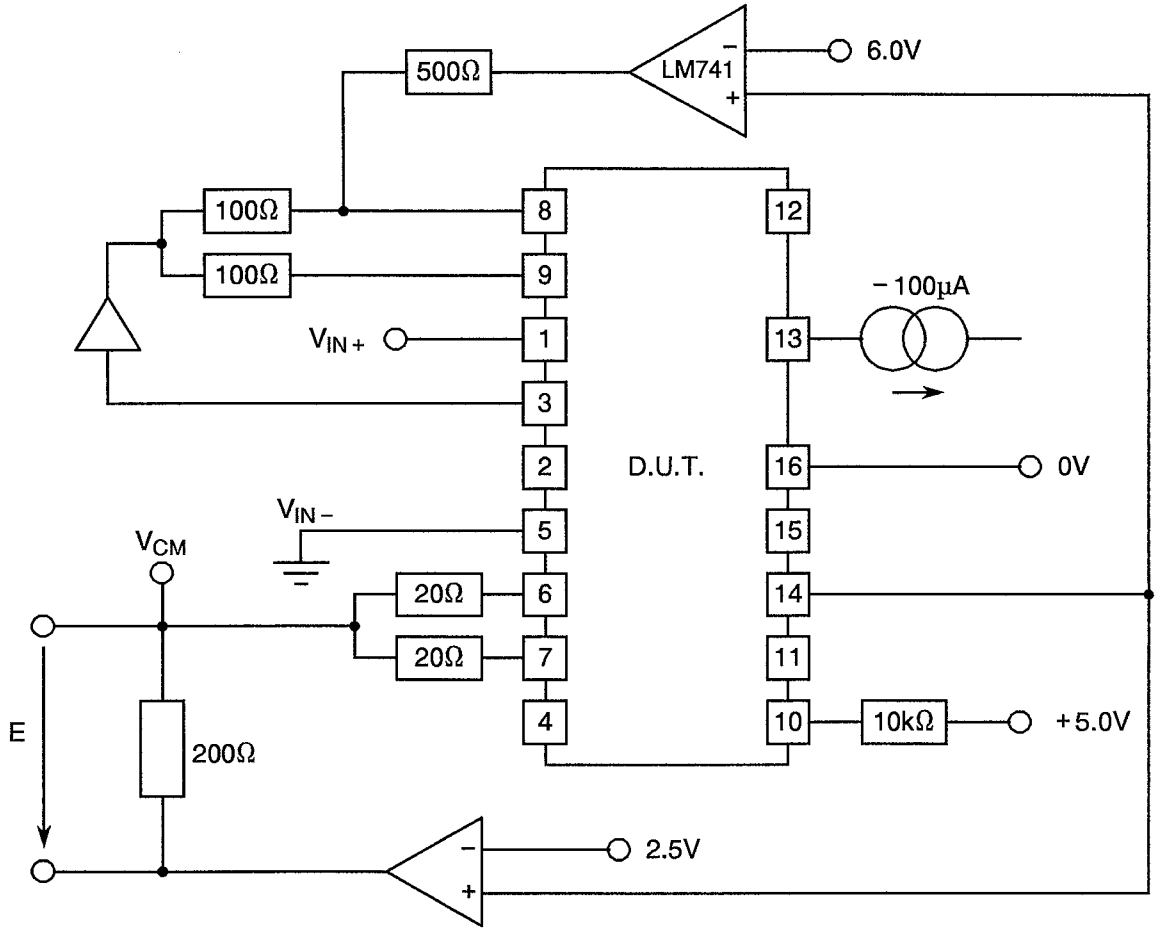
1. Pin numbers refer to DIL package.
2. Tests 34, 35: $V_{PIN4} = 0.5V$, measure $E = E_1$ when $V_{CM} = 15V$ and $E = E_2$ when $V_{CM} = 0V$.

$$V_{TH2} = \frac{E_1}{11} \qquad V_{TH2} = \frac{E_2}{11}$$

3. Test 37: $V_{PIN4} = 0.5V$, measure current (I_{ADJ}) into pin 4 when $V_{CM} = 0V$.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(u) - "CURRENT SENSE AMPLIFIER SECTION", THRESHOLD SUPPLY SENSITIVITY

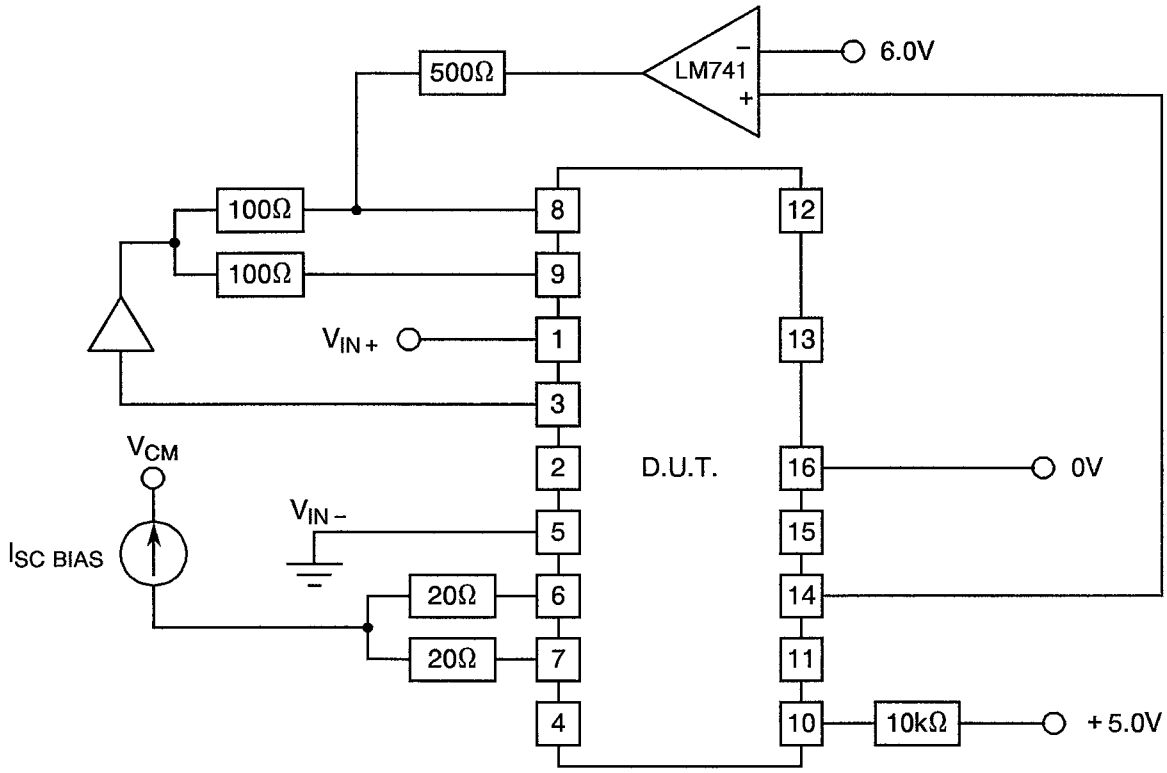


NOTES

1. Pin numbers refer to DIL package.
2. Test 36: Measure $E = E_1$ when $V_{IN+} = 5.0V$ and measure $E = E_2$ when $V_{IN+} = 35V$. $S_{THS} = \dfrac{(E_1 - E_2) / 11}{\dfrac{V_{TH1}}{30}}$

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(v) - "CURRENT SENSE AMPLIFIER SECTION", INPUT BIAS CURRENT

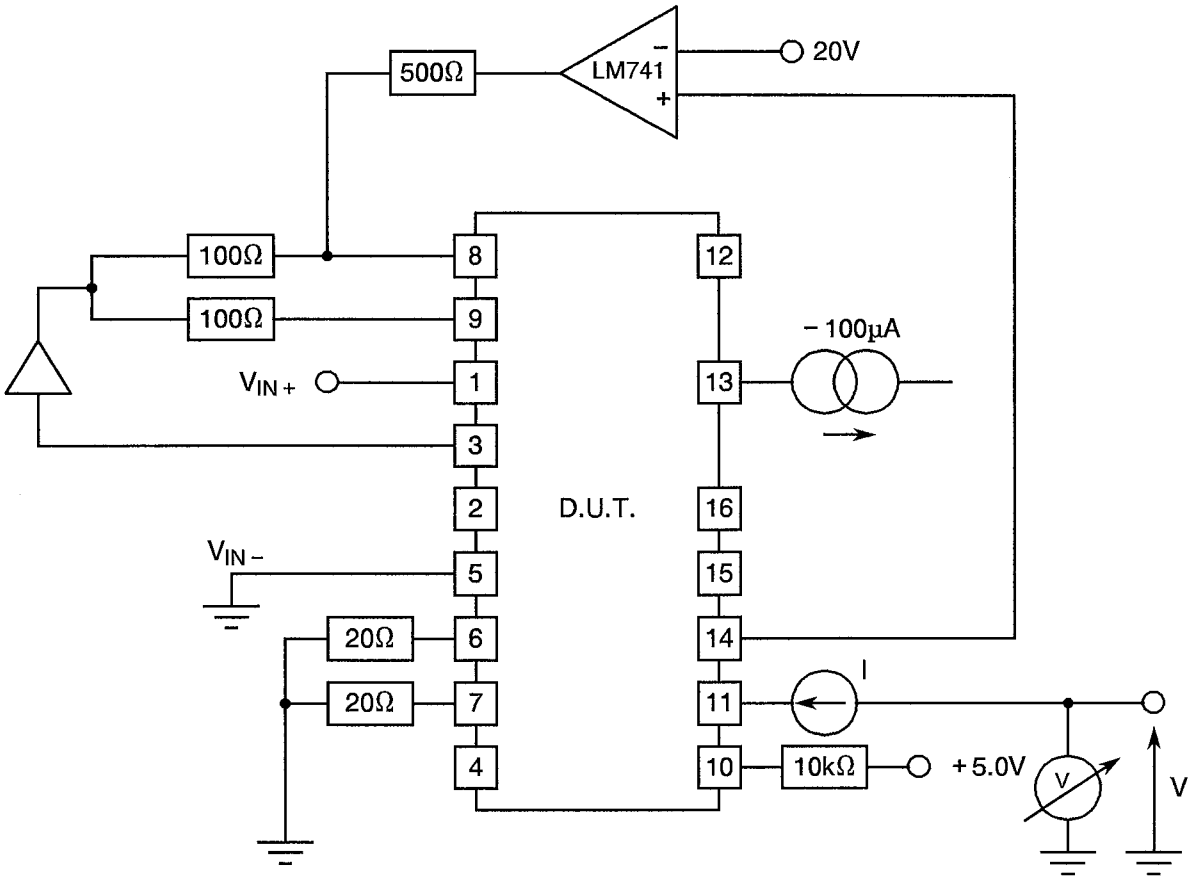


NOTES

1. Pin numbers refer to DIL package.
2. Tests 38, 39: Measure current ($I_{SC\ BIAS}$) into pin 6 and into pin 7 when $V_{CM} = 15V$ and when $V_{CM} = 0V$.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(w) - "FAULT AMPLIFIER SECTION", FAULT DELAY



NOTES

1. Pin numbers refer to DIL package.
2. Test 40: Measure current I into pin 11 ($V_{PIN11} = 0.5V$). Ramp pin 11 until fault alert turns on, measure voltage V at pin 11.

$$t_{D\ FAULT} = \frac{\Delta V \times C\ (1.0\mu F)}{-I}$$

TABLE 4 - PARAMETER DRIFT VALUES

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	CHANGE LIMITS (Δ)	UNIT
1	Supply Current (Standby)	I_{CC}	As per Table 2	As per Table 2	±10	%
2	Output Voltage (Reference to V_{IN-})	V_{REF1}	As per Table 2	As per Table 2	±0.5	%
5	Output Voltage (Reference to V_{IN+})	V_{REF2}	As per Table 2	As per Table 2	±1.0	%
7	Input Offset Voltage	V_{IO}	As per Table 2	As per Table 2	±0.5	mV
8 to 9	Input Bias Current	I_{IB}	As per Table 2	As per Table 2	±0.4 or (1) 100	µA %
10	Input Offset Current	I_{IO}	As per Table 2	As per Table 2	±0.1 or (1) 100	µA %

NOTES
1. Whichever is greater, referred to the initial value.

TABLE 5(a) - CONDITIONS FOR HIGH TEMPERATURE REVERSE BIAS BURN-IN

Not applicable.

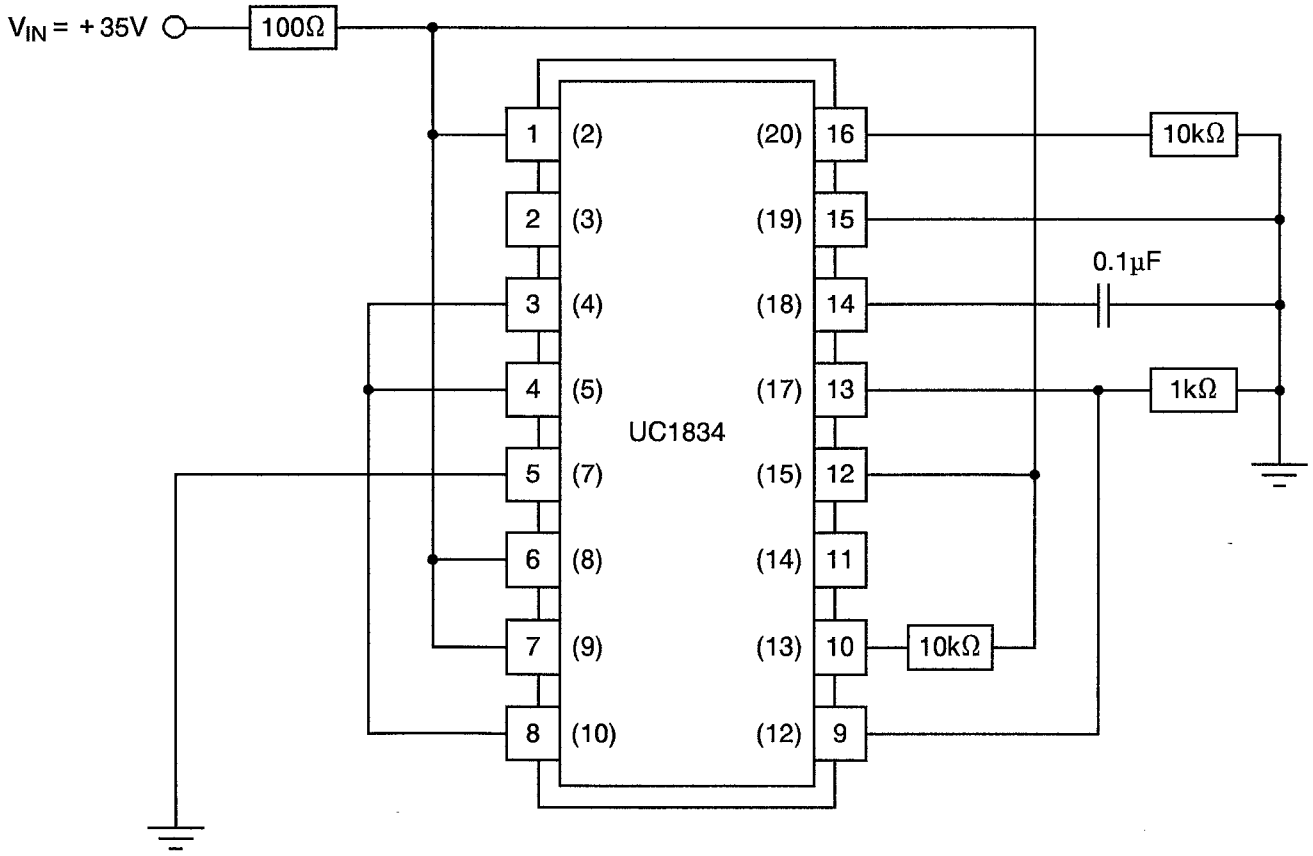
TABLE 5(b) - CONDITIONS FOR POWER BURN-IN AND OPERATING LIFE TESTS

No.	CHARACTERISTICS	SYMBOL	CONDITION	UNIT
1	Ambient Temperature	T_{amb}	+125(+5−0)	°C
2	Positive Supply Voltage	V_{IN+}	35	V
3	Negative Supply Voltage	V_{IN-}	0	V

FIGURE 5(a) - ELECTRICAL CIRCUIT FOR HIGH TEMPERATURE REVERSE BIAS BURN-IN

Not applicable.

FIGURE 5(b) - ELECTRICAL CIRCUIT FOR POWER BURN-IN AND OPERATING LIFE TESTS



NOTES

1. Pin numbers in parenthesis are for the chip carrier package.
2. All resistors are 5% tolerance (1% for construction purposes when possible), 1/8W @ 125°C.
3. All capacitors are 10% tolerance, rated 50V @ +125°C.

4.8 ENVIRONMENTAL AND ENDURANCE TESTS (CHARTS IV AND V OF ESA/SCC GENERIC SPECIFICATION NO. 9000)

4.8.1 Electrical Measurements on Completion of Environmental Tests

The parameters to be measured on completion of environmental tests are scheduled in Table 6. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.8.2 Electrical Measurements at Intermediate Points during Endurance Tests

The parameters to be measured at intermediate points during endurance tests are as scheduled in Table 6 of this specification. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.8.3 Electrical Measurements on Completion of Endurance Tests

The parameters to be measured on completion of endurance testing are as scheduled in Table 6 of this specification. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.8.4 Conditions for Operating Life Tests

The requirements for operating life testing are specified in Section 9 of ESA/SCC Generic Specification No. 9000. The conditions for operating life testing shall be as specified in Table 5(b) of this specification.

4.8.5 Electrical Circuits for Operating Life Tests

Circuits for use in performing the operating life tests are shown in Figure 5(b) of this specification.

4.8.6 Conditions for High Temperature Storage Test

The requirements for the high temperature storage test are specified in ESA/SCC Generic Specification No. 9000. The temperature to be applied shall be the maximum storage temperature specified in Table 1(b) of this specification.

TABLE 6 - ELECTRICAL MEASUREMENTS ON COMPLETION OF ENVIRONMENTAL TESTS AND AT INTERMEDIATE POINTS AND ON COMPLETION OF ENDURANCE TESTING

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	CHANGE LIMITS (Δ)	ABSOLUTE		UNIT
						MIN.	MAX.	
1	Supply Current (Standby)	I_{CC}	As per Table 2	As per Table 2	±10%	-	7.0	mA
2	Output Voltage (Referenced to V_{IN-})	V_{REF1}	As per Table 2	As per Table 2	±0.5%	1.485	1.515	V
5	Output Voltage (Referenced to V_{IN+})	V_{REF2}	As per Table 2	As per Table 2	±1.0%	−2.04	−1.96	V
7	Input Offset Voltage	V_{IO}	As per Table 2	As per Table 2	±5.0%	-	6.0	mV
8 to 9	Input Bias Current	I_{IB}	As per Table 2	As per Table 2	±0.4μA or (2) ±100%	-	−4.0	μA
10	Input Offset Current	I_{IO}	As per Table 2	As per Table 2	±0.1μA or (2) ±100%	-	1.0	μA

NOTES

1. The change limits (Δ) are applicable to the Operating Life test only. The change in parameters between initial and end point measurements shall not exceed the limits given. In addition, the absolute limits shall not be exceeded.
2. Whichever is greater, referred to the initial value.

APPENDIX 'A'

AGREED DEVIATIONS FOR UNITRODE (USA)

ITEMS AFFECTED	DESCRIPTION OF DEVIATIONS
Para. 4.2.1	ESA/SCC No. 21400 (S.E.M. Inspection) may be replaced by MIL-STD-883, Test Method 2018.
Para. 4.2.2	ESA/SCC No. 20400 (Internal Visual Inspection) may be replaced by MIL-STD-883, Test Method 2010, Condition A. ESA/SCC No. 20500 (Physical Dimensions) may be replaced by MIL-STD-2016.
Paras. 4.2.2, 4.2.3, 4.2.4 and 4.2.5	ESA/SCC No. 20500 (External Visual Inspection) may be replaced by MIL-STD-883, Test Method 2009.
Paras. 4.2.4 and 4.2.5	ESA/SCC No. 24800 (Permanence of Marking) may be replaced by MIL-STD-883, Test Method 2015.
	Lot information according to ESA/SCC Generic Specification No. 9000, Para. 10.1 will be on the front page of the data package but not repeated on each page of the documentation.