MONOLITHIC MICROWAVE INTEGRATED CIRCUIT (MMIC), GaAs, TRAVELLING WAVE AMPLIFIER BASED ON TYPE P35-4150

ESCC Detail Specification No. 9012/001

ISSUE 1

October 2002

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ESA/SCC Detail Specification No. 9012/001

space components
coordination group

Issue/Rev.	Date	Approved by	
		SCCG Chairman	ESA Director General or his Deputy
Issue 1	January 1998		

DOCUMENTATION CHANGE NOTICE

Rev. Letter	Rev. Date	Reference	CHANGE Item	Approved DCR No.

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APPENDICES (Applicable to specific Manufacturers only)

1. GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics, test and inspection data for 2.0 to 18GHz MMIC, GaAs Travelling Wave Amplifier, based on P35-4150. It shall be read in conjunction with ESA/SCC Generic Specification No. 9010, the requirements of which are supplemented herein.

1.2 COMPONENT TYPE VARIANTS

Variants of the basic type MMIC specified herein, which are also covered by this specification, are given in Table 1(a).

1.3 MAXIMUM RATINGS

The maximum ratings, which shall not be exceeded at any time during use or storage, applicable to the MMICs specified herein, are scheduled in Table 1(b).

1.4 PARAMETER DERATING INFORMATION

The derating information applicable to the MMICs specified herein is given in Figure 1.

1.5 PHYSICAL DIMENSIONS

The physical dimensions of the MMICs specified herein are shown in Figure 2.

1.6 FUNCTIONAL DIAGRAM

The functional diagram, showing pad and lead identification of the MMICs specified herein, is shown in Figure 3.

1.7 HANDLING PRECAUTIONS

These devices are susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacture, testing, packaging, shipment and handling.

These devices are categorised as Class 1 with a Minimum Critical Path Failure Voltage of 200V.

2. APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:-

(a) ESA/SCC Generic Specification No. 9010 for Monolithic Microwave Integrated Circuits (MMICs).

(b) MIL-STD-750, Test Methods and Procedures for Semiconductor Devices.

TABLE 1(a) - TYPE VARIANTS

VARIANT	BASED ON TYPE	CASE	FIGURE	LEAD MATERIAL AND FINISH
01	P35-4150-0	Naked Dice	2(a)	N/A
02	P35-4150-1	Flat Pack	2(b)	G7

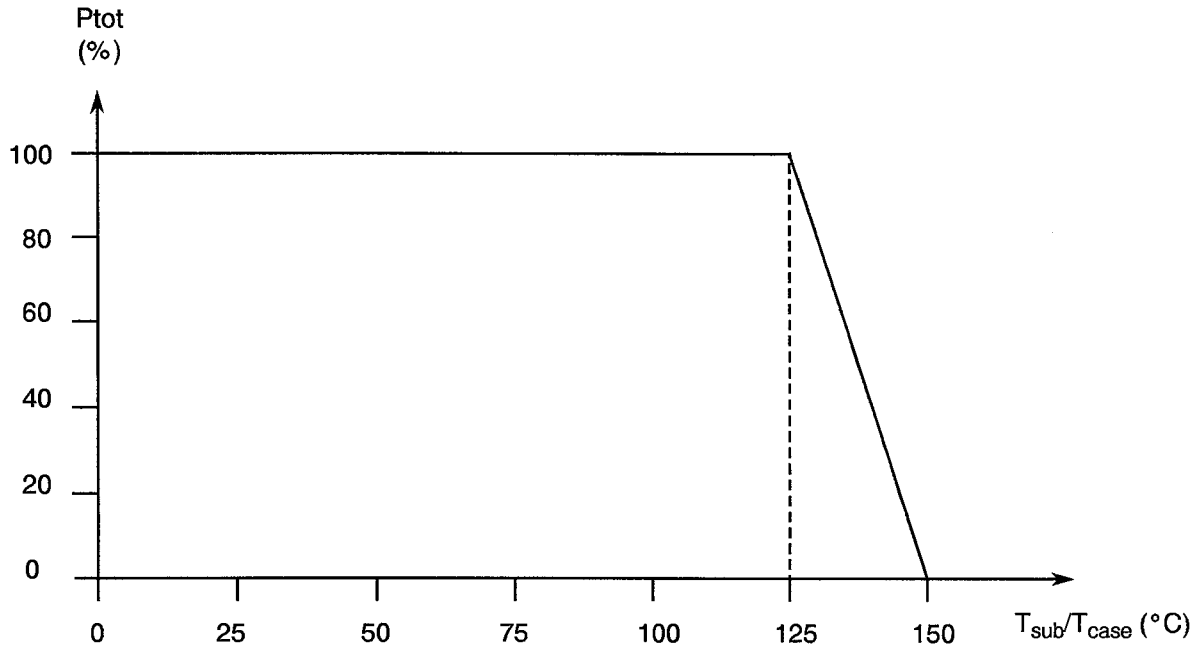
TABLE 1(b) - MAXIMUM RATINGS

No.	CHARACTERISTICS	SYMBOL	MAXIMUM RATING	UNIT	REMARKS
1	Drain to Source Voltage Variant 01 Variant 02	V_{DS}	 6.0 8.0	V	
2	Gate to Source Voltage	V_{GS}	−3.0	V	
3	Drain Current	I_D	120	mA	Note 1
4	Maximum RF Input Power	P_{IN}	17	dBM	
5	Power Dissipitation Variant 01 Variant 02	P_{tot}	 480 700	mW	Notes 2 and 3
6	Operating Temperature Range Variant 01 Variant 02	T_{op}	−65 to +150	°C	 T_{sub} T_{case}
7	Storage Temperature Range	T_{stg}	−65 to +150	°C	
8	Soldering Temperature Variant 01 Variant 02	T_{sol}	 +310 +200	°C	 Note 4 Note 5

NOTES

1. At V_{GS} of 0V, drain current (I_D) may exceed 120mA. V_{GS} should therefore be set to -0.6V maximum before applying V_{DS}.
2. At T_{sub} or T_{case} = +125°C. For derating at T_{sub} or T_{case} > +125°C, see Figure1.
3. Thermal impedance from FET channel to die backface is 52°C/W for dice which are mounted using <25µm of AuSn eutectic solder (80:20). Maximum recommended bias is V_{DS} = 6.0V for Variant 01 and 8.0V for Variant 02 at I_D = 80mA. Variant 02 uses an internal 35Ω series resistor on V_D which does not affect FET Thermal Impedance.
4. Duration 120 seconds maximum during die attachment.
5. Duration 30 seconds maximum and the same termination shall not be resoldered until 3 minutes have elapsed.

FIGURE 1 - PARAMETER DERATING INFORMATION



Power Dissipation versus Temperature

3. TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESA/SCC Basic Specification No. 21300 shall apply. In addition the following symbols are used:-

V_{DS} = Drain to Source Voltage.
V_{GS} = Gate to Source Voltage.
I_D = Drain Current.
$V_{GS(th)}$ = Gate Threshold Voltage.
I_{GS} = Gate to Source Leakage Current.

4. REQUIREMENTS

4.1 GENERAL

The complete requirements for procurement of the MMICs specified herein shall be stated in this specification and ESA/SCC Generic Specification No. 9010 for Monolithic Microwave Integrated Circuits (MMICs). Deviations from the Generic Specification, applicable to this specification only, are listed in Para. 4.2.

Deviations from the applicable Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESA/SCC requirements and do not affect the components' reliability, are listed in the appendices attached to this specification.

4.2 DEVIATIONS FROM GENERIC SPECIFICATION

4.2.1 Deviations from Production Control

(a) Para. 5.2.3 Total Dose Radiation Testing: Shall not be performed.

4.2.2 Deviations from Final Production Tests (Chart II)

None.

4.2.3 Deviations from Burn-in and Electrical Measurements (Chart III)

(a) Para. 9.15, High Temperature Reverse Bias test and subsequent electrical measurements related to this test shall be omitted.

4.2.4 Deviations from Qualification Tests (Chart IV)

(a) Para. 9.27, Special Testing: Shall not be performed.

4.2.5 Deviations from Lot Acceptance Tests (Chart V)

(a) Para. 9.27, Special Testing: Shall not be performed.

4.3 MECHANICAL REQUIREMENTS

4.3.1 Dimension Check

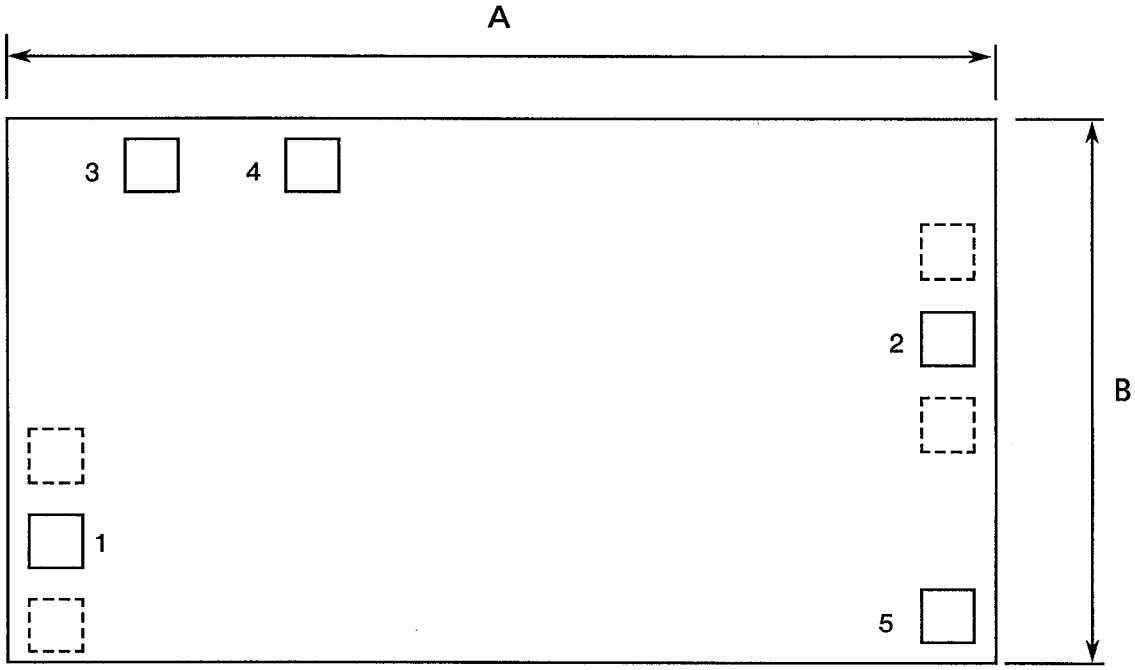
The dimensions of the MMICs specified herein shall be checked. They shall conform to those shown in Figure 2.

4.3.2 Weight

The maximum weight of the MMICs specified herein shall be 10 milligrammes for Variant 01 and 0.5 grammes for Variant 02.

FIGURE 2 - PHYSICAL DIMENSIONS

FIGURE 2(a) - NAKED DICE



Die thickness: 200 ± 20 µm.

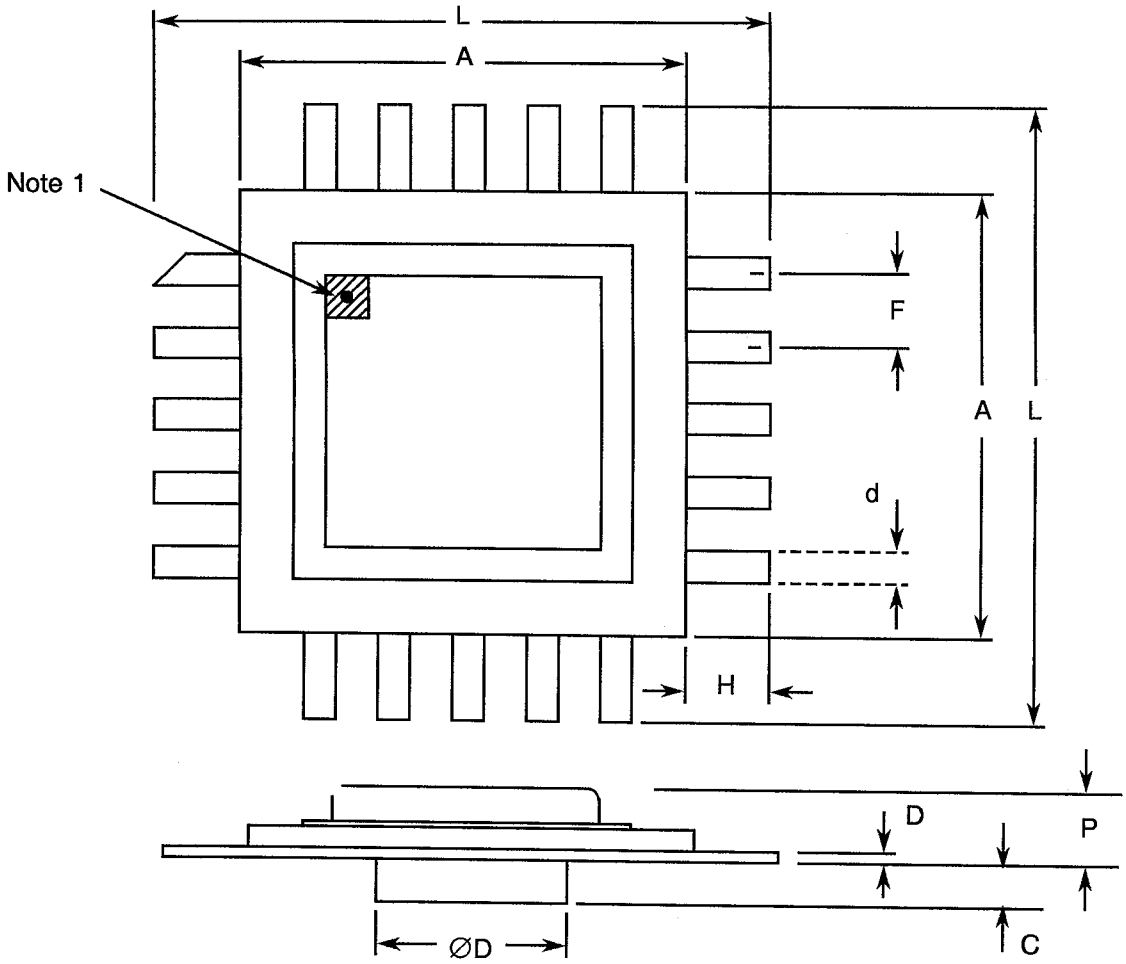
Symbol	Micrometres	
	Min.	Max.
A	2110	2210
B	2034	2134

NOTES

1. --- = Ground.

FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)

FIGURE 2(b) - FLAT PACKAGE, 20-PIN



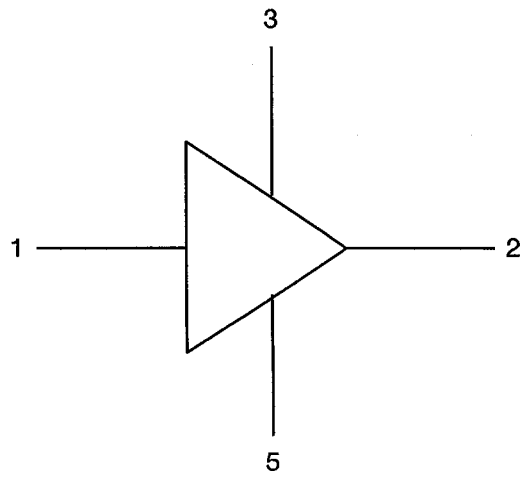
Symbol	Millimetres		Notes
	Min.	Max.	
A	7.80	8.04	-
C	-	0.83	Heatsink
D	0.10	0.16	Leadframe
d	0.47	0.77	2
ØD	-	3.30	-
F	1.15	1.39	3
H	0.80	1.40	-
L	9.70	10.10	-
P	-	2.90	-

NOTES

1. Index area, a dot shall be located adjacent to Pin 1 and shall be within the shaded area shown. Pin 1 shall also be cropped as shown. For pin numbering, see Para. 4.5.2.2.
2. All leads.
3. 16 spaces.

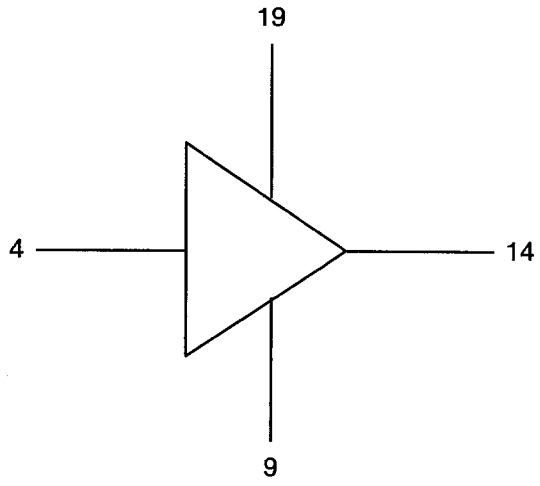
FIGURE 3 - FUNCTIONAL DIAGRAM

FIGURE 3(a) - VARIANT 01



Pad No.	Function
1	RF in
2	RF out
3	V_D
4	Not used
5	V_G
Chip Backface	GND

FIGURE 3(b) - VARIANT 02



Pin No.	Function
4	RF in
9	V_G
14	RF out
19	V_D
1, 3, 5, 6, 8, 10, 11, 13, 15, 16, 18, 20	GND
2, 7, 12, 17	Not used

4.3.3 Terminal Strength

The requirements for terminal strength testing are specified in Section 9 of ESA/SCC Generic Specification No. 9010. For Variant 02, the test conditions shall be as follows:-

(a) Condition: 'A' (Tension).
(b) Force: 0.227 kg.
(c) Duration: 30 seconds.

4.3.4 Bond Strength

The requirements for bond strength testing are specified in Section 9 of ESA/SCC Generic Specification No. 9010. For Variant 02, the test conditions shall be as follows:-

(a) Condition: 'D'.
(b) Bond Strength: 3.0g force minimum.

4.3.5 Die Shear

The requirements for die shear testing are specified in Section 9 of ESA/SCC Generic Specification No. 9010. For Variant 02, the test conditions shall be as follows:-

(a) Minimum acceptable die shear strength: 2.5kg.
3.125kg = less than 50% adhesion.
5.0kg = less than 10% adhesion.

4.4 MATERIALS AND FINISHES

The materials and finishes shall be as specified herein. Where a definite material is not specified, a material which will enable the MMICs specified herein to meet the performance requirements of this specification shall be used. Acceptance or approval of any constituent material shall not guarantee acceptance of the finished product.

4.4.1 Case

For Variant 02, the case shall be hermetically sealed and have a ceramic body. The lid shall be preform soldered.

4.4.2 Pad/Lead Material and Finish

For Variant 01, the pad and die backface metallisation material shall be TiPtAu with a minimum pad thickness of 2.4 μm of gold.

For Variant 02, the lead material shall be Type 'G' with Type '7' finish in accordance with the requirements of ESA/SCC Basic Specification No. 23500 (see Table 1(a) for Type Variants).

4.5 MARKING

4.5.1 General

The marking for naked dice delivered to this specification shall be made on the delivery package and shall be limited to the SCC Component Number as specified in Para. 4.5.3, Traceability Information as specified in Para. 4.5.4 and the "ESD SENSITIVE" label specified at the end of this paragraph.

The marking of all components delivered to this specification shall be in accordance with the requirements of ESA/SCC Basic Specification No. 21700 and the following paragraphs. When the component is too small to accomodate all of the marking specified, as much as space permits shall be marked, and the marking information, in full, shall accompany the component in its primary package.

The information to be marked and the order of precedence, shall be as follows:-

(a) Lead Identification.

(b) The SCC Component Number.

(c) Traceability Information.

The primary package shall bear an "ESD SENSITIVE" label.

4.5.2 Pad/Lead Identification

4.5.2.1 Pad Identification

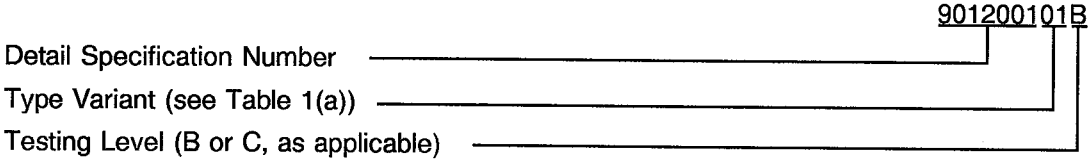
Pad identification shall be as shown in Figures 2(a) and 3(a) of this specification.

4.5.2.2 Lead Identification

Lead identification shall be as shown in Figures 2(b) and 3(b) of this specification. An index shall be located on the top of the package in the position defined in Note 1 to Figure 2(b). The pin numbering shall be read in a counter-clockwise direction with the index on the left-hand side.

4.5.3 The SCC Component Number

Each component shall bear the SCC Component Number which shall be constituted and marked as follows:



4.5.4 Traceability Information

Each component shall be marked in respect of traceability information in accordance with the requirements of ESA/SCC Basic Specification No. 21700.

4.6 ELECTRICAL MEASUREMENTS

4.6.1 Electrical Measurements at Room Temperature

The parameters to be measured at room temperature are scheduled as follows:-

(a) Table 2(a) - D.C. parameters for probe and pin measurement.

(b) Table 2(b) - R.F. parameters for probe measurement.

(c) Table 2(c) - R.F. parameters for pin measurement.

Unless otherwise specified, the measurements shall be performed at $T_{amb} = 22 \pm 3$ °C.

4.6.2 Electrical Measurements at High and Low Temperatures

The parameters to be measured at high and low temperatures are scheduled as follows:-

(a) Table 3(a) - D.C. and R.F. parameters for probe measurement.

(b) Table 3(b) - D.C. parameters for pin measurement.

Unless otherwise specified, the measurements shall be performed at $T_{amb} = +125(+0-3)$ °C.

4.6.3 Circuits for Electrical Measurements

Circuits for use in performing the electrical measurements listed in Tables 2 and 3 of this specification are shown in Figure 4 of this specification.

4.7 BURN-IN TESTS

4.7.1 Parameter Drift Values

The parameter drift values applicable to burn-in are specified in Table 4 of this specification. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C. The parameter drift values (Δ) applicable to the parameters scheduled, shall not be exceeded. In addition to these drift value requirements, the appropriate limit value specified for a given parameter in Table 2 shall not be exceeded.

4.7.2 Conditions for High Temperature Reverse Bias Burn-in (Table 5(a))

Not applicable.

4.7.3 Conditions for Power Burn-in

The requirements for power burn-in are specified in Section 9 of ESA/SCC Generic Specification No. 9010. The conditions for power burn-in shall be as specified in Table 5(b) of this specification.

4.7.4 Electrical Circuits for High Temperature Reverse Bias Burn-in (Figure 5(a))

Not applicable.

4.7.5 Electrical Circuits for Power Burn-in

Circuits for use in performing the power burn-in tests are shown in Figure 5(b) of this specification.

TABLE 2(a) - ELECTRICAL MEASUREMENT AT ROOM TEMPERATURE - D.C. PARAMETERS FOR PROBE AND PIN MEASUREMENTS

No.	CHARACTERISTICS	SYMBOL	MIL-STD-750 TEST METHOD	TEST FIGURE	TEST CONDITIONS	LIMITS		UNIT
						MIN.	MAX.	
1	Gate Threshold Voltage	$V_{GS(th)}$	3403	4(a)	$I_D = 0.5mA$ $V_{DS} = 5.0V$	−1.2	−2.5	V
2	Gate to Source Leakage Current Variant 01 Variant 02	I_{GS}	3411 Bias Cond. C	4(a)	$I_D = 0.5mA$ $V_{DS} = 5.0V$ $V_{GS(th)}$ = Note 1.	 - -	 −30 −20	µA

NOTES

1. The Gate Threshold Voltage is adjusted to achieve $I_D = 0.5mA$ and the Leakage Current is then measured.

TABLE 2(b) - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - R.F. PARAMETERS FOR PROBE MEASUREMENTS

No.	CHARACTERISTICS	SYMBOL	MIL-STD-750 TEST METHOD	TEST FIGURE	TEST CONDITIONS	LIMITS		UNIT
						MIN.	MAX.	
3	Small Signal Gain	S21	3570	4(b)	$V_{DS} = 5.0V$ $P_{IN} = -10dBm$ $I_D = 60mA$ f = 2.0 to 18GHz (Swept)	5.0	-	dB
4	Input Return Loss	S11	3570	4(b)	$V_{DS} = 5.0V$ $P_{IN} = -10dBm$ $I_D = 60mA$ f = 2.0 to 18GHz (Swept)	9.0	-	dB
5	Output Return Loss	S22	3570	4(b)	$V_{DS} = 5.0V$ $P_{IN} = -10dBm$ $I_D = 60mA$ f = 2.0 to 18GHz (Swept)	8.0	-	dB
6	Reverse Isolation	S12	3570	4(b)	$V_{DS} = 5.0V$ $P_{IN} = -10dBm$ $I_D = 60mA$ f = 2.0GHz f = 18GHz	 26 12	 - -	dB
7	Noise Figure	NF	3246	4(c)	$V_{DS} = 5.0V$ $I_D = 60mA$ f = 2.0 to 18GHz (Swept) (Note 1)	-	8.5	dB

NOTES

1. Measurements shall be performed on a sample basis, 5 dice per wafer.

TABLE 2(b) - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - R.F. PARAMETERS FOR PROBE MEASUREMENTS (CONT.)

No.	CHARACTERISTICS	SYMBOL	MIL-STD-750 TEST METHOD	TEST FIGURE	TEST CONDITIONS	LIMITS		UNIT
						MIN.	MAX.	
8	Output Power at 1dB Gain Compression	P-1dB	3510	4(d)	V_{DS} = 5.0V I_D = 60mA f = 2.0GHz f = 18GHz (Note 1)	 17 14	 - -	dBm

NOTES
1. Measurements shall be performed on a sample basis, 5 dice per wafer.

TABLE 2(c) - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - R.F. PARAMETERS FOR PIN MEASUREMENTS

No.	CHARACTERISTICS	SYMBOL	MIL-STD-750 TEST METHOD	TEST FIGURE	TEST CONDITIONS	LIMITS (1)		UNIT
						MIN.	MAX.	
3	Small Signal Gain	S21	3570	4(b)	V_{DS} = 7.0V P_{IN} = − 10dBm I_D = 60mA f = 2.0 to 10GHz (Swept)	4.5	-	dB
4	Input Return Loss	S11	3570	4(b)	V_{DS} = 7.0V P_{IN} = − 10dBm I_D = 60mA f = 2.0 to 10GHz (Swept)	8.0	-	dB
5	Output Return Loss	S22	3570	4(b)	V_{DS} = 7.0V P_{IN} = − 10dBm I_D = 60mA f = 2.0 to 10GHz (Swept)	6.0	-	dB
6	Reverse Isolation	S12	3570	4(b)	V_{DS} = 7.0V P_{IN} = − 10dBm I_D = 60mA f = 2.0GHz	20	-	dB
7	Noise Figure	NF	3246	4(c)	V_{DS} = 7.0V I_D = 60mA f = 2.0 to 10GHz (Swept)	-	9.0	dB
8	Output Power at 1dB Gain Compression	P-1dB	3510	4(d)	V_{DS} = 7.0V I_D = 60mA f = 2.0GHz	17	-	dBm

NOTES
1. Measured in test jig ETF-9000. These values include a contribution from the test jig so performance may vary with each test jig.

TABLE 3(a) - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES - D.C. AND R.F. PARAMETERS FOR PROBE MEASUREMENTS

No.	CHARACTERISTICS	SYMBOL	MIL-STD-750 TEST METHOD	TEST FIGURE	TEST CONDITIONS	LIMITS		UNIT
						MIN.	MAX.	
1	Gate Threshold Voltage	$V_{GS(th)}$	3403	4(a)	V_{DS} = 5.0V I_D = 0.5mA	-	−3.0	V
2	Gate to Source Leakage Current	I_{GS}	3411 Bias Cond. C	4(a)	V_{DS} = 5.0V I_D = 0.5mA $V_{GS(th)}$ = Note 1.	-	−20	µA
3	Small Signal Gain	S21	3570	4(b)	V_{DS} = 5.0V P_{IN} = −10dBm I_D = 60mA f = 2.0 to 12GHz (Swept)	3.8	-	dB
6	Reverse Isolation	S12	3570	4(b)	V_{DS} = 5.0V P_{IN} = −10dBm I_D = 60mA f = 2.0GHz	20	-	dB
7	Noise Figure	NF	3246	4(c)	V_{DS} = 5.0V I_D = 60mA f = 2.0 to 12GHz (Swept)	-	9.5	dB

NOTES

1. The Gate Threshold Voltage is adjusted to achieve I_D = 0.5mA and the Leakage Current is then measured.

TABLE 3(b) - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES - D.C. PARAMETERS FOR PIN MEASUREMENTS

No.	CHARACTERISTICS	SYMBOL	MIL-STD-750 TEST METHOD	TEST FIGURE	TEST CONDITIONS	LIMITS		UNIT
						MIN.	MAX.	
1	Gate Threshold Voltage	$V_{GS(th)}$	3403	4(a)	V_{DS} = 5.0V I_D = 0.5mA	-	−3.0	V
2	Gate to Source Leakage Current	I_{GS}	3411 Bias Cond. C	4(a)	V_{DS} = 5.0V I_D = 0.5mA $V_{GS(th)}$ = Note 1.	-	−20	µA

NOTES

1. The Gate Threshold Voltage is adjusted to achieve I_D = 0.5mA and the Leakage Current is then measured.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS

FIGURE 4(a) - D.C. AUTOMATIC TEST EQUIPMENT

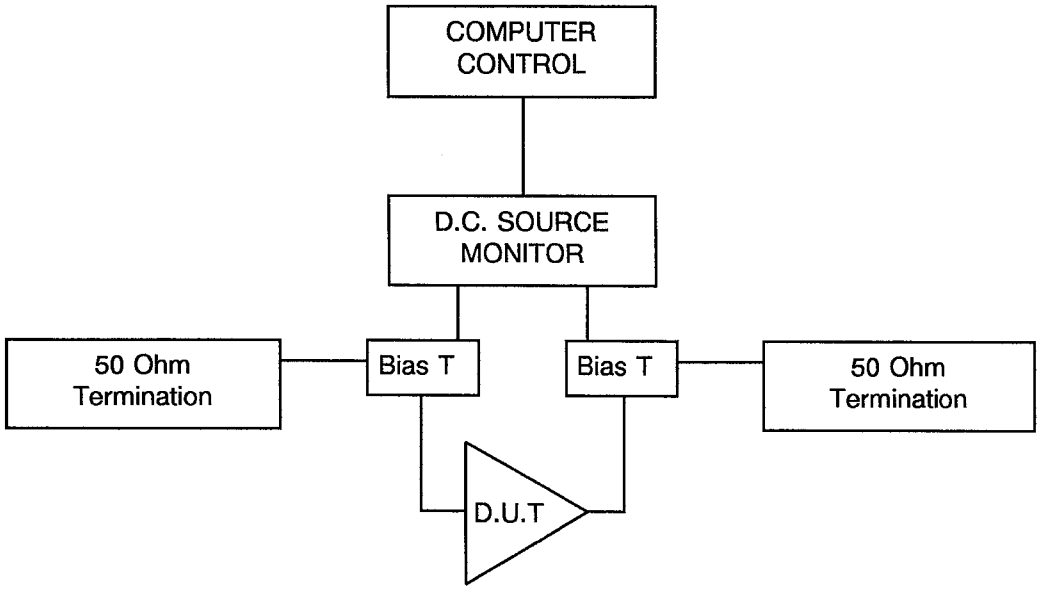


FIGURE 4(b) - S-PARAMETER MEASUREMENT EQUIPMENT

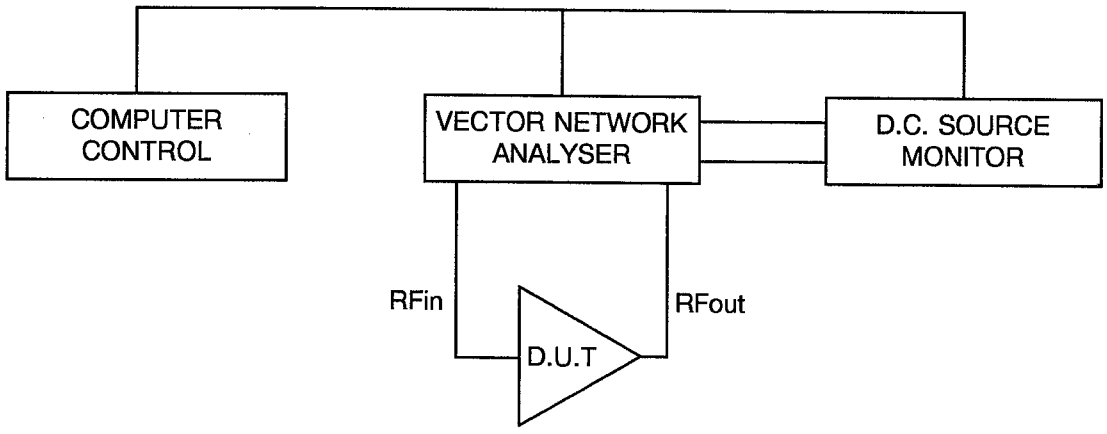


FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS

FIGURE 4(c) - NOISE FIGURE MEASUREMENT EQUIPMENT

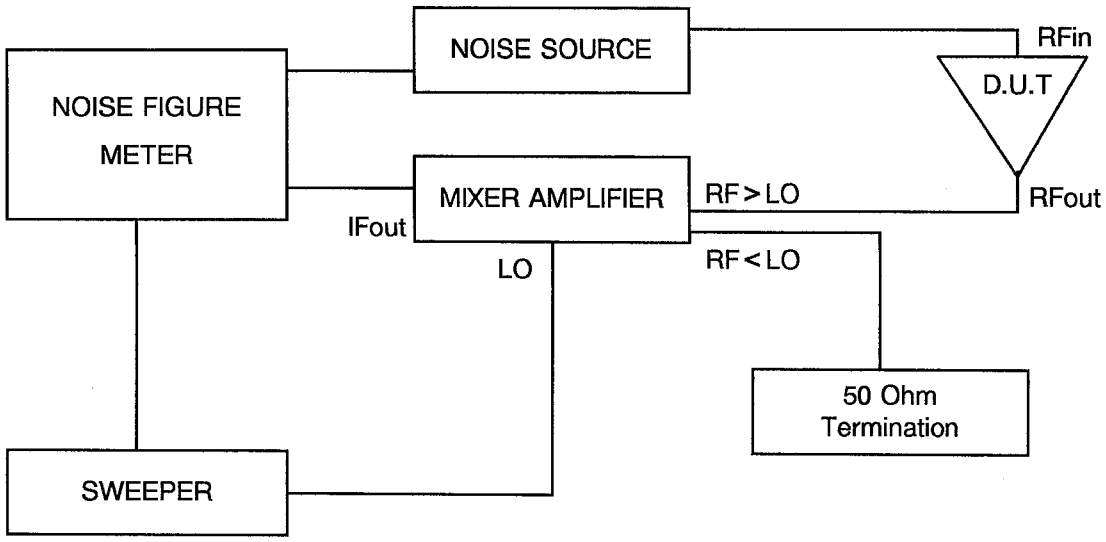


FIGURE 4(d) - GAIN COMPRESSION MEASUREMENT EQUIPMENT

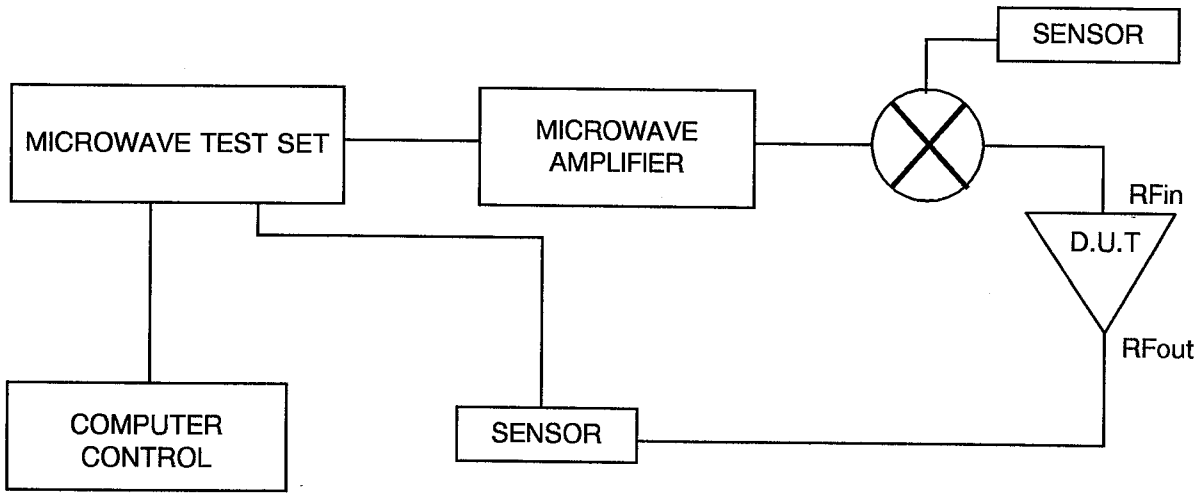


TABLE 4 - PARAMETER DRIFT VALUES

No.	CHARACTERISTICS	SYMBOL	SPEC AND/OR TEST METHOD	TEST CONDITIONS	CHANGE LIMITS (Δ)	UNIT
1	Gate Threshold Voltage	$V_{GS(th)}$	As per Table 2(a)	As per Table 2(a)	±10	%
2	Gate to Source Leakage Current	I_{GS}	As per Table 2(a)	As per Table 2(a)	+5.0	µA
3	Small Signal Gain	S21	As per Table 2(c)	As per Table 2(c)	±0.5	dB
4	Input Return Loss	S11	As per Table 2(c)	As per Table 2(c)	±1.0	dB
5	Output Return Loss	S22	As per Table 2(c)	As per Table 2(c)	±1.0	dB
6	Reverse Isolation	S12	As per Table 2(c)	As per Table 2(c)	±1.0	dB
7	Noise Figure	NF	As per Table 2(c)	As per Table 2(c)	±0.5	dB
8	Output Power at 1dB Gain Compression	P-1dB	As per Table 2(c)	As per Table 2(c)	±0.5	dBm

TABLE 5(a) - CONDITIONS FOR HIGH TEMPERATURE REVERSE BIAS BURN-IN

Not applicable.

TABLE 5(b) - CONDITIONS FOR POWER BURN-IN AND OPERATING LIFE TESTS

No.	CHARACTERISTICS	SYMBOL	CONDITION	UNIT
1	Case Temperature	T_{case}	+125(+0−3)	°C
2	Drain to Source Voltage	V_{DS}	7.0	V
3	Gate to Source Voltage	V_{GS}	Note 1	V
4	Drain Current	I_D	60	mA

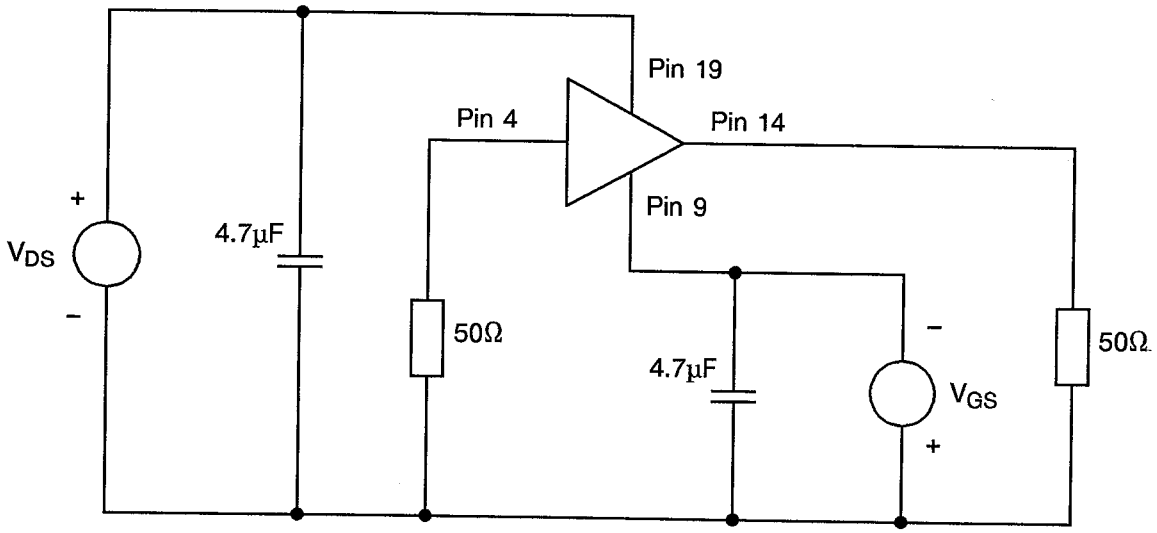
NOTES

1. Gate to Source Voltage to be adjusted at the beginning of the test to achieve $I_D = 60mA$.

FIGURE 5(a) - ELECTRICAL CIRCUIT FOR HIGH TEMPERATURE REVERSE BIAS BURN-IN

Not applicable.

FIGURE 5(b) - ELECTRICAL CIRCUIT FOR POWER BURN-IN AND OPERATING LIFE TESTS



PIN No.	FUNCTION
4	RF in
9	V_G
14	RF out
19	V_D

4.8 ENVIRONMENTAL AND ENDURANCE TESTS (CHARTS IV AND V OF ESA/SCC GENERIC SPECIFICATION No. 9010)

4.8.1 Electrical Measurements on Completion of Environmental Tests

The parameters to be measured on completion of environmental tests are scheduled in Table 6 of this specification. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.8.2 Electrical Measurements at Intermediate Points and on Completion of Endurance Tests

The parameters to be measured at intermediate points and on completion of endurance testing are scheduled in Table 6 of this specification. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.8.3 Conditions for Operating Life Tests (Part of Endurance Testing)

The requirements for operating life testing are specified in Section 9 of ESA/SCC Generic Specification No. 9010. The conditions for operating life testing shall be the same as specified in Table 5(b) for the power burn-in test.

4.8.4 Electrical Circuits for Operating Life Tests

The circuit to be used for performance of the operating life test shall be the same as shown in Figure 5(b) for power burn-in.

4.9 TOTAL DOSE IRRADIATION TESTING

Not applicable.

4.10 SPECIAL TESTING

Not applicable.

TABLE 6 - ELECTRICAL MEASUREMENTS ON COMPLETION OF ENVIRONMENTAL TESTS AND AT INTERMEDIATE POINTS AND ON COMPLETION OF ENDURANCE TESTING

No.	CHARACTERISTICS	SYMBOL	SPEC AND/OR TEST METHOD	TEST CONDITIONS	LIMITS		UNIT
					MIN.	MAX.	
1	Gate Threshold Voltage	$V_{GS(th)}$	As per Table 2(a)	As per Table 2(a)	−1.2	−2.5	V
2	Gate to Source Leakage Current	I_{GS}	As per Table 2(a)	As per Table 2(a)	-	−30	µA
3	Small Signal Gain	S21	As per Table 2(c)	As per Table 2(c)	4.5	-	dB
4	Input Return Loss	S11	As per Table 2(c)	As per Table 2(c)	7.5	-	dB
5	Output Return Loss	S22	As per Table 2(c)	As per Table 2(c)	5.0	-	dB
6	Reverse Isolation	S12	As per Table 2(c)	As per Table 2(c) f = 2.0GHz	19	-	dB
7	Noise Figure	NF	As per Table 2(c)	As per Table 2(c)	-	9.5	dB
8	Output Power at 1dB Gain Compression	P-1dB	As per Table 2(c)	As per Table 2(c) f = 2.0GHz	16	-	dBm

FIGURE 6 - BIAS CONDITIONS FOR IRRADIATION TESTING

Not applicable.

TABLE 7 - ELECTRICAL MEASUREMENTS DURING AND ON COMPLETION OF IRRADIATION TESTING

Not applicable.

APPENDIX 'A'

AGREED DEVIATIONS FOR GMMT CASWELL (G.B.)

ITEMS AFFECTED	DESCRIPTION OF DEVIATIONS
Para. 4.2.1	Para. 5.2.2, SEM Inspection: May be performed to GMMT CL/QB/2156
Paras. 4.2.2, 4.2.3, 4.2.4 and 4.2.5	All electrical measurements may be made using test jig EFT-9000 with MLC20/8 packages. The test jig is manufactured by Triquint Semiconductor U.S.A. and has the following characteristics: - 8 x 50Ω SMA connectors. - Operating frequency range D.C. to 12 GHz. - Insertion Loss < 0.7dB. - Return Loss < 1.7dB.