INTEGRATED CIRCUITS, MONOLITHIC,

SILICON ON SAPPHIRE, CMOS LOCAL

TIME MANAGEMENT SYSTEM,

BASED ON TYPE MS-13196

ESCC Detail Specification No. 9544/007

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ESA/SCC Detail Specification No. 9544/007

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APPENDICES (Applicable to specific Manufacturers only)

1. GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics, test and inspection data for a monolithic, Silicon on Sapphire CMOS Local Time Management System, based on Type MS-13196. It shall be read in conjunction with ESA/SCC Generic Specification No. 9000, the requirements of which are supplemented herein.

1.2 COMPONENT TYPE VARIANTS

Variants of the basic type integrated circuits specified herein, which are also covered by this specification, are given in Table 1(a).

1.3 MAXIMUM RATINGS

The maximum ratings, which shall not be exceeded at any time during use or storage, applicable to the integrated circuits specified herein, are as scheduled in Table 1(b).

1.4 PARAMETER DERATING INFORMATION (FIGURE 1)

Not applicable.

1.5 PHYSICAL DIMENSIONS

As per Figure 2.

1.6 PIN ASSIGNMENT

As per Figure 3(a).

1.7 TRUTH TABLE

As per Figure 3(b).

1.8 CIRCUIT DESCRIPTION

As per Figure 3(c).

1.9 FUNCTIONAL DIAGRAM

As per Figure 3(d).

1.10 HANDLING PRECAUTIONS

These devices are susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacture, testing, packaging, shipment and any handling.

These components are categorised as Class 1 with a Minimum Critical Path Failure Voltage of 500 Volts.

1.11 INPUT/OUTPUT PROTECTION NETWORKS

Protection networks shall be incorporated into each input and output as shown in Figure 3(e).

TABLE 1(a) - TYPE VARIANTS

VARIANT	CASE	FIGURE	LEAD MATERIAL AND FINISH
01	FLAT	2(a)	D2

TABLE 1(b) - MAXIMUM RATINGS

No.	CHARACTERISTICS	SYMBOL	MAXIMUM RATINGS	UNIT	REMARKS
1	Supply Voltage	V_{DD}	−0.5 to +7.0	V	-
2	Input Voltage	V_{IN}	−0.5 to V_{DD} + 0.5	V	-
3	DC Input Current	I_{IN}	20	mA	-
4	DC Output Current	I_{OUT}	10	mA	Note 1
5	Device Dissipation (Continuous)	P_D	300	mWdc	-
6	Output Dissipation	P_{DSO}	50	mWdc	Note 1
7	Operating Temperature Range	T_{op}	−55 to +125	°C	T_{amb}
8	Storage Temperature Range	T_{stg}	−65 to +150	°C	-
9	Soldering Temperature	T_{sol}	+260	°C	Note 2

NOTES

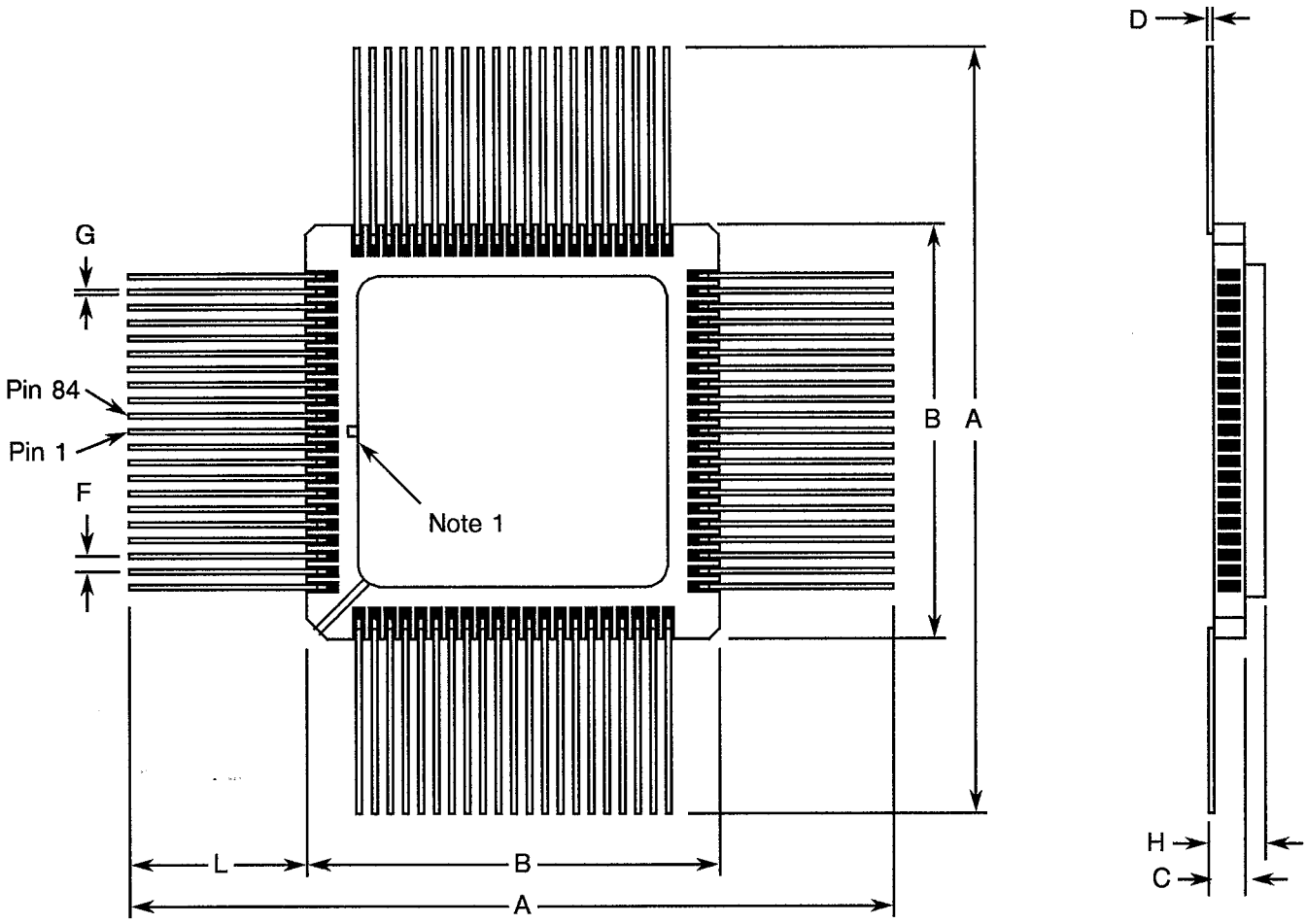
1. Single output.
2. Duration 5 seconds maximum at a distance of not less than 1.0mm from the device body and the same lead shall not be resoldered until 3 minutes have elapsed.

FIGURE 1 - PARAMETER DERATING INFORMATION

Not applicable.

FIGURE 2 - PHYSICAL DIMENSIONS

FIGURE 2 - FLAT PACKAGE, 84-PIN



SYMBOL	MILLIMETRES		NOTES
	MIN	MAX	
A	42.64	44.25	
B	23.14	23.75	
C	1.47	1.83	2, 5
D	0.10	0.20	
F	0.94	1.10	3, 4
G	0.17	0.33	2
H	1.80	2.31	
L	9.75	10.25	2

NOTES

1. Pin number 1 location.
2. All leads.
3. 80 spaces for flat package.
4. The true position pin spacing is xmm between centre lines. Each pin centreline is located within +/- 0.1mm of its true longitudinal position relative to pins 1 and 84.
5. The dimension is measured at the point of exit of the lead from the body.

FIGURE 3(a) - PIN ASSIGNMENT

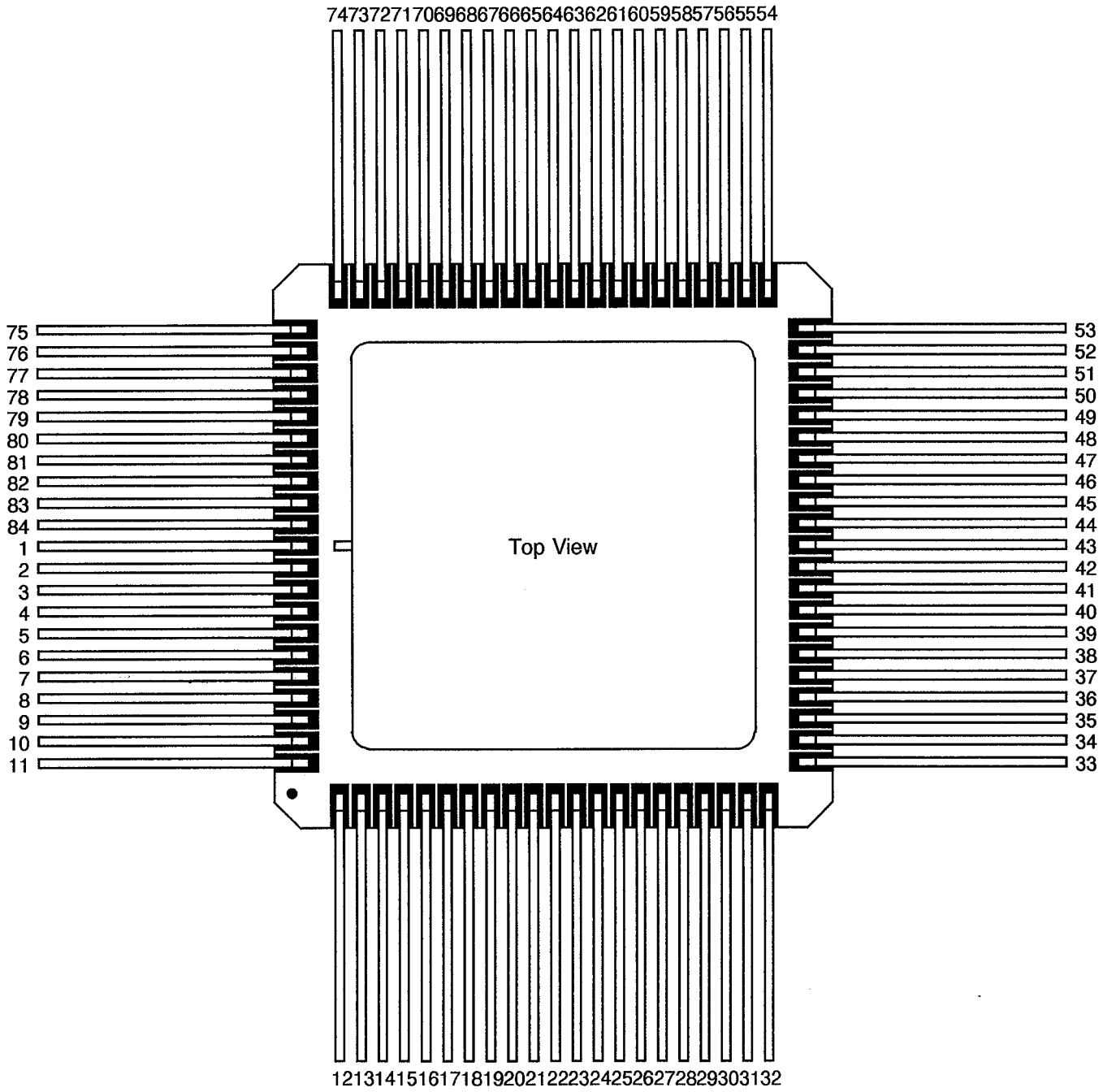


FIGURE 3(a) - PIN ASSIGNMENT (CONTINUED)

PIN DESCRIPTION

SYMBOL	FUNCTION	DESCRIPTION	PIN NUMBER
V_{DD}	Input	Positive Supply	1
D15	Data Input	CMOS Input/Output	2
D14	Data Input	CMOS Input/Output	3
D13	Data Input	CMOS Input/Output	4
D12	Data Input	CMOS Input/Output	5
V_{SS}	Input	Negative Supply	6
V_{DD}	Input	Positive Supply	7
D11	Data Input	CMOS Input/Output	8
D10	Data Input	CMOS Input/Output	9
D9	Data Input	CMOS Input/Output	10
D8	Data Input	CMOS Input/Output	11
V_{SS}	Input	Negative Supply	12
V_{DD}	Input	Positive Supply	13
D7	Data Input	CMOS Input/Output	14
D6	Data Input	CMOS Input/Output	15
D5	Data Input	CMOS Input/Output	16
D4	Data Input	CMOS Input/Output	17
V_{SS}	Input	Negative Supply	18
V_{DD}	Input	Positive Supply	19
D3	Data Input	CMOS Input/Output	20
D2	Data Input	CMOS Input/Output	21
D1	Data Input	CMOS Input/Output	22
D0	Data Input	CMOS Input/Output	23
V_{SS}	Input	Negative Supply	24
V_{DD}	Input	Positive Supply	25
WINDOW	CTMS Flag	Output	26
$\overline{\text{READY}}$	Ready	Output	27
$\overline{\text{RD}}$	Read Strobe	CMOS Input	28
$\overline{\text{CS}}$	Chip Select	CMOS Input	29
$\overline{\text{WR}}$	Write Strobe	CMOS Input	30
AD4	Address Internal Register	CMOS Input	31
AD3	Address Internal Register	CMOS Input	32
AD2	Address Internal Register	CMOS Input	33
AD1	Address Internal Register	CMOS Input	34
AD0	Address Internal Register	CMOS Input	35
MPROCLK	Microprocessor Clock	CMOS Input	36
TESTADDR0	Test Mode Select	CMOS Input	37
TESTADDR1	Test Mode Select	CMOS Input	38

FIGURE 3(a) - PIN ASSIGNMENT (CONTINUED)

PIN DESCRIPTION

SYMBOL	FUNCTION	DESCRIPTION	PIN NUMBER
MPROC	Microprocessor Selection	CMOS Input	39
EXTRIN	External Error	CMOS Input	40
ETSTRB	Elapsed Time Strobe	CMOS Input	41
SWEVENT	Stop Watch Event	CMOS Input	42
SWSTART	Stop Watch Start/Hold	CMOS Input	43
CLKF0	Bus Clock Frequency Selection	CMOS Input	44
CLKF1	Bus Clock Frequency Selection	CMOS Input	45
CLKF2	Bus Clock Frequency Selection	CMOS Input	46
ETTHR1	Elapsed Time Threshold	CMOS Input	47
ETTHR0	Elapsed Time Threshold	CMOS Input	48
GOTHR0	Go Threshold Selection	CMOS Input	49
GOTHR1	Go Threshold Selection	CMOS Input	50
SIN	Serial Input/ Sync Input	CMOS Input	51
SER	Serial/Parallel	CMOS Input	52
CTMSG	CTMS Message	CMOS Input	53
AUXTAL	Auxilliary 16MHz Clock Selection	CMOS Input	54
PFGPHIN	Waveform Generator Facility Phase In	CMOS Input	55
PFGMODE	Waveform Generator Facility Mode	CMOS Input	56
ETALRM	Elapsed Time Alarm	Output	57
TVLD	Time Valid	Output	58
PFGHOUT	Waveform Generator Facility Out	Output	59
V_{SS}	Input	Negative Supply	60
V_{DD}	Input	Positive Supply	61
PFGWAVE	Waveform Generator Facility Waveform	Output	62
EXTSHEN	External Shift Enable	Output	63
EXTDATA	External Data	Output	64
EXTELD	External Elapsed Time Load	Output	65
V_{SS}	Input	Negative Supply	66
V_{DD}	Input	Positive Supply	67
EXTDEMUX1	External Demultiplexer	Output	68
EXTDEMUX0	External Demultiplexer	Output	69
DPLLFREE	DPLL Free-Wheeling Flag	CMOS Input	70
DPLLINC	DPLL Down	CMOS Input	71
DPLLDEC	DPLL Up	CMOS Input	72
$\overline{\text{EXRST}}$	External Reset	CMOS Input	73
BUSCLK	Bus Clock	CMOS Input	74
XTAL1	Crystal Input	CMOS Input	75
XTAL2	Crystal Output	Output	76

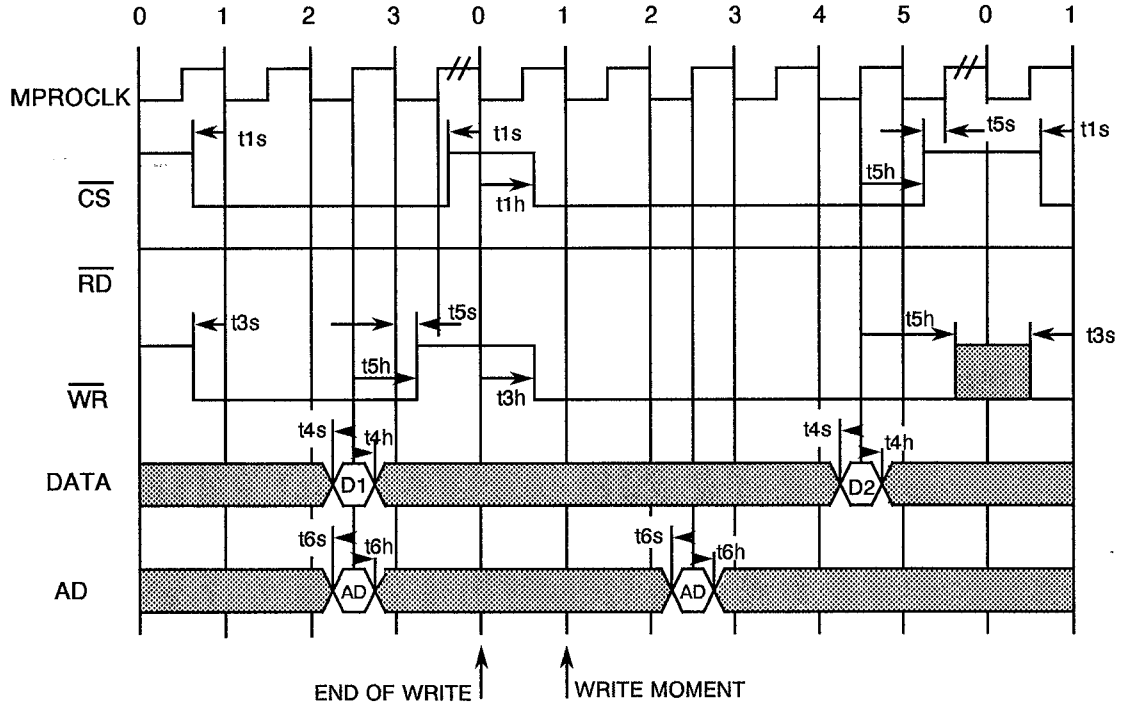
FIGURE 3(a) - PIN ASSIGNMENT (CONTINUED)

PIN DESCRIPTION

SYMBOL	FUNCTION	DESCRIPTION	PIN NUMBER
XTALCLK	Crystal Clock Output	Output	77
V_{SS}	Input	Negative Supply	78
V_{DD}	Input	Positive Supply	79
EXTCOUNT	External ET Counter Clock	Output	80
EXTCLK	External DPLL Clock	Output	81
MEANFREQ	Mean Frequency	Output	82
DPHASE	DPLL Phase Reference	Output	83
V_{SS}	Input	Negative Supply	84

FIGURE 3(b) - TRUTH TABLE

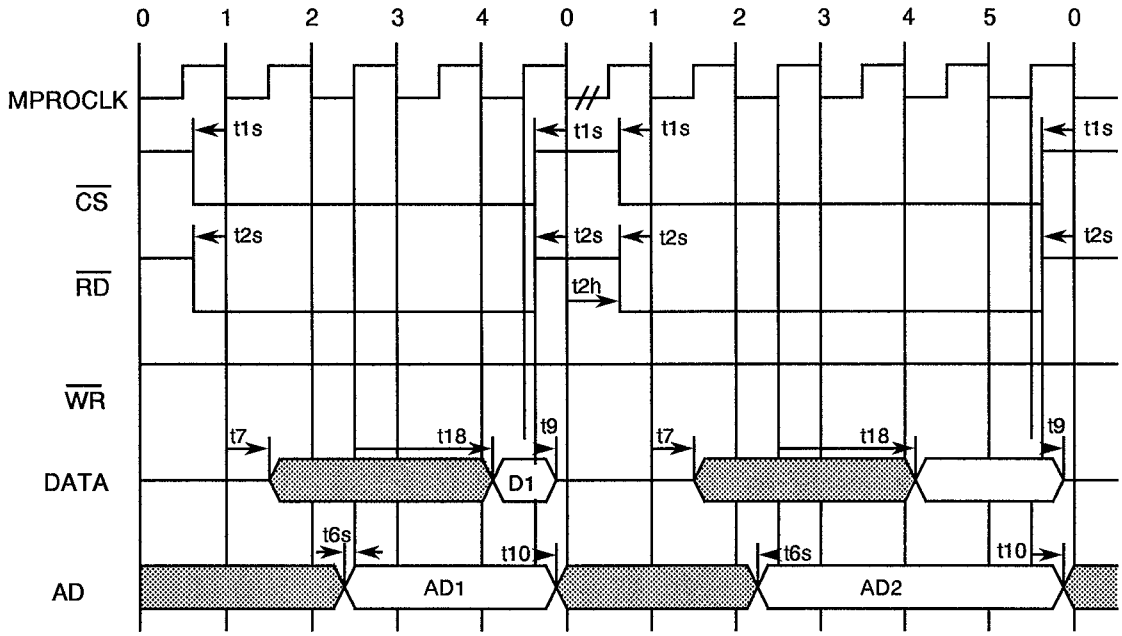
TIMING DIAGRAMS



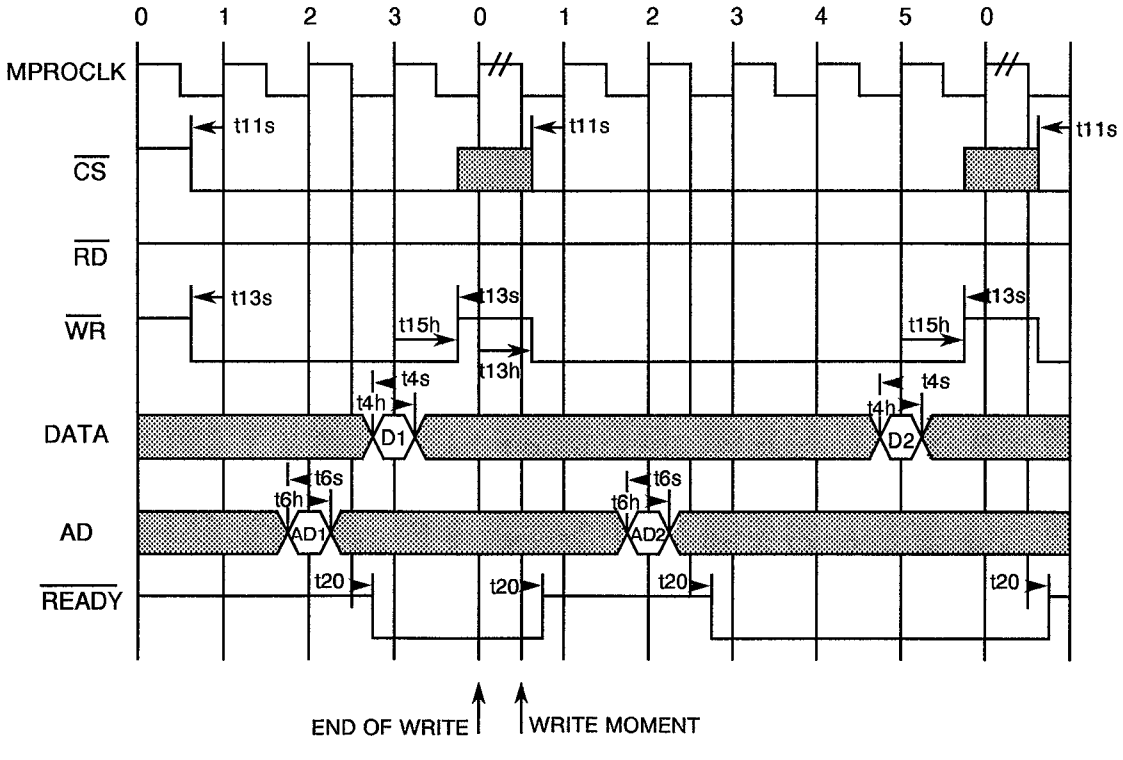
ERC-32 Write Cycle

FIGURE 3(b) - TRUTH TABLE (CONTINUED)

TIMING DIAGRAMS (CONTINUED)



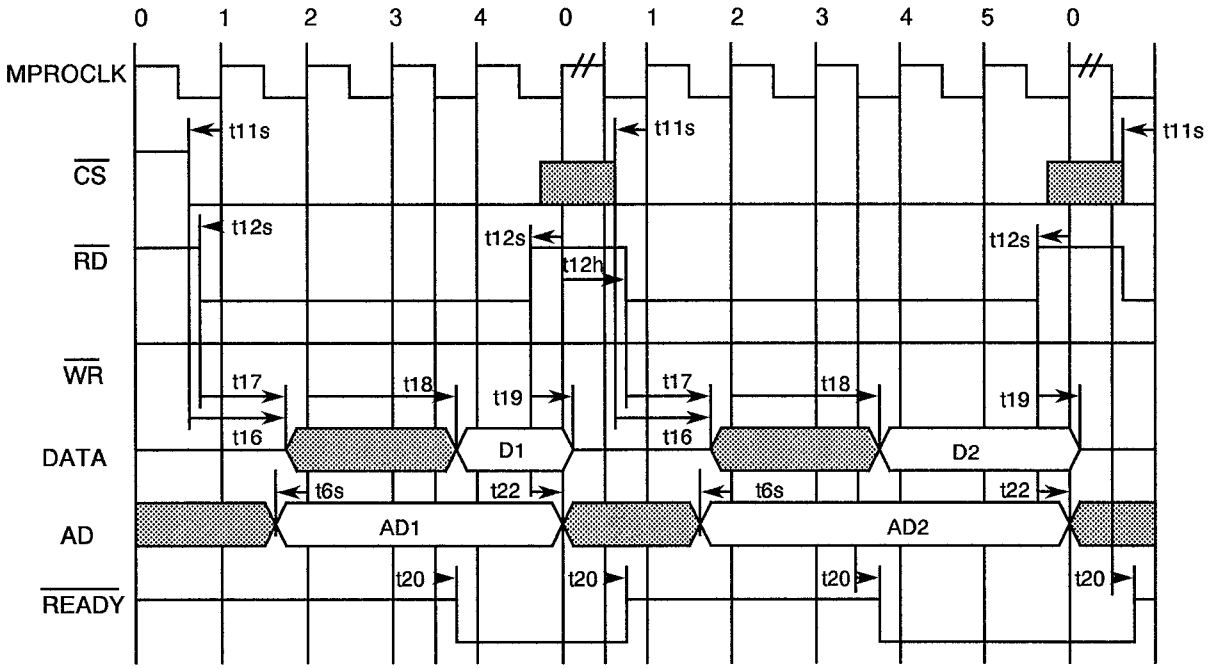
ERC-32 Read Cycle



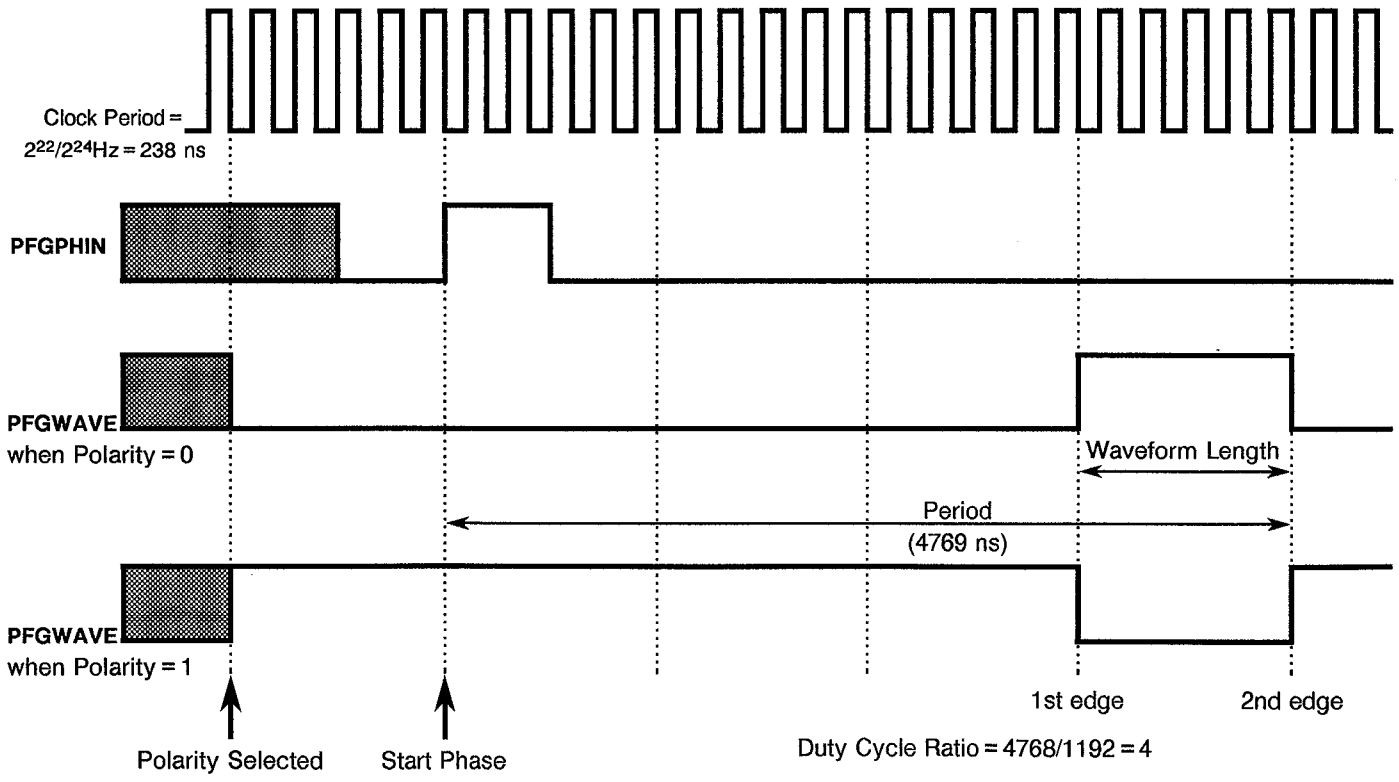
MA31750 Write Cycle

FIGURE 3(b) - TRUTH TABLE (CONTINUED)

TIMING DIAGRAMS (CONTINUED)



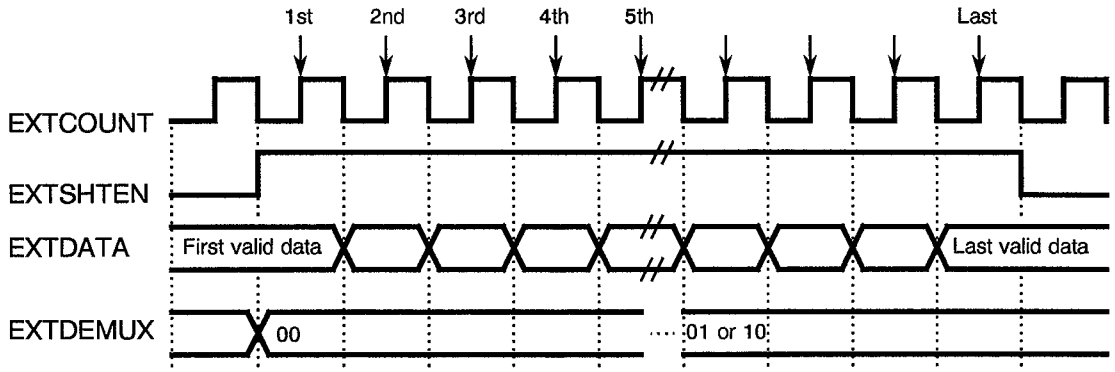
MA31750 Read Cycle



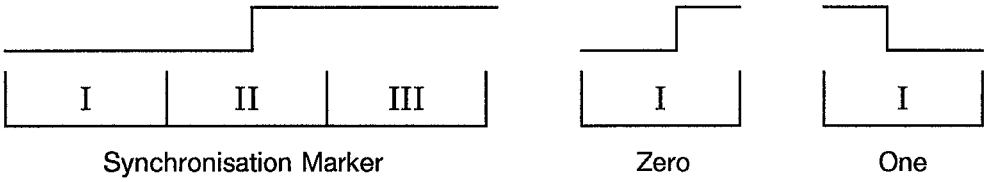
Waveform Generator Parameters for the Case ET Counter = 2^{22}Hz

FIGURE 3(b) - TRUTH TABLE (CONTINUED)

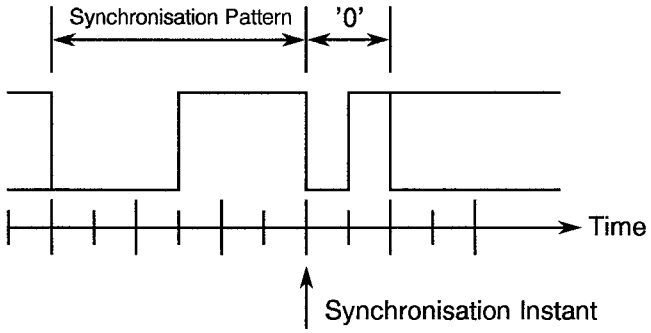
TIMING DIAGRAMS (CONTINUED)



Parallel/Stand-Alone Operation Extension Interface Protocol



Manchester Code



Synchronisation Instant

LTMS Operation Mode and Clock Selection

Mode		Ctmsg	Ser	Auxtal	Clkf[2:0]	Phase Reference	LTMS Frequency	ET Resolution
SERIAL	SERAUX OBDH/TIME BUS +16MHz CLOCK	1	1	1	x11 x10 x01 x00	$2^{22}/32$ Hz $2^{21}/32$ Hz $2^{20}/32$ Hz $2^{19}/32$ Hz	2^{24} Hz 2^{24} Hz 2^{24} Hz 2^{24} Hz	2^{-22} 2^{-22} 2^{-22} 2^{-22}
	SERBUS OBDH BUS + BUS CLOCK	1	1	0	x11 x10 x01 x00	2^{22} Hz 2^{21} Hz 2^{20} Hz 2^{19} Hz	2^{22} Hz 2^{21} Hz 2^{20} Hz 2^{19} Hz	2^{-22} 2^{-21} 2^{-20} 2^{-19}

Serial Mode

FIGURE 3(b) - TRUTH TABLE (CONTINUED)

Mode		Ctmsg	Ser	Auxtal	Clkf[2:0]	Phase Reference	LTMS Frequency	ET Resolution
Parallel	PARAUX	1	0	1	011	2^{22} Hz	2^{24} Hz	2^{-22}
					010	2^{21} Hz	2^{24} Hz	2^{-22}
					001	2^{20} Hz	2^{24} Hz	2^{-22}
					000	2^{19} Hz	2^{24} Hz	2^{-22}
					111	2^{22} Hz/1024	2^{22} Hz	2^{-22}
					110	2^{21} Hz/1024	2^{21} Hz	2^{-21}
					101	2^{20} Hz/1024	2^{20} Hz	2^{-20}
					100	2^{19} Hz/1024	2^{19} Hz	2^{-19}
	PARBUS	1	0	0	x11	2^{22} Hz	2^{22} Hz	2^{-22}
					x10	2^{21} Hz	2^{21} Hz	2^{-21}
					x01	2^{20} Hz	2^{20} Hz	2^{-20}
					x00	2^{19} Hz	2^{19} Hz	2^{-19}

Parallel Operation

Mode		Ctmsg	Ser	Auxtal	Clkf[2:0]	Phase Reference	LTMS Frequency	ET Resolution
Stand Alone	SALAUX	0	X	1	x11	2^{22} Hz	2^{24} Hz	2^{-22}
					x10	2^{21} Hz	2^{24} Hz	2^{-22}
					x01	2^{20} Hz	2^{24} Hz	2^{-22}
					x00	2^{19} Hz	2^{24} Hz	2^{-22}
	SALBUS	0	X	0	x11	2^{22} Hz	2^{22} Hz	2^{-22}
					x10	2^{21} Hz	2^{21} Hz	2^{-21}
					x01	2^{20} Hz	2^{20} Hz	2^{-20}
					x00	2^{19} Hz	2^{19} Hz	2^{-19}

Stand Alone Operation

FIGURE 3(b) - TRUTH TABLE (CONTINUED)

Etthr[1:0]	ET Resolution	Monotonous ET Counter LSB Position	Typical (Time)	ET Counter Clock Periods
00	2^{-22}	2^{-20}	±1.0µs	±4.0
01	2^{-22}	2^{-16}	±15.2µs	±64
10	2^{-22}	2^{-12}	±244µs	±1024
11	2^{-22}	2^{-8}	±3.9ms	±16384
00	2^{-21}	2^{-19}	±1.9µs	±4.0
01	2^{-21}	2^{-15}	±30.5µs	±64
10	2^{-21}	2^{-11}	±488µs	±1024
11	2^{-21}	2^{-7}	±7.8ms	±16384
00	2^{-20}	2^{-18}	±3.8µs	±4.0
01	2^{-20}	2^{-14}	±61µs	±64
10	2^{-20}	2^{-10}	±0.97ms	±1024
11	2^{-20}	2^{-6}	±15.6ms	±16384
00	2^{-19}	2^{-17}	±7.6µs	±4.0
01	2^{-19}	2^{-13}	±122µs	±64
10	2^{-19}	2^{-9}	±1.95ms	±1024
11	2^{-19}	2^{-5}	±31.2ms	±16384

ET Threshold Values

FIGURE 3(b) - TRUTH TABLE (CONTINUED)

LTMS REGISTER ADDRESSES

WORD	ADDRESS	READ	WRITE
Not Used	0	R (1)	-
CTMS Message Register (2)			
CTMS Status Field	1	R	W in Parallel and Stand-Alone operation only
Coarse Time Field MSW	2	R	W in Parallel and Stand-Alone operation only
Coarse Time Field LSW	3	R	W in Parallel and Stand-Alone operation only
Pulse Field MSW	4	R	W in Parallel and Stand-Alone operation only
Pulse Field LSW	5	R	W in Parallel and Stand-Alone operation only
Waveform Coarse Length Field	6	R	W in Parallel and Stand-Alone operation only
Waveform Fine Length Field MSW	7	R	W in Parallel and Stand-Alone operation only
Waveform Fine Length Field LSW	8	R	W in Parallel and Stand-Alone operation only
Polarity and Duty Cycle Ratio Field	9	R	W in Parallel and Stand-Alone operation only
Status Registers			
LTMS Status Register	10	R	-
CTMS Status Register	11	R	-
Alarm Register			
Alarm - ET Coarse MSW	12	R	W
Alarm - ET Coarse LSW	13	R	W
Alarm - ET Fine MSW	14	R	W
Alarm - ET Fine LSW	15	R	W
Time-Stamp			
Time-Stamp - LTMS Status	16	R	-
Time-Stamp - ET Coarse MSW	17	R	-
Time-Stamp - ET Coarse LSW	18	R	-
Time-Stamp - ET Fine MSW	19	R	-
Time-Stamp - ET Fine LSBs and CTMS Status 8 MSBs	20	R	-
Stop-Watch			
SW - Coarse Time	21	R	W - SWCountEvents selected by write
SW - Fine MSW	22	R	W - SWCountEvents selected by write
SW - Fine LSB	23	R	W - SWCountEvents selected by write
SW - Events MSW	24	R	W - SWMeasureTime selected by write
SW - Events	25	R	W - SWMeasureTime selected by write
SW - Events LSW	26	R	W - SWMeasureTime selected by write
Control Register (3)	27	R	Only bits 2, 3, 5, 6, 7 and 8 are writeable
Waveform Generator (4)			
Waveform Coarse Length	28	R	W
Waveform Fine Length MSW	29	R	W
Waveform Fine Length LSW	30	R	W
Polarity and Duty Cycle Ratio	31	R	W

NOTES

1. When this unused address is read, the data on the 16 bit data bus is all zeros.
2. Read-back of a CTMS Message is only possible after the end of the message transfer is detected by the LTMS.
3. For the Control Register, Read operations are done on an internal copy of the register. Write operations write into the register itself.
4. Only internally used when PFGMODE = 1. If PFGMODE = 0, these address locations can be used as storage registers.

FIGURE 3(b) - TRUTH TABLE (CONTINUED)

ERROR CODES (BITS 4-3 IN LTMS STATUS REGISTER)

CODE	NAME	DESCRIPTION
00	No Error	LTMS Synchronisation has been performed. No Message Error or Synchronisation Error or Synchronisation Warning was detected.
01	Message Error	A Message Error or a Synchronisation Time-Out has been detected. No LTMS Synchronisation has been or will be performed using the erroneous message.
10	Synchronisation Error	In Serial and Parallel operations, a valid CTMS Message has been received, but a Synchronisation Error occurred. The LTMS Sychronisation has not been performed. In Stand-Alone operation, a valid CTMS Message has been received but a Synchronisation Error or Warning was detected. In the case of a Synchronisation Error, no LTMS Synchronisation occurred. In the case of a Synchronisation Warning, the LTMS Synchronisation has been performed but this error code warns that a time discontinuity may have occurred.
11	Mode/Go Synchronisation	A valid CTMS Message has been received. At the moment an LTMS Synchronisation occurred, the Synchronisation Instant that resulted in the LTMS Synchronisation did not occur inside the ET Threshold window or the ET Coarse of the CTMS Message was not equal to the ET Coarse of the ET Counter + 1.0 second. However, Initialisation Flag was set or, in Serial and Parallel operations only, the Go Threshold was reached while LTMS Status EXTERROR flag was 0. This code warns that a time discontinuity occurred.

CTMS STATUS REGISTER

BIT	NAME	DESCRIPTION
15	Toggle	Bit 15 is toggled each time new CTMS Status information is loaded in the CTMS Status Register, i.e. each time a Synchronisation Pulse follows a valid CTMS Message. This bit is also available in the Time-Stamp Facility after a time-stamp has been performed.
14	Pulse Flag	Pulse Flag of the last valid CTMS Message preceding the latest Synchronisation Instant. This bit is also available in the Time-Stamp Facility after a time-stamp has been performed.
13	Waveform Flag	Waveform Flag of the last valid CTMS Message preceding the latest Synchronisation Instant. This bit is also available in the Time-Stamp Facility after a time-stamp has been performed.
12	Initialisation Flag	Initialisation Flag of the last valid CTMS Message preceding the latest Synchronisation Instant. This bit is also available in the Time-Stamp Facility after a time-stamp has been performed.
11 - 8	Time Chain Flags	Time Chain Flags of the last valid CTMS Message preceding the latest Synchronisation Instant. These bits are also available in the Time-Stamp Facility after a time-stamp has been performed.
7 - 0	Mission Specific Flags	Mission Specific Flags of the last valid CTMS Message preceding the latest Synchronisation Instant. These bits are also available in the Time - Stamp Facility after a time-stamp has been performed.

FIGURE 3(b) - TRUTH TABLE (CONTINUED)

LTMS CONTROL REGISTER

BIT	NAME	MODE	CONTROL	DESCRIPTION
15-10	Not used	R	LTMS	Zero values are provided during a Read cycle.
09	TVLDbit	R	LTMS	The TVLDbit flag is a copy of the TVLD output.
08	SWSTART bit	R/W	LTMS and User	This flag allows control of the Stop-Watch facility operations from the Control Register when SWSELbit = 1. In this case, the SW can be started or continued with SWSTARTbit = 1. It is halted using SWSTART = 0. When SWSELbit = 0, the Stop-Watch operations are under control of the SWSTART input. Reading SWSTARTbit can be used to monitor SWSTART.
07	SWSELbit	R/W	LTMS and User	The SWSELbit flag allows to select if the Stop-Watch facility operations (i.e. start/continue or hold/stop the measurement) are controlled via SWSTART input (if SWSELbit = 0) or via the SWSTARTbit flag (if SWSELbit = 1). User requests for updating the SWSELbit flag (and changing the SW control mode) are only accepted if, at the same time, the SWSTARTbit flag is specified = 0. If SWSTARTbit = 1, the SWSELbit remains unchanged.
06	SWEVENT bit	R/W	User	A 0 to 1 transition on the SWEVENTbit flag is equivalent to generating a pulse on the SWEVENT input. Pulses generated on the SWEVENT input are not reflected onto the SWEVENTbit flag.
05	EXTERINbit	R/W	User	The EXTERINbit flag is fully under the control of the User. EXTERINbit = 1 can, for example, indicate that external checks on the current CTMS Message have detected errors. Asserting the EXTERINbit flag has the same effect as raising the EXTERIN input but both operate independently. Either one being high impedes synchronisation.
04	PFGWAVE bit	R	LTMS	The PFGWAVEbit flag is a copy of the PFGWAVE output.
03	PFGPHIN bit	R/W	User	The PFGPHINbit flag is set when: - A 1 is written on this bit position. - A rising edge is detected on the PFGPHIN input. Assuming that the PFGPHINbit flag is initially = 0, raising the flag has the same effect as raising the PFGPHIN input. When the PFGPHINbit flag is high, there is a difference. In particular, the next rising edges detected on the PFGPHIN input are not disabled: the related phase information is passed to the Waveform Generator facility whatever the value of the PFGPHINbit flag is. The PFGPHINbit flag hence has not to be reset at each rising edge of the PFGPHIN input in the case that the Waveform Generator facility is controlled by the PFGPHIN input. On the other hand, attempting to assert the PFGPHINbit flag while it is already 1 does not generate further phase signals to the Waveform Generator facility. The PFGPHINbit flag has to be reset first.
02	ETSTRBbit	R/W	User	The ETSTRBbit flag is set when: - A 1 is written on this bit position. - A rising edge is detected on ETSTRB input. Asserting ETSTRBbit has the same effect as raising the ETSTRB input. The ETSTRBbit flag is cleared by the LTMS at the end of a read access of the Time-Stamp facility with the highest address (i.e. when the Time-Stamp facility is ready for a new Time-Stamp cycle).
01	ETALRMbit	R	LTMS	The ETALRMbit flag is a copy of the ETALRM output.
00	WINDOW bit	R	LTMS	The WINDOWbit flag is a copy of the WINDOW output.

FIGURE 3(b) - TRUTH TABLE (CONTINUED)

LTMS STATUS REGISTER

BIT	NAME	DESCRIPTION
15	Stop-Watch	This flag is set when the Stop-Watch facility has completed the requested measurement. i.e. when the Stop-Watch facility Time counter (if in SWCountEvents mode) or the SW Event counter (if in SWMeasureTime mode) reaches 0. The stop-watch flag is also set when the SW Event Counter (if in SWCountEvents mode) or the SW Time Counter (in SWMeasureTime mode) saturates. The flag is cleared when the User starts to write in the Stop-Watch facility.
14	Waven	This flag is set as soon as the waveform generation has started on the pfgwave output, i.e. the Waveform Generator facility is active. The waven flag is reset as soon as the Waveform Generator facility becomes stopped or is put on hold.
13	Phase	This flag concerns the LTMS Pulse Generator facility. The phase flag is updated at an LTMS Synchronisation instant (or the first wrap around instant of Fine Time of the Monotonous ET Counter following the last LTMS Synchronisation) following an LTMS Synchronisation that loaded a new message. In case the phase flag is updated at the wrap around instant, the phase flag value simply remains unchanged at the next LTMS Synchronisation (at $t > T+2$ sec). Assuming to be at $T+2$ sec while and LTMS Synchronisation occurred at $T+1$ sec, the phase flag is set to 1 if no pulse was generated on pfgphout between $T+1$ sec $= t < T+2$ sec while the CTMS Message transmitted between T and $T+1$ sec included a Pulse field. The phase flag is cleared at $T+2$ sec if no CTMS Message Pulse field was available (i.e. no pulse had to be generated between $T+1$ sec $= t < T+2$ sec) or if a pulse has been successfully generated between $T+1$ sec $= t < T+2$ sec.
12	Alarm	This flag is set after an external reset. In Serial and Parallel operation, it is cleared on the second LTMS Synchronisation. In Stand-Alone mode it is cleared the moment the writing of address 15 is detected. From the moment it is cleared on, the flag is set when a time already past is loaded in the Alarm Clock facility, in all operations. Writing an Alarm time greater than the current Elapsed Time in the ET Alarm Register de-asserts the alarm flag.
11	Time-Stamp	This flag is set when an event is detected on the etstrb input while the Time-Stamp facility is busy. It is cleared only when the next valid event is processed.
10	Synchto	This flag is set when a Synchronisation Pulse Time-out is detected in Serial and Parallel operations. It is cleared at the detection of the next Synchronisation Instant. In Stand-Alone operation, the synchto flag is always $=0$.
09	Etcto	This flag is set when the ET Threshold is exceeded at the moment an LTMS Synchronisation should be performed. The etcto flag is reset at a following LTMS Synchronisation where the Synchronisation Instant is inside the ET Threshold window.
08	Windout	In Parallel and Stand-Alone operations, this flag is set when a window violation is encountered while writing in the CTMS Message register. The windout flag is cleared as soon as address 1 of a new CTMS Message is written while the window output is one. Read access has no impact on the window flag in Parallel operation. In Serial operation, the windout flag is set as soon as one of the two window is encountered. The windout flag is reset the next time address 1 of the CTMS Meaasge is read while window is set.
07	Exterror	The exterror flag becomes 1 when the exterin input and/or Control Register exterinbit flag are set. exterror $=1$ can, for example, mean that an external check has detected an error in the CTMS Message. No LTMS Synchronisation is performed as long as the exterror flag is set. However, the assertion of the exterror flag does not disable the acquisition of new valid CTMS Messages. The exterror flag is cleared when both the exterin input and the Control Register exterinbit flag become/are low.
06	Wasfree	This flag is set when the DPLL has been free-wheeling at least once since the last LTMS Synchronisation. When this flag is set, the local time reference has probably drifted. The wasfree flag is reset on the next LTMS Synchronisation.
05	Free	This flag 1 when the DPLL is free-wheeling. It is 0 as soon as the DPLL is locked again.
04-03	Errcode[1:0]	These flags hold information about what the LTMS has done with the last CTMS Message it received.
02-00	Errcount[2:0]	This is the Error Counter. It is used to record the build-up of Message and Synchronisation Errors detected in previous CTMS Messages.

FIGURE 3(c) - CIRCUIT DESCRIPTION

The LTMS (Local Time Management System) is the key element of a decentralised time distribution scheme. Local copies of the centralised Elapsed Time (ET) reference of a spacecraft are maintained by LTMS devices located close to the Users. The central ET reference is assumed to be managed by a Central Time Management System (CTMS). The coherence between the local ET references and the central ET reference is maintained by means of time synchronisation messages distributed by the CTMS. The LTMS performs regular synchronisations with respect to the central ET reference using such messages and provides its Users with several time facilities related to the local ET reference, a Time-Stamp, an Alarm Clock, a Pulse Generator, a Waveform Generator and a Stop-Watch.

MAIN FEATURES

- Compliance with the CCSDS-CUC Elapsed Time code standard format.
- Compliance with the Serial Time Distribution Protocol Extensions of the 4-255 Data Bus.
- Elapsed Time resolution from 2^{-19} down to 2^{-22} of a second.
- Serial and parallel time synchronisation message reception, or Standalone operation.
- Parallel microprocessor interface directly compatible with the ERC32 and MA31750 microprocessors.
- Time-Stamp facility.
- Alarm Clock facility.
- Pulse Generator facility.
- Waveform Generator facility that can be combined with the Pulse Generator to form a Programmable Frequency Generator.
- Stop-Watch facility counting the number of events within a specified time interval or the time between a specified number of events.
- Extension Interface for implementation of additional User facilities and error checkers.
- External oscillator interface driving an internal or external DPLL, to achieve high resolution and free-wheeling capability.
- Error detection, management and recovery capabilities.

SYSTEM OVERVIEW

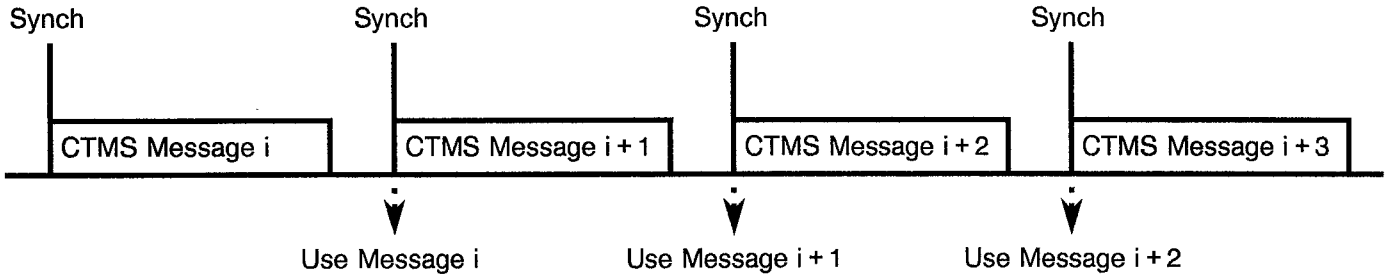
The Central Time Management System (CTMS) manages a central ET reference. The LTMS maintains a local copy of the system Elapsed Time (ET) reference, complaint to the CCSDS-CUC ET format. In order to keep the (same) local time reference available to all the Users embedding an LTMS, four kinds of information are presented to the LTMS.

- Once every second, a CTMS Message including a time code is broadcast from the CTMS to all the LTMS components in the system. These messages can be acquired through a serial or a parallel microprocessor interface. The serial message is Manchester encoded. The Manchester encoding is either self-synchronised or synchronised to the bus clock.

- Each CTMS Message is followed by a Synchronisation Instant indicating when the time code in that CTMS Message becomes valid. This Synchronisation Instant occurs at 1 second intervals and indicates an integer amount of seconds. It is provided by the CTMS.

FIGURE 3(c) - CIRCUIT DESCRIPTION (CONTINUED)

CTMS MESSAGE USAGE



- The LTMS receives Phase References from the CTMS to which the clock driving the local counter can be phase and frequency adjusted. These Phase References do not always have to occur at regular intervals.

- The LTMS also receives a clock to drive the LTMS ET Counter. This clock does not necessarily originate from the CTMS but may be a local clock.

The LTMS performs format checks on the incoming CTMS Messages (message checks). It also checks the correct placement of the Synchronisation Instant and the validity of the CTMS Message information for synchronisation purposes (synchronisation checks).

If there were no Message Errors in the CTMS Message and no Synchronisation Errors occured, an LTMS Synchronisation is performed on the detection of the Synchronisation Instant. The LTMS Synchronisation consists of pre-setting the local ET Counter to an integer amount of ET seconds distribution chain in the dedicated facility registers.

By setting a flag, called the Initialisation Flag, in the CTMS Message, it is possible to disable the Synchronisation Checks and force a CTMS Message to be used for LTMS synchronisation.

The LTMS User is permanently informed about the time validity by a dedicated output. For more details, the User has access to a status register via the parallel microprocessor interface. The LTMS also has a status register dedicated to the status of the rest of the time-distribution chain.

If the Phase References occur at regular intervals but at too low a rate with regards to the required time resolution, or if they occur irregularly, or if free-wheeling capability is required in case of Phase Reference transmission failure, the LTMS makes use of a Digital Phase Locked Loop (DPLL). It can use either its internal LTMS DPLL, or an external one. The DPLL provides an internal 2^{22}Hz clock, phase-adjusted to the incoming Phase References, that drives the ET Counter. This internal 2^{22}Hz clock is derived from an external 2^{24}Hz clock. This can be either an existing clock signal or a crystal oscillator.

Phase-adjustment is done by modifying the internal 2^{22}Hz clock period by adding or subtracting a 2^{24}Hz period to lock on to the Phase References.

If the DPLL cannot lock onto the incoming Phase References is starts free-wheeling. It then generates a 2^{22}Hz clock that is merely a division of the external 2^{24}Hz clock without performing any phase corrections. Meanwhile the DPLL tries to lock onto the incoming Phase References again.

FIGURE 3(c) - CIRCUIT DESCRIPTION (CONTINUED)

The LTMS supports several time facilities, accessible via the parallel microprocessor interface and dedicated control pins. The time facilities can be controlled and observed via dedicated inputs and outputs as well as via a Control Register.

The Time-Stamp Facility allows the LTMS User to time-tag data. An external event is used to store the current ET Counter value plus the status of the LTMS and of the rest of the time-chain.

The Alarm Clock Facility allows the LTMS User to generate an alarm to start an action at a pre-defined instant.

The Stop-Watch Facility allows the LTMS User to measure time intervals or the number of events within a pre-defined time interval.

The Pulse Generator Facility allows the CTMS to generate pulses at a maximum 1Hz rate.

The Waveform Generator Facility allows the LTMS User or the CTMS to generate a periodic waveform. The waveform frequency and shape are programmable via the parallel microprocessor interface or the CTMS Message respectively.

The Pulse-and Waveform Generator facilities can be combined to form a Programmable Frequency Generator that generates a periodic waveform, controlled in phase as well.

The LTMS Extension Interface allows the LTMS User to increase or customise the time facilities with a minimum of external hardware.

The LTMS can also be used in stand-alone operation. The LTMS maintains its own time reference in this case and no regular synchronisation is required. It is however possible to initialise the LTMS from time-to-time via the parallel microprocessor interface. This provides the capability to use the LTMS and its time facilities even if no central ET reference is available. The time-out checks are disabled because the time messages are now optional. The LTMS Synchronisation corresponds to an initialisation in this case.

Elapsed Time Format

All time information sent to and provided by the LTMS is compliant to the CCSDS-CUC format. The P-field of each CTMS Message time information is constant for the LTMS application. Consequently, it does not need to be transmitted. The T-field of the CTMS Message time information comprises 4 coarse time octets (bits with weights 2^0 to 2^{31}).

CCSDS-CUC ET Format

P-Field octet (7:0)	T-Field octets			
00110100				
2^{32}	2^{24}	2^{16}	2^8	2^0

FIGURE 3(c) - CIRCUIT DESCRIPTION (CONTINUED)

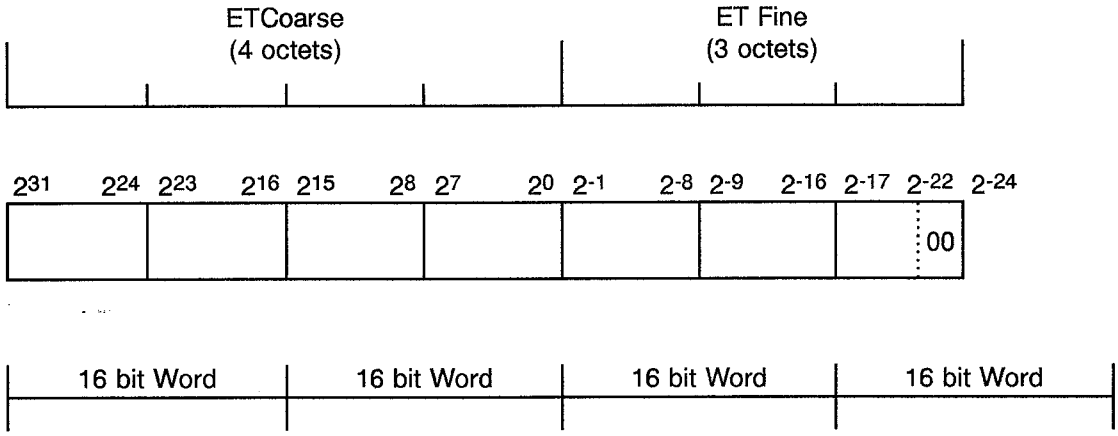
The LTMS ET Counter is the local time reference consisting of the ET Fine counter (22 bits with a weight < 1 second) and the ET Coarse counter (32 bits with a weight ≥ 1 second, leading to a wrap-around period of 136 years).

The LTMS ET Counter resolution depends on the operation selection. As a result of this, the ET Counter least significant bit can have weights 2^{-22}, 2^{-21}, 2^{-20} or 2^{-19}.

The position within an octet of a bit with a defined weight is constant and independent of the LTMS operation.

The LTMS Stop-Watch facility resolution depends on the operation selection. The bit weights for the least significant bit of the Stop-Watch facility can be 2^{-24}, 2^{-22}, 2^{-21}, 2^{-20} or 2^{-19}. Its most significant bit has the weight 2^{31}.

LTMS ET Format



Some of the LTMS registers have bits that are not used. When one of those registers is read, zero values are read for those bits. This is, for example, the case for bits with weight smaller than the selected resolution in the ET Counter or the Stop-Watch facility.

FIGURE 3(d) - FUNCTIONAL DIAGRAM

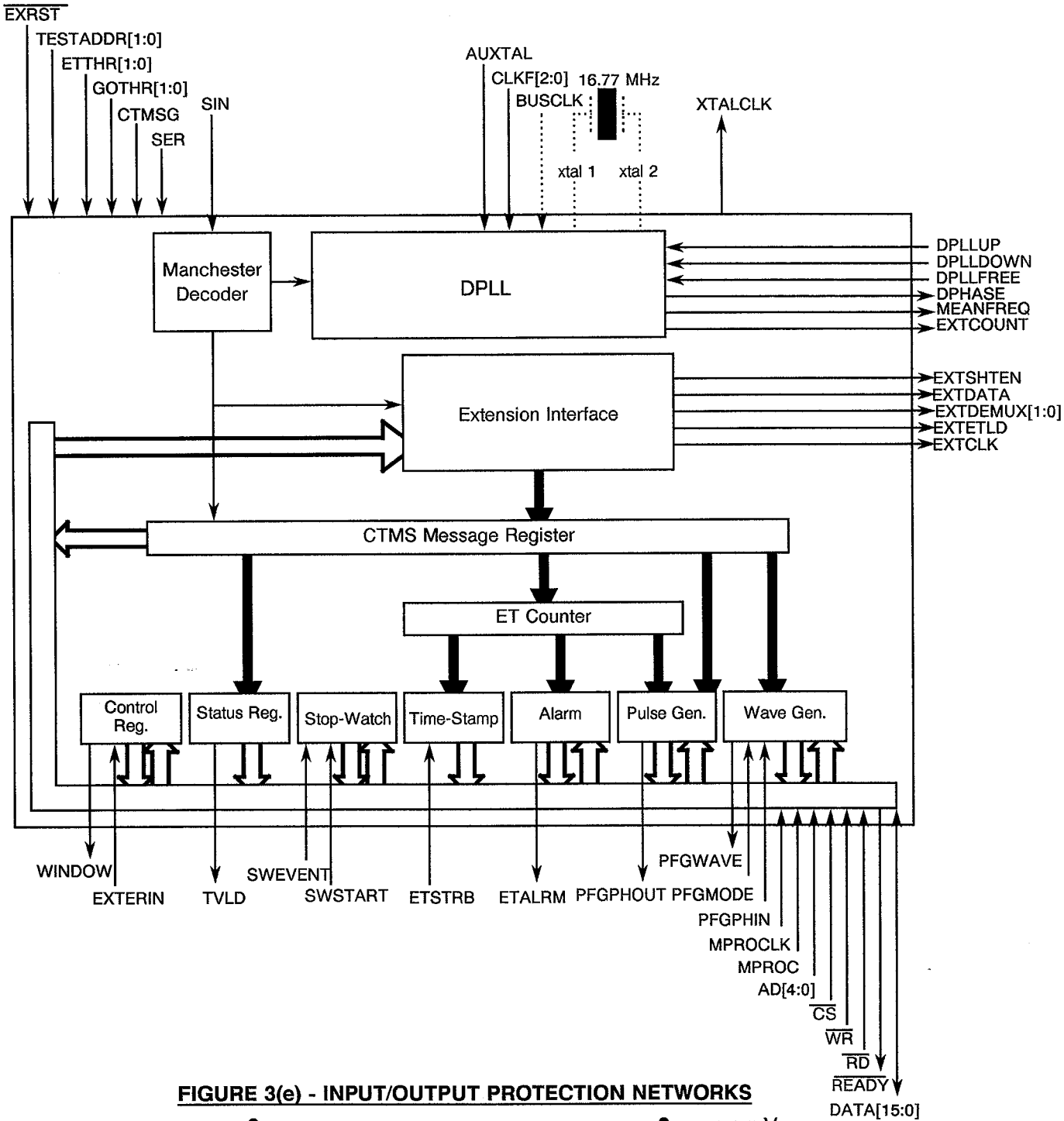
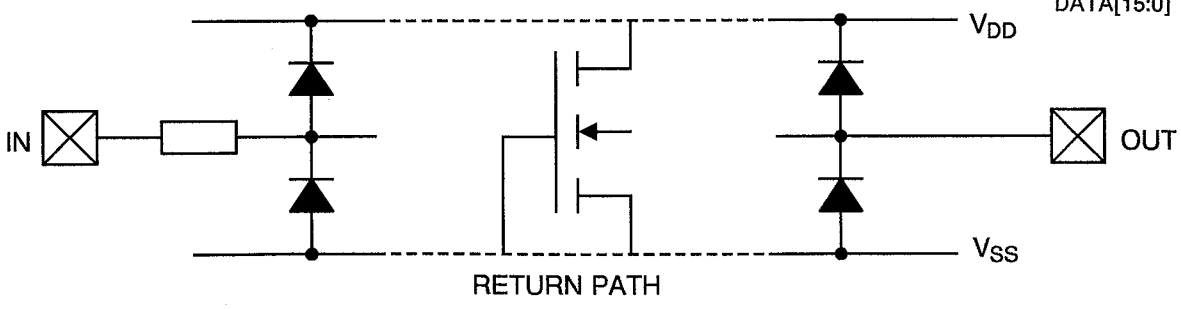


FIGURE 3(e) - INPUT/OUTPUT PROTECTION NETWORKS



2. APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:-

(a) ESA/SCC Generic Specification No. 9000 for Integrated Circuits.

(b) MIL-STD-883, Test Methods and Procedures for Micro-electronics.

(c) ESA PSS-04-106, Packet Telemetry Standard.

(d) ESA PSS-04-107, Packet Telecommand Standard.

3. TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESA/SCC Basic Specification No. 21300 shall apply. In addition, the following abbreviation is used:-

V_{IC} - Input/Output Clamp Voltage.

4. REQUIREMENTS

4.1 GENERAL

The complete requirements for procurement of the integrated circuits specified herein are stated in this specification and ESA/SCC Generic Specification No. 9000 for Integrated Circuits. Deviations from the Generic Specification, applicable to this specification only, are listed in Para. 4.2.

Deviations from the applicable Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESA/SCC requirements and do not affect the components' reliability, are listed in the appendices attached to this specification.

4.2 DEVIATIONS FROM GENERIC SPECIFICATION

4.2.1 Deviations from Special In-process Controls

(a) Para. 5.2.2, Total Dose Irradiation Testing: Shall be performed during qualification and maintenance of qualification.

(b) Para. 5.2.2, Total Dose Irradiation Testing: Shall be performed during procurement on a lot acceptance basis at the total dose irradiation level specified in the Purchase Order.

4.2.2 Deviations from Final Production Tests (Chart II)

None.

4.2.3 Deviations from Burn-in and Electrical Measurements (Chart III)

(a) Para. 7.1.1(a), "High Temperature Reverse Bias" test and subsequent electrical measurements related to this test shall be omitted.

4.2.4 Deviations from Qualification Tests (Chart IV)

None.

4.2.5 Deviations from Lot Acceptance Tests (Chart V)

None.

4.3 MECHANICAL REQUIREMENTS

4.3.1 Dimension Check

The dimensions of the integrated circuits specified herein shall be checked. They shall conform to those shown in Figure 2.

4.3.2 Weight

The maximum weight of the integrated circuits specified herein shall be 5.0 grammes.

4.3.3 Terminal Strength

The requirements for terminal strength testing are specified in Section 9 of ESA/SCC Basic Specification No. 9000. The test conditions shall be as follows:-

Applied Force: 1.0 ± 0.1 Newtons, 3 bends at 45°.

4.4 MATERIALS AND FINISHES

The materials and finishes shall be as specified herein. Where a definite material is not specified, a material which will enable the integrated circuits specified herein to meet the performance requirements of this specification shall be used. Acceptance or approval of any constituent material does not guarantee acceptance of the finished product.

4.4.1 Case

The case shall be hermetically sealed and have a ceramic body and the lids shall be pre-form soldered.

4.4.2 Lead Material and Finish

The material shall be Type 'D' with Type '2' finish in accordance with the requirements of ESA/SCC Basic Specification No. 23500. (See Table 1(a) for Type Variants).

4.5 MARKING

4.5.1 General

The marking of all components delivered to this specification shall be in accordance with with the requirements of ESA/SCC Basic Specification No. 21700 and the following paragraphs. When the component is too small to accommodate all of the marking specified, as much as space permits shall be marked and the marking information, in full, shall accompany the component in its primary package.

The information to be marked and the order of precedence, shall be as follows:-

(a) Lead Identification.

(b) The SCC Component Number.

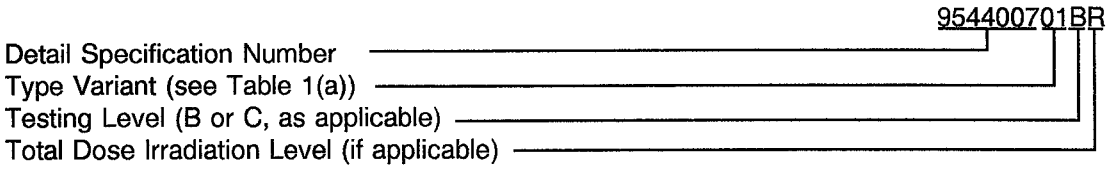
(c) Traceability Information.

4.5.2 Lead Identification

An index shall be located at the top of the package in the position defined in Note 1 to Figure 2 or, alternatively, a tab may be used to identify Pin No. 1. The pin numbering must be read with the index or tab on the left-hand side.

4.5.3 The SCC Component Number

Each component shall bear the SCC Component Number which shall be constituted and marked as follows:



The Total Dose Irradiation Level designation shall be added for those devices for which a sample has been successfully tested to the level in question. For these devices, a code shall be added in accordance with the requirements of ESA/SCC Basic Specification No. 22900.

4.5.4 Traceability Information

Each component shall be marked in respect of traceability information in accordance with the requirements of ESA/SCC Basic Specification No. 21700.

4.6 ELECTRICAL MEASUREMENTS

4.6.1 Electrical Measurements at Room Temperature

The parameters to be measured in respect of electrical characteristics are scheduled in Table 2. Unless otherwise specified, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.6.2 Electrical Measurements at High and Low Temperatures

The parameters to be measured at high and low temperatures are scheduled in Table 3. The measurements shall be performed at $T_{amb} = +125(+0-5)$ °C and $-55(+5-0)$ °C respectively.

4.6.3 Circuits for Electrical Measurements

Circuits for use in performing electrical measurements listed in Tables 2 and 3 of this specification are shown in Figure 4.

4.7 BURN-IN TESTS

4.7.1 Parameter Drift Values

The parameter drift values applicable to burn-in are specified in Table 4 of this specification. Unless otherwise stated, measurements shall be performed at $T_{amb} = +22 \pm 3$ °C. The parameter drift values (Δ) applicable to the parameters scheduled, shall not be exceeded. In addition to these drift value requirements, the appropriate limit value specified for a given parameter in Table 2 shall not be exceeded.

4.7.2 Conditions for High Temperature Reverse Bias Burn-in (Table 5(a))

Not applicable.

4.7.3 Conditions for Power Burn-in

The requirements for power burn-in are specified in Section 7 of ESA/SCC Generic Specification No. 9000. The conditions for power burn-in shall be as specified in Table 5(b) of this specification.

4.7.4 Electrical Circuits for High Temperature Reverse Bias Burn-in (Figure 5(a))

Not applicable.

4.7.5 Electrical Circuits for Power Burn-in

A circuit for use in performing the power burn-in test is shown in Figure 5(b) of this specification.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS

No.	CHARACTERISTICS	SYMBOL	MIL-STD 883 TEST METHOD	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
1	Functional Test 1 (Basic)	-	3014	-	Verify Device Operation with Load V_{IL} = 0V, V_{IH} = 5.0V V_{OL} = 1.0V, V_{OH} = 4.0V I_{OUT} = ± 2.0mA C_L = 100pF ± 20% V_{DD} = 5.0V, V_{SS} = 0V Pattern = Note 1	-	-	-
2	Functional Test 2 (Nominal Voltage)	-	3014	-	Verify Device Operation with Load V_{IL} = 0.5V, V_{IH} = 4.5V V_{OL} = 1.0V, V_{OH} = 4.0V I_{OUT} = ± 2.0mA C_L = 100pF ± 20% V_{DD} = 5.0V, V_{SS} = 0V Pattern = Note 1	-	-	-
3	Functional Test 3 (High Voltage)	-	3014	-	Verify Device Operation with Load V_{IL} = 0.5V, V_{IH} = 5.0V V_{OL} = 1.0V, V_{OH} = 4.5V I_{OUT} = ± 2.0mA C_L = 100pF ± 20% V_{DD} = 5.5V, V_{SS} = 0V Pattern = Note 1	-	-	-
4	Functional Test 4 (Low Voltage)	-	3014	-	Verify Device Operation with Load V_{IL} = 0.5V, V_{IH} = 4.0V V_{OL} = 1.0V, V_{OH} = 3.5V I_{OUT} = ± 2.0mA C_L = 100pF ± 20% V_{DD} = 4.5V, V_{SS} = 0V Pattern = Note 1	-	-	-
5	Quiescent Current	I_{DD}	3005	4(a)	V_{IL} = 0V, V_{IH} = 5.5V V_{DD} = 5.5V, V_{SS} = 0V All Outputs Open Note 2 (Pins 1 + 19 + 25 + 61 + 67 + 79)	-	500	µA
6 to 41	Input Current Low Level	I_{IL}	3009	4(b)	V_{IN} (Under Test) = 0V V_{IN} (Remaining Inputs) = 5.5V V_{DD} = 5.5V, V_{SS} = 0V (Pins 28-29-30-31-32-33-34-35-36-37-38-39-40-41-42-43-44-45-46-47-48-49-50-51-52-53-54-55-56-70-71-72-73-74-75)	-	− 2.0	µA

NOTES: See Page 32.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	MIL-STD 883 TEST METHOD	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
42 to 77	Input Current High Level	I_{IH}	3009	4(c)	V_{IN} (Under Test) = 5.5V V_{IN} (Remaining Inputs) = 0V V_{DD} = 5.5V, V_{SS} = 0V (Pins 28-29-30-31-32-33-34-35-36-37-38-39-40-41-42-43-44-45-46-47-48-49-50-51-52-53-54-55-56-70-71-72-73-74-75)	2.0	-	µA
78 to 110	Output Voltage Low Level 1	V_{OL1}	3007	4(d)	V_{IL} = 0.5V, V_{IH} = 4.0V I_{OL} = 4.0mA V_{DD} = 4.5V, V_{SS} = 0V Note 9 (Pins 2-3-4-5-8-9-10-11-14-15-16-17-20-21-22-23-26-27-57-58-59-62-63-64-65-68-69-77-80-81-82-83)	-	0.4	V
111	Output Voltage Low Level 2	V_{OL2}	3007	4(d)	V_{IL} = 0.5V, V_{IH} = 4.0V I_{OL} = 0.5mA V_{DD} = 4.5V, V_{SS} = 0V Note 3 (Pin 76)	-	0.4	V
112 to 144	Output Voltage High Level 1	V_{OH1}	3006	4(e)	V_{IL} = 0.5V, V_{IH} = 4.0V I_{OL} = −4.0mA V_{DD} = 4.5V, V_{SS} = 0V Note 3 (Pins 2-3-4-5-8-9-10-11-14-15-16-17-20-21-22-23-26-27-57-58-59-62-63-64-65-68-69-77-80-81-82-83)	3.9	-	V
145 to 177	Output Voltage High Level 2	V_{OH2}	3006	4(e)	V_{IL} = 0.5V, V_{IH} = 4.0V I_{OL} = −0.5mA V_{DD} = 4.5V, V_{SS} = 0V Note 3 (Pins 2-3-4-5-8-9-10-11-14-15-16-17-20-21-22-23-26-27-57-58-59-62-63-64-65-68-69-77-80-81-82-83)	4.2	-	V
178	Output Voltage High Level 3	V_{OH3}	3006	4(e)	V_{IL} = 0.5V, V_{IH} = 4.0V I_{OL} = −0.5mA V_{DD} = 4.5V, V_{SS} = 0V Note 3 (Pin 76)	3.9	-	V
179 to 214	Threshold Voltage Low Level 1 (CMOS Inputs)	V_{THN1}	-	4(f)	V_{DD} = 4.5V, V_{SS} = 0V (Pins 28-29-30-31-32-33-34-35-36-37-38-39-40-41-42-43-44-45-46-47-48-49-50-51-52-53-54-55-56-70-71-72-73-74-75)	1.3	-	V

NOTES: See Page 32.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	MIL-STD 883 TEST METHOD	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
215 to 250	Threshold Voltage High Level 1 (CMOS Inputs)	V_{THP1}	-	4(f)	V_{DD} = 4.5V, V_{SS} = 0V (Pins 28-29-30-31-32-33-34-35-36-37-38-39-40-41-42-43-44-45-46-47-48-49-50-51-52-53-54-55-56-70-71-72-73-74-75)	-	3.2	V
251 to 286	Threshold Voltage Low Level 2 (CMOS Inputs)	V_{THN2}	-	4(f)	V_{DD} = 5.5V, V_{SS} = 0V (Pins 28-29-30-31-32-33-34-35-36-37-38-39-40-41-42-43-44-45-46-47-48-49-50-51-52-53-54-55-56-70-71-72-73-74-75)	1.7	-	V
287 to 322	Threshold Voltage High Level 2 (CMOS Inputs)	V_{THP2}	-	4(f)	V_{DD} = 5.5V, V_{SS} = 0V (Pins 28-29-30-31-32-33-34-35-36-37-38-39-40-41-42-43-44-45-46-47-48-49-50-51-52-53-54-55-56-70-71-72-73-74-75)	-	3.9	V
323 to 391	Input/Output Clamp Voltage (to V_{SS})	V_{IC1}	3022	4(g)	I_{IN} = −100µA V_{DD} = V_{SS} = 0V (Pins 2-3-4-5-8-9-10-11-14-15-16-17-20-21-22-23-26-27-28-29-30-31-32-33-34-35-36-37-38-39-40-41-42-43-44-45-46-47-48-49-50-51-52-53-54-55-56-57-58-59-62-63-64-65-68-69-70-71-72-73-74-75-76-77-80-81-82-83)	-	−2.0	V
392 to 460	Input/Output Clamp Voltage (to V_{DD})	V_{IC2}	3022	4(g)	I_{IN} = 100µA V_{DD} = V_{SS} = 0V (Pins 2-3-4-5-8-9-10-11-14-15-16-17-20-21-22-23-26-27-28-29-30-31-32-33-34-35-36-37-38-39-40-41-42-43-44-45-46-47-48-49-50-51-52-53-54-55-56-57-58-59-62-63-64-65-68-69-70-71-72-73-74-75-76-77-80-81-82-83)	-	2.0	V
461 to 477	Output Leakage Current Third State (Low Level Applied)	I_{OZL}	3006	4(h)	V_{IN} (3-State Control) = Note 4 V_{OUT} = 0V V_{DD} = 5.5V, V_{SS} = 0V (Pins 2-3-4-5-8-9-10-11-14-15-16-17-20-21-22-23)	-	−30	µA

NOTES: See Page 32.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	MIL-STD 883 TEST METHOD	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
478 to 494	Output Leakage Current Third State (High Level Applied)	I_{OZH}	3006	4(h)	V_{IN} (3-State Control) = Note 4 V_{OUT} = 5.5V V_{DD} = 5.5V, V_{SS} = 0V (Pins 2-3-4-5-8-9-10-11-14-15-16-17-20-21-22-23)	30	-	µA
495	Supply Current (During Normal Operation)	I_{DDS}	3005	4(a)	V_{IL} = 0V, V_{IH} = 5.5V I_{OL} = − 0.5mA V_{DD} = 5.5V, V_{SS} = 0V Note 5 (Pins 1 + 19 + 25 + 61 + 67 + 79)	-	40	mA

NOTES

1. Pattern for functional test:

No.	PATTERN	VECTOR LENGTH
1	Func1MHz	31278
2	Func4MHz	71260
3	Func16MHz	15066
4	EXTI.CTL	15719
5	ETD.STAT.LTMS	16307
6	fl.ETA	29762
7	MPI	6324
8	fa.Synchr__EXTCLK + SW	6698
9	fa.Synchr__EXTCOUNT	15702
10	Resetpattern	30
11	fa.LTMS.Inputs	822
12	Output0	38
13	Output1	129
14	mproc	158

2. Measurement is performed with the device having been initialised using functional test pattern "reset", stopped at end of pattern. Total combined current for all V_{DD} Pins.
3. The output pin under test is configured into correct state for the measurement by using a functional test pattern on the inputs with produces a low or high at the pin, as appropriate.
4. The device is configured using a functional test pattern so that the pin under test is in the Third-State condition for the measurement. The measurement includes the input currents I_{IL} and I_{IH}.
5. Test vectors 9940 to 15538 of functional test pattern Func4MHz are used for measurement of I_{DDS}.
6. Guaranteed but not tested. Characterised after major process changes.
7. Parameters tested go-no-go during Functional tests 2, 3 and 4.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS

No.	CHARACTERISTICS	SYMBOL	MIL-STD 883 TEST METHOD	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
496 to 531	Input Capacitance	C_{IN}	3012	4(i)	V_{IN} (Not Under Test) = 0V $V_{DD} = V_{SS} = 0V$ Note 6 (Pins 28-29-30-31-32-33-34-35-36-37-38-39-40-41-42-43-44-45-46-47-48-49-50-51-52-53-54-55-56-70-71-72-73-74-75)	-	10	pF
532 to 547	Input/Output Capacitance	$C_{IN/OUT}$	3012	4(i)	V_{IN} (Not Under Test) = 0V $V_{DD} = V_{SS} = 0V$ Note 6 (Pins 2-3-4-5-8-9-10-11-14-15-16-17-20-21-22-23)	-	15	pF
548 to 559	Output Capacitance	C_{OUT}	3012	4(i)	V_{IN} (Not Under Test) = 0V $V_{DD} = V_{SS} = 0V$ Note 6 (Pins 26-27-57-58-59-62-63-64-65-68-69-76)	-	15	pF
560	Rise and Fall Time (CMOS Inputs)	t_r/t_f	3004	-	Note 7	-	100	ns
561 to 563	MPROCLK Low to ETALRM Low	TM	3003	-	Note 7	-	77	ns
564 to 566	DPLL Delay	TDPLL	3003	-	AUXTAL = 1 $I_{OUT} = \pm 2.0mA$ $C_L = 100pF \pm 20\%$ Note 7	-	65	ns
567	Oscillator Frequency	FX	3003	-	AUXTAL = 1 $I_{OUT} = \pm 2.0mA$ $C_L = 100pF \pm 20\%$ Note 7	2^{24}	-	Hz
568 to 570	XTAL1 to XTALCLK Valid	TXX	3003	-	AUXTAL = 1 $I_{OUT} = \pm 2.0mA$ $C_L = 100pF \pm 20\%$ Note 7	-	26	ns
571 to 573	XTAL1 High to MEANFREQ Valid	TXDPR	3003	-	AUXTAL = 1 $I_{OUT} = \pm 2.0mA$ $C_L = 100pF \pm 20\%$ Note 7	-	80	ns
574 to 576	XTAL1 High to DPHASE Valid	TXDP	3003	-	AUXTAL = 1 $I_{OUT} = \pm 2.0mA$ $C_L = 100pF \pm 20\%$ Note 7	-	80	ns
577 to 579	XTAL1 High to WINDOW Valid	TXWD	3003	-	AUXTAL = 1 $I_{OUT} = \pm 2.0mA$ $C_L = 100pF \pm 20\%$ Note 7	-	102	ns

NOTES: See Page 32.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	MIL-STD 883 TEST METHOD	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
580 to 582	XTAL1 High to ETALRM High	TXAL	3003	-	AUXTAL = 1 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	-	105	ns
583 to 585	XTAL1 High to TVLD Valid	TXV	3003	-	AUXTAL = 1 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	-	104	ns
586 to 588	XTAL1 High to PFGPHOUT Valid	TXPH	3003	-	AUXTAL = 1 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	-	104	ns
589 to 591	XTAL1 High to PFGWAVE Valid	TXWV	3003	-	AUXTAL = 1 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	-	104	ns
592 to 594	XTAL1 High to EXTCOUNT Valid	TXXC	3003	-	AUXTAL = 1 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	-	94	ns
595 to 597	XTAL1 High EXTSHTEN Valid	TXSH	3003	-	AUXTAL = 1 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	-	118	ns
598 to 600	XTAL1 High to EXTDATA Valid	TXDT	3003	-	AUXTAL = 1 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	-	118	ns
601 to 603	XTAL1 High to EXTDEMUX Valid	TXDMX	3003	-	AUXTAL = 1 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	-	118	ns
604 to 606	XTAL1 High to EXTCLK Valid	TXXCK	3003	-	AUXTAL = 1 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	-	64	ns
607 to 609	XTAL1 High to EXTETID Low	TXLDF	3003	-	AUXTAL = 1 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	-	81	ns

NOTES: See Page 32.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	MIL-STD 883 TEST METHOD	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
610 to 612	XTAL1 High to EXTETID High	TXLDR	3003	-	AUXTAL = 1 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	-	111	ns
613 to 615	BUSCLK to MEANFREQ	TBDPR	3003	-	AUXTAL = 0 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	-	42	ns
616 to 618	BUSCLK to DPHASE	TBDP	3003	-	AUXTAL = 0 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	-	42	ns
619 to 621	BUSCLK High to WINDOW Valid	TBWD	3003	-	AUXTAL = 0 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	-	74	ns
622 to 624	BUSCLK High to ETALRM High	TBAL	3003	-	AUXTAL = 0 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	-	75	ns
625 to 627	BUSCLK High to TVLD Valid	TBV	3003	-	AUXTAL = 0 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	-	74	ns
628 to 630	BUSCLK High to PFGPHOUT Valid	TBPH	3003	-	AUXTAL = 0 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	-	74	ns
631 to 633	BUSCLK to EXTCOUNT	TBXC	3003	-	AUXTAL = 0 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	-	62	ns
634 to 636	BUSCLK Low to EXTSHTEN Valid	TBSH	3003	-	AUXTAL = 0 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	-	87	ns
637 to 639	BUSCLK Low to EXTDATA Valid	TBDT	3003	-	AUXTAL = 0 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	-	87	ns

NOTES: See Page 32.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	MIL-STD 883 TEST METHOD	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
640 to 642	BUSCLK Low to EXTDEMUX Valid	TBDMX	3003	-	AUXTAL = 0 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	-	87	ns
643 to 645	BUSCLK to EXTCLK	TBXCK	3003	-	AUXTAL = 0 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	-	50	ns
646 to 648	BUSCLK Low to EXTETLD Low	TBLDF	3003	-	AUXTAL = 0 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	-	96	ns
649 to 651	BUSCLK Low to EXTETLD High	TBLDR	3003	-	AUXTAL = 0 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	-	96	ns
652 to 654	DATA Setup to MPROCLK High	t4s	3003	-	I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	6.0	-	ns
655 to 657	DATA Hold to MPROCLK High	t4h	3003	-	I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	3.0	-	ns
658 to 660	AD Setup to MPROCLK High	t6s	3003	-	I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	0	-	ns
661 to 663	AD Hold to MPROCLK High	t6h	3003	-	I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	11	-	ns
664 to 666	$\overline{CS}$ Setup to MPROCLK Low	t1s	3003	-	MPROC = 0 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	1.0	-	ns
667 to 669	$\overline{CS}$ Hold to MPROCLK Low	t1h	3003	-	MPROC = 0 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	9.0	-	ns
670 to 672	$\overline{RD}$ Setup to MPROCLK Low	t2s	3003	-	MPROC = 0 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	2.0	-	ns

NOTES: See Page 32.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	MIL-STD 883 TEST METHOD	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
673 to 675	$\overline{RD}$ Hold to MPROCLK Low	t2h	3003	-	MPROC = 0 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	8.0	-	ns
676 to 678	$\overline{WR}$ Setup to MPROCLK Low	t3s	3003	-	MPROC = 0 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	1.0	-	ns
679 to 681	$\overline{WR}$ Hold to MPROCLK Low	t3h	3003	-	MPROC = 0 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	9.0	-	ns
682 to 684	$\overline{CS}$ and $\overline{WR}$ Hold to MPROCLK High	t5s	3003	-	MPROC = 0 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	13	-	ns
685 to 687	$\overline{CS}$ and $\overline{WR}$ Hold to MPROCLK High	t5h	3003	-	MPROC = 0 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	7.0	-	ns
688 to 690	DATA Enable Delay after MPROCLK Low	t7	3003	-	MPROC = 0 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	58	-	ns
691 to 693	DATA Valid after Deassertion of $\overline{RD}$ or $\overline{CS}$	t9	3003	-	MPROC = 0 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	59	-	ns
694 to 696	AD Hold after Deassertion of $\overline{RD}$ or $\overline{CS}$	t10	3003	-	MPROC = 0 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	19	-	ns
697 to 699	$\overline{RD}$ Setup to MPROCLK High	t11s	3003	-	MPROC = 1 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	9.0	-	ns
700 to 702	$\overline{RD}$ Setup to MPROCLK High	t12s	3003	-	MPROC = 1 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	9.0	-	ns

NOTES: See Page 32.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	MIL-STD 883 TEST METHOD	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
703 to 705	$\overline{RD}$ Hold to MPROCLK High	t12h	3003	-	MPROC = 1 I_{OUT} = ±2.0mA C_L = 100pF ±20% Note 7	12	-	ns
706 to 708	$\overline{WR}$ Setup to MPROCLK High	t13s	3003	-	MPROC = 1 I_{OUT} = ±2.0mA C_L = 100pF ±20% Note 7	9.0	-	ns
709 to 711	$\overline{WR}$ Low Hold to MPROCLK High	t13h	3003	-	MPROC = 1 I_{OUT} = ±2.0mA C_L = 100pF ±20% Note 7	3.0	-	ns
712 to 714	$\overline{WR}$ High Hold to MPROCLK High	t15h	3003	-	MPROC = 1 I_{OUT} = ±2.0mA C_L = 100pF ±20% Note 7	7.0	-	ns
715 to 717	DATA Enable Delay After Assertion of $\overline{CS}$	t16	3003	-	MPROC = 1 I_{OUT} = ±2.0mA C_L = 100pF ±20% Note 7	-	50	ns
718 to 720	DATA Enable after Deassertion of $\overline{RD}$	t17	3003	-	MPROC = 1 I_{OUT} = ±2.0mA C_L = 100pF ±20% Note 7	-	50	ns
721 to 723	DATA Valid after MPROCLK High	t18	3003	-	MPROC = 1 I_{OUT} = ±2.0mA C_L = 100pF ±20% Note 7	-	72	ns
724 to 726	DATA Valid after Deassertion of $\overline{RD}$	t19	3003	-	MPROC = 1 I_{OUT} = ±2.0mA C_L = 100pF ±20% Note 7	-	59	ns
727 to 729	MPROCLK Low to $\overline{READY}$ Valid	t20	3003	-	MPROC = 1 I_{OUT} = ±2.0mA C_L = 100pF ±20% Note 7	-	36	ns
730 to 732	AD Hold after Deassertion of $\overline{RD}$	t22	3003	-	MPROC = 1 I_{OUT} = ±2.0mA C_L = 100pF ±20% Note 7	-	19	ns

NOTES: See Page 32.

TABLE 3(a) - ELECTRICAL MEASUREMENTS AT HIGH TEMPERATURE - d.c. PARAMETERS

No.	CHARACTERISTICS	SYMBOL	MIL-STD 883 TEST METHOD	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
1	Functional Test 1 (Basic)	-	3014	-	Verify Device Operation with Load V_{IL} = 0V, V_{IH} = 5.0V V_{OL} = 1.0V, V_{OH} = 4.0V I_{OUT} = ±2.0mA C_L = 100pF ± 20% V_{DD} = 5.0V, V_{SS} = 0V Pattern = Note 1	-	-	-
2	Functional Test 2 (Nominal Voltage)	-	3014	-	Verify Device Operation with Load V_{IL} = 0.5V, V_{IH} = 4.5V V_{OL} = 1.0V, V_{OH} = 4.0V I_{OUT} = ±2.0mA C_L = 100pF ± 20% V_{DD} = 5.0V, V_{SS} = 0V Pattern = Note 1	-	-	-
3	Functional Test 3 (High Voltage)	-	3014	-	Verify Device Operation with Load V_{IL} = 0.5V, V_{IH} = 5.0V V_{OL} = 1.0V, V_{OH} = 4.5V I_{OUT} = ±2.0mA C_L = 100pF ± 20% V_{DD} = 5.5V, V_{SS} = 0V Pattern = Note 1	-	-	-
4	Functional Test 4 (Low Voltage)	-	3014	-	Verify Device Operation with Load V_{IL} = 0.5V, V_{IH} = 4.0V V_{OL} = 1.0V, V_{OH} = 3.5V I_{OUT} = ±2.0mA C_L = 100pF ± 20% V_{DD} = 4.5V, V_{SS} = 0V Pattern = Note 1	-	-	-
5	Quiescent Current	I_{DD}	3005	4(a)	V_{IL} = 0V, V_{IH} = 5.5V V_{DD} = 5.5V, V_{SS} = 0V All Outputs Open Note 2 (Pins 1 + 19 + 25 + 61 + 67 + 79)	-	10	mA
6 to 41	Input Current Low Level	I_{IL}	3009	4(b)	V_{IN} (Under Test) = 0V V_{IN} (Remaining Inputs) = 5.5V V_{DD} = 5.5V, V_{SS} = 0V (Pins 28-29-30-31-32-33-34-35-36-37-38-39-40-41-42-43-44-45-46-47-48-49-50-51-52-53-54-55-56-70-71-72-73-74-75)	-	−10	µA

NOTES: See Page 32.

TABLE 3(a) - ELECTRICAL MEASUREMENTS AT HIGH TEMPERATURE - d.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	MIL-STD 883 TEST METHOD	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
42 to 77	Input Current High Level	I_{IH}	3009	4(c)	V_{IN} (Under Test) = 5.5V V_{IN} (Remaining Inputs) = 0V V_{DD} = 5.5V, V_{SS} = 0V (Pins 28-29-30-31-32-33-34-35-36-37-38-39-40-41-42-43-44-45-46-47-48-49-50-51-52-53-54-55-56-70-71-72-73-74-75)	10	-	µA
78 to 110	Output Voltage Low Level 1	V_{OL1}	3007	4(d)	V_{IL} = 0.5V, V_{IH} = 4.0V I_{OL} = 4.0mA V_{DD} = 4.5V, V_{SS} = 0V Note 9 (Pins 2-3-4-5-8-9-10-11-14-15-16-17-20-21-22-23-26-27-57-58-59-62-63-64-65-68-69-77-80-81-82-83)	-	0.4	V
111	Output Voltage Low Level 2	V_{OL2}	3007	4(d)	V_{IL} = 0.5V, V_{IH} = 4.0V I_{OL} = 0.5mA V_{DD} = 4.5V, V_{SS} = 0V Note 3 (Pin 76)	-	0.4	V
112 to 144	Output Voltage High Level 1	V_{OH1}	3006	4(e)	V_{IL} = 0.5V, V_{IH} = 4.0V I_{OL} = −4.0mA V_{DD} = 4.5V, V_{SS} = 0V Note 3 (Pins 2-3-4-5-8-9-10-11-14-15-16-17-20-21-22-23-26-27-57-58-59-62-63-64-65-68-69-77-80-81-82-83)	3.9	-	V
145 to 177	Output Voltage High Level 2	V_{OH2}	3006	4(e)	V_{IL} = 0.5V, V_{IH} = 4.0V I_{OL} = −0.5mA V_{DD} = 4.5V, V_{SS} = 0V Note 3 (Pins 2-3-4-5-8-9-10-11-14-15-16-17-20-21-22-23-26-27-57-58-59-62-63-64-65-68-69-77-80-81-82-83)	4.2	-	V
178	Output Voltage High Level 3	V_{OH3}	3006	4(e)	V_{IL} = 0.5V, V_{IH} = 4.0V I_{OL} = −0.5mA V_{DD} = 4.5V, V_{SS} = 0V Note 3 (Pin 76)	3.9	-	V
179 to 214	Threshold Voltage Low Level 1 (CMOS Inputs)	V_{THN1}	-	4(f)	V_{DD} = 4.5V, V_{SS} = 0V (Pins 28-29-30-31-32-33-34-35-36-37-38-39-40-41-42-43-44-45-46-47-48-49-50-51-52-53-54-55-56-70-71-72-73-74-75)	1.3	-	V

NOTES: See Page 32.

TABLE 3(a) - ELECTRICAL MEASUREMENTS AT HIGH TEMPERATURE - d.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	MIL-STD 883 TEST METHOD	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
215 to 250	Threshold Voltage High Level 1 (CMOS Inputs)	V_{THP1}	-	4(f)	V_{DD} = 4.5V, V_{SS} = 0V (Pins 28-29-30-31-32-33-34-35-36-37-38-39-40-41-42-43-44-45-46-47-48-49-50-51-52-53-54-55-56-70-71-72-73-74-75)	-	3.2	V
251 to 286	Threshold Voltage Low Level 2 (CMOS Inputs)	V_{THN2}	-	4(f)	V_{DD} = 5.5V, V_{SS} = 0V (Pins 28-29-30-31-32-33-34-35-36-37-38-39-40-41-42-43-44-45-46-47-48-49-50-51-52-53-54-55-56-70-71-72-73-74-75)	1.7	-	V
287 to 322	Threshold Voltage High Level 2 (CMOS Inputs)	V_{THP2}	-	4(f)	V_{DD} = 5.5V, V_{SS} = 0V (Pins 28-29-30-31-32-33-34-35-36-37-38-39-40-41-42-43-44-45-46-47-48-49-50-51-52-53-54-55-56-70-71-72-73-74-75)	-	3.9	V
323 to 391	Input/Output Clamp Voltage (to V_{SS})	V_{IC1}	3022	4(g)	I_{IN} = −100µA V_{DD} = V_{SS} = 0V (Pins 2-3-4-5-8-9-10-11-14-15-16-17-20-21-22-23-26-27-28-29-30-31-32-33-34-35-36-37-38-39-40-41-42-43-44-45-46-47-48-49-50-51-52-53-54-55-56-57-58-59-62-63-64-65-68-69-70-71-72-73-74-75-76-77-80-81-82-83)	-	−2.0	V
392 to 460	Input/Output Clamp Voltage (to V_{DD})	V_{IC2}	3022	4(g)	I_{IN} = 100µA V_{DD} = V_{SS} = 0V (Pins 2-3-4-5-8-9-10-11-14-15-16-17-20-21-22-23-26-27-28-29-30-31-32-33-34-35-36-37-38-39-40-41-42-43-44-45-46-47-48-49-50-51-52-53-54-55-56-57-58-59-62-63-64-65-68-69-70-71-72-73-74-75-76-77-80-81-82-83)	-	2.0	V
461 to 477	Output Leakage Current Third State (Low Level Applied)	I_{OZL}	3006	4(h)	V_{IN} (3-State Control) = Note 4 V_{OUT} = 0V V_{DD} = 5.5V, V_{SS} = 0V (Pins 2-3-4-5-8-9-10-11-14-15-16-17-20-21-22-23)	-	−100	µA

NOTES: See Page 32.

TABLE 3(a) - ELECTRICAL MEASUREMENTS AT HIGH TEMPERATURE - d.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	MIL-STD 883 TEST METHOD	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
478 to 494	Output Leakage Current Third State (High Level Applied)	I_{OZH}	3006	4(h)	V_{IN} (3-State Control) = Note 4 V_{OUT} = 5.5V V_{DD} = 5.5V, V_{SS} = 0V (Pins 2-3-4-5-8-9-10-11-14-15-16-17-20-21-22-23)	100	-	µA
495	Supply Current (During Normal Operation)	I_{DDS}	3005	4(a)	V_{IL} = 0V, V_{IH} = 5.5V I_{OL} = − 0.5mA V_{DD} = 5.5V, V_{SS} = 0V Note 5 (Pins 1 + 19 + 25 + 61 + 67 + 79)	-	50	mA

NOTES: See Page 32.

TABLE 3(a) - ELECTRICAL MEASUREMENTS AT HIGH TEMPERATURE - a.c. PARAMETERS

No.	CHARACTERISTICS	SYMBOL	MIL-STD 883 TEST METHOD	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
561 to 563	MPROCLK Low to ETALRM Low	TM	3003	-	Note 7	-	77	ns
564 to 566	DPLL Delay	TDPLL	3003	-	AUXTAL = 1 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	-	65	ns
568 to 570	XTAL1 to XTALCLK Valid	TXX	3003	-	AUXTAL = 1 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	-	26	ns
571 to 573	XTAL1 High to MEANFREQ Valid	TXDPR	3003	-	AUXTAL = 1 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	-	80	ns
574 to 576	XTAL1 High to DPHASE Valid	TXDP	3003	-	AUXTAL = 1 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	-	80	ns
577 to 579	XTAL1 High to WINDOW Valid	TXWD	3003	-	AUXTAL = 1 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	-	102	ns
580 to 582	XTAL1 High to ETALRM High	TXAL	3003	-	AUXTAL = 1 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	-	105	ns
583 to 585	XTAL1 High to TVLD Valid	TXV	3003	-	AUXTAL = 1 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	-	104	ns
586 to 588	XTAL1 High to PFGPHOUT Valid	TXPH	3003	-	AUXTAL = 1 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	-	104	ns
589 to 591	XTAL1 High to PFGWAVE Valid	TXWV	3003	-	AUXTAL = 1 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	-	104	ns
592 to 594	XTAL1 High to EXTCOUNT Valid	TXXC	3003	-	AUXTAL = 1 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	-	94	ns

NOTES: See Page 32.

TABLE 3(a) - ELECTRICAL MEASUREMENTS AT HIGH TEMPERATURE - a.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	MIL-STD 883 TEST METHOD	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
595 to 597	XTAL1 High EXTSHTEN Valid	TXSH	3003	-	AUXTAL = 1 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	-	118	ns
598 to 600	XTAL1 High to EXTDATA Valid	TXDT	3003	-	AUXTAL = 1 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	-	118	ns
601 to 603	XTAL1 High to EXTDEMUX Valid	TXDMX	3003	-	AUXTAL = 1 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	-	118	ns
604 to 606	XTAL1 High to EXTCLK Valid	TXXCK	3003	-	AUXTAL = 1 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	-	64	ns
607 to 609	XTAL1 High to EXTETID Low	TXLDF	3003	-	AUXTAL = 1 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	-	81	ns
610 to 612	XTAL1 High to EXTETID High	TXLDR	3003	-	AUXTAL = 1 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	-	111	ns
613 to 615	BUSCLK to MEANFREQ	TBDPR	3003	-	AUXTAL = 0 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	-	42	ns
616 to 618	BUSCLK to DPHASE	TBDP	3003	-	AUXTAL = 0 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	-	42	ns
619 to 621	BUSCLK High to WINDOW Valid	TBWD	3003	-	AUXTAL = 0 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	-	74	ns
622 to 624	BUSCLK High to ETALRM High	TBAL	3003	-	AUXTAL = 0 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	-	75	ns

NOTES: See Page 32.

TABLE 3(a) - ELECTRICAL MEASUREMENTS AT HIGH TEMPERATURE - a.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	MIL-STD 883 TEST METHOD	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
625 to 627	BUSCLK High to TVLD Valid	TBV	3003	-	AUXTAL = 0 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	-	74	ns
628 to 630	BUSCLK High to PFGPHOUT Valid	TBPH	3003	-	AUXTAL = 0 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	-	74	ns
631 to 633	BUSCLK to EXTCOUNT	TBXC	3003	-	AUXTAL = 0 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	-	62	ns
634 to 636	BUSCLK Low to EXTSHTEN Valid	TBSH	3003	-	AUXTAL = 0 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	-	87	ns
637 to 639	BUSCLK Low to EXTDATA Valid	TBDT	3003	-	AUXTAL = 0 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	-	87	ns
640 to 642	BUSCLK Low to EXTDEMUX Valid	TBDMX	3003	-	AUXTAL = 0 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	-	87	ns
643 to 645	BUSCLK to EXTCLK	TBXCK	3003	-	AUXTAL = 0 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	-	50	ns
646 to 648	BUSCLK Low to EXTETLD Low	TBLDF	3003	-	AUXTAL = 0 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	-	96	ns
649 to 651	BUSCLK Low to EXTETLD High	TBLDR	3003	-	AUXTAL = 0 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	-	96	ns
652 to 654	DATA Setup to MPROCLK High	t4s	3003	-	I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	6.0	-	ns

NOTES: See Page 32.

TABLE 3(a) - ELECTRICAL MEASUREMENTS AT HIGH TEMPERATURE - a.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	MIL-STD 883 TEST METHOD	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
655 to 657	DATA Hold to MPROCLK High	t4h	3003	-	I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	3.0	-	ns
658 to 660	AD Setup to MPROCLK High	t6s	3003	-	I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	0	-	ns
661 to 663	AD Hold to MPROCLK High	t6h	3003	-	I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	11	-	ns
664 to 666	$\overline{CS}$ Setup to MPROCLK Low	t1s	3003	-	MPROC = 0 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	1.0	-	ns
667 to 669	$\overline{CS}$ Hold to MPROCLK Low	t1h	3003	-	MPROC = 0 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	9.0	-	ns
670 to 672	$\overline{RD}$ Setup to MPROCLK Low	t2s	3003	-	MPROC = 0 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	2.0	-	ns
673 to 675	$\overline{RD}$ Hold to MPROCLK Low	t2h	3003	-	MPROC = 0 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	8.0	-	ns
676 to 678	$\overline{WR}$ Setup to MPROCLK Low	t3s	3003	-	MPROC = 0 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	1.0	-	ns
679 to 681	$\overline{WR}$ Hold to MPROCLK Low	t3h	3003	-	MPROC = 0 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	9.0	-	ns
682 to 684	$\overline{CS}$ and $\overline{WR}$ Hold to MPROCLK High	t5s	3003	-	MPROC = 0 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	13	-	ns
685 to 687	$\overline{CS}$ and $\overline{WR}$ Hold to MPROCLK High	t5h	3003	-	MPROC = 0 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	7.0	-	ns

NOTES: See Page 32.

TABLE 3(a) - ELECTRICAL MEASUREMENTS AT HIGH TEMPERATURE - a.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	MIL-STD 883 TEST METHOD	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
688 to 690	DATA Enable Delay after MPROCLK Low	t7	3003	-	MPROC = 0 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	58	-	ns
691 to 693	DATA Valid after Deassertion of $\overline{RD}$ or $\overline{CS}$	t9	3003	-	MPROC = 0 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	59	-	ns
694 to 696	AD Hold after Deassertion of $\overline{RD}$ or $\overline{CS}$	t10	3003	-	MPROC = 0 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	19	-	ns
697 to 699	$\overline{RD}$ Setup to MPROCLK High	t11s	3003	-	MPROC = 1 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	9.0	-	ns
700 to 702	$\overline{RD}$ Setup to MPROCLK High	t12s	3003	-	MPROC = 1 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	9.0	-	ns
703 to 705	$\overline{RD}$ Hold to MPROCLK High	t12h	3003	-	MPROC = 1 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	12	-	ns
706 to 708	$\overline{WR}$ Setup to MPROCLK High	t13s	3003	-	MPROC = 1 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	9.0	-	ns
709 to 711	$\overline{WR}$ Low Hold to MPROCLK High	t13h	3003	-	MPROC = 1 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	3.0	-	ns
712 to 714	$\overline{WR}$ High Hold to MPROCLK High	t15h	3003	-	MPROC = 1 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	7.0	-	ns
715 to 717	DATA Enable Delay After Assertion of $\overline{CS}$	t16	3003	-	MPROC = 1 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	-	50	ns

NOTES: See Page 32.

TABLE 3(a) - ELECTRICAL MEASUREMENTS AT HIGH TEMPERATURE - a.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	MIL-STD 883 TEST METHOD	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
718 to 720	DATA Enable after Deassertion of $\overline{RD}$	t17	3003	-	MPROC = 1 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	-	50	ns
721 to 723	DATA Valid after MPROCLK High	t18	3003	-	MPROC = 1 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	-	72	ns
724 to 726	DATA Valid after Deassertion of $\overline{RD}$	t19	3003	-	MPROC = 1 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	-	59	ns
727 to 729	MPROCLK Low to $\overline{READY}$ Valid	t20	3003	-	MPROC = 1 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	-	36	ns
730 to 732	AD Hold after Deassertion of $\overline{RD}$	t22	3003	-	MPROC = 1 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	-	19	ns

NOTES: See Page 32.

TABLE 3(b) - ELECTRICAL MEASUREMENTS AT LOW TEMPERATURE - d.c. PARAMETERS

No.	CHARACTERISTICS	SYMBOL	MIL-STD 883 TEST METHOD	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
1	Functional Test 1 (Basic)	-	3014	-	Verify Device Operation with Load V_{IL} = 0V, V_{IH} = 5.0V V_{OL} = 1.0V, V_{OH} = 4.0V I_{OUT} = ±2.0mA C_L = 100pF ± 20% V_{DD} = 5.0V, V_{SS} = 0V Pattern = Note 1	-	-	-
2	Functional Test 2 (Nominal Voltage)	-	3014	-	Verify Device Operation with Load V_{IL} = 0.5V, V_{IH} = 4.5V V_{OL} = 1.0V, V_{OH} = 4.0V I_{OUT} = ±2.0mA C_L = 100pF ± 20% V_{DD} = 5.0V, V_{SS} = 0V Pattern = Note 1	-	-	-
3	Functional Test 3 (High Voltage)	-	3014	-	Verify Device Operation with Load V_{IL} = 0.5V, V_{IH} = 5.0V V_{OL} = 1.0V, V_{OH} = 4.5V I_{OUT} = ±2.0mA C_L = 100pF ± 20% V_{DD} = 5.5V, V_{SS} = 0V Pattern = Note 1	-	-	-
4	Functional Test 4 (Low Voltage)	-	3014	-	Verify Device Operation with Load V_{IL} = 0.5V, V_{IH} = 4.0V V_{OL} = 1.0V, V_{OH} = 3.5V I_{OUT} = ±2.0mA C_L = 100pF ± 20% V_{DD} = 4.5V, V_{SS} = 0V Pattern = Note 1	-	-	-
5	Quiescent Current	I_{DD}	3005	4(a)	V_{IL} = 0V, V_{IH} = 5.5V V_{DD} = 5.5V, V_{SS} = 0V All Outputs Open Note 2 (Pins 1 + 19 + 25 + 61 + 67 + 79)	-	10	mA
6 to 41	Input Current Low Level	I_{IL}	3009	4(b)	V_{IN} (Under Test) = 0V V_{IN} (Remaining Inputs) = 5.5V V_{DD} = 5.5V, V_{SS} = 0V (Pins 28-29-30-31-32-33-34-35-36-37-38-39-40-41-42-43-44-45-46-47-48-49-50-51-52-53-54-55-56-70-71-72-73-74-75)	-	−2.0	µA

NOTES: See Page 32.

TABLE 3(b) - ELECTRICAL MEASUREMENTS AT LOW TEMPERATURE - d.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	MIL-STD 883 TEST METHOD	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
42 to 77	Input Current High Level	I_{IH}	3009	4(c)	V_{IN} (Under Test) = 5.5V V_{IN} (Remaining Inputs) = 0V V_{DD} = 5.5V, V_{SS} = 0V (Pins 28-29-30-31-32-33-34-35-36-37-38-39-40-41-42-43-44-45-46-47-48-49-50-51-52-53-54-55-56-70-71-72-73-74-75)	2.0	-	µA
78 to 110	Output Voltage Low Level 1	V_{OL1}	3007	4(d)	V_{IL} = 0.5V, V_{IH} = 4.0V I_{OL} = 4.0mA V_{DD} = 4.5V, V_{SS} = 0V Note 9 (Pins 2-3-4-5-8-9-10-11-14-15-16-17-20-21-22-23-26-27-57-58-59-62-63-64-65-68-69-77-80-81-82-83)	-	0.4	V
111	Output Voltage Low Level 2	V_{OL2}	3007	4(d)	V_{IL} = 0.5V, V_{IH} = 4.0V I_{OL} = 0.5mA V_{DD} = 4.5V, V_{SS} = 0V Note 3 (Pin 76)	-	0.4	V
112 to 144	Output Voltage High Level 1	V_{OH1}	3006	4(e)	V_{IL} = 0.5V, V_{IH} = 4.0V I_{OL} = −4.0mA V_{DD} = 4.5V, V_{SS} = 0V Note 3 (Pins 2-3-4-5-8-9-10-11-14-15-16-17-20-21-22-23-26-27-57-58-59-62-63-64-65-68-69-77-80-81-82-83)	3.9	-	V
145 to 177	Output Voltage High Level 2	V_{OH2}	3006	4(e)	V_{IL} = 0.5V, V_{IH} = 4.0V I_{OL} = −0.5mA V_{DD} = 4.5V, V_{SS} = 0V Note 3 (Pins 2-3-4-5-8-9-10-11-14-15-16-17-20-21-22-23-26-27-57-58-59-62-63-64-65-68-69-77-80-81-82-83)	4.2	-	V
178	Output Voltage High Level 3	V_{OH3}	3006	4(e)	V_{IL} = 0.5V, V_{IH} = 4.0V I_{OL} = −0.5mA V_{DD} = 4.5V, V_{SS} = 0V Note 3 (Pin 76)	3.9	-	V
179 to 214	Threshold Voltage Low Level 1 (CMOS Inputs)	V_{THN1}	-	4(f)	V_{DD} = 4.5V, V_{SS} = 0V (Pins 28-29-30-31-32-33-34-35-36-37-38-39-40-41-42-43-44-45-46-47-48-49-50-51-52-53-54-55-56-70-71-72-73-74-75)	1.3	-	V

NOTES: See Page 32.

TABLE 3(b) - ELECTRICAL MEASUREMENTS AT LOW TEMPERATURE - d.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	MIL-STD 883 TEST METHOD	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
215 to 250	Threshold Voltage High Level 1 (CMOS Inputs)	V_{THP1}	-	4(f)	V_{DD} = 4.5V, V_{SS} = 0V (Pins 28-29-30-31-32-33-34-35-36-37-38-39-40-41-42-43-44-45-46-47-48-49-50-51-52-53-54-55-56-70-71-72-73-74-75)	-	3.2	V
251 to 286	Threshold Voltage Low Level 2 (CMOS Inputs)	V_{THN2}	-	4(f)	V_{DD} = 5.5V, V_{SS} = 0V (Pins 28-29-30-31-32-33-34-35-36-37-38-39-40-41-42-43-44-45-46-47-48-49-50-51-52-53-54-55-56-70-71-72-73-74-75)	1.7	-	V
287 to 322	Threshold Voltage High Level 2 (CMOS Inputs)	V_{THP2}	-	4(f)	V_{DD} = 5.5V, V_{SS} = 0V (Pins 28-29-30-31-32-33-34-35-36-37-38-39-40-41-42-43-44-45-46-47-48-49-50-51-52-53-54-55-56-70-71-72-73-74-75)	-	3.9	V
323 to 391	Input/Output Clamp Voltage (to V_{SS})	V_{IC1}	3022	4(g)	I_{IN} = −100µA V_{DD} = V_{SS} = 0V (Pins 2-3-4-5-8-9-10-11-14-15-16-17-20-21-22-23-26-27-28-29-30-31-32-33-34-35-36-37-38-39-40-41-42-43-44-45-46-47-48-49-50-51-52-53-54-55-56-57-58-59-62-63-64-65-68-69-70-71-72-73-74-75-76-77-80-81-82-83)	-	−2.0	V
392 to 460	Input/Output Clamp Voltage (to V_{DD})	V_{IC2}	3022	4(g)	I_{IN} = 100µA V_{DD} = V_{SS} = 0V (Pins 2-3-4-5-8-9-10-11-14-15-16-17-20-21-22-23-26-27-28-29-30-31-32-33-34-35-36-37-38-39-40-41-42-43-44-45-46-47-48-49-50-51-52-53-54-55-56-57-58-59-62-63-64-65-68-69-70-71-72-73-74-75-76-77-80-81-82-83)	-	2.0	V
461 to 477	Output Leakage Current Third State (Low Level Applied)	I_{OZL}	3006	4(h)	V_{IN} (3-State Control) = Note 4 V_{OUT} = 0V V_{DD} = 5.5V, V_{SS} = 0V (Pins 2-3-4-5-8-9-10-11-14-15-16-17-20-21-22-23)	-	−30	µA

NOTES: See Page 32.

TABLE 3(b) - ELECTRICAL MEASUREMENTS AT LOW TEMPERATURE - d.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	MIL-STD 883 TEST METHOD	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
478 to 494	Output Leakage Current Third State (High Level Applied)	I_{OZH}	3006	4(h)	V_{IN} (3-State Control) = Note 4 V_{OUT} = 5.5V V_{DD} = 5.5V, V_{SS} = 0V (Pins 2-3-4-5-8-9-10-11-14-15-16-17-20-21-22-23)	30	-	µA
495	Supply Current (During Normal Operation)	I_{DDS}	3005	4(a)	V_{IL} = 0V, V_{IH} = 5.5V I_{OL} = −0.5mA V_{DD} = 5.5V, V_{SS} = 0V Note 5 (Pins 1 + 19 + 25 + 61 + 67 + 79)	-	50	mA

NOTES: See Page 32.

TABLE 3(b) - ELECTRICAL MEASUREMENTS AT LOW TEMPERATURE - a.c. PARAMETERS

No.	CHARACTERISTICS	SYMBOL	MIL-STD 883 TEST METHOD	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
561 to 563	MPROCLK Low to ETALRM Low	TM	3003	-	Note 7	-	77	ns
564 to 566	DPLL Delay	TDPLL	3003	-	AUXTAL = 1 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	-	65	ns
568 to 570	XTAL1 to XTALCLK Valid	TXX	3003	-	AUXTAL = 1 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	-	26	ns
571 to 573	XTAL1 High to MEANFREQ Valid	TXDPR	3003	-	AUXTAL = 1 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	-	80	ns
574 to 576	XTAL1 High to DPHASE Valid	TXDP	3003	-	AUXTAL = 1 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	-	80	ns
577 to 579	XTAL1 High to WINDOW Valid	TXWD	3003	-	AUXTAL = 1 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	-	102	ns
580 to 582	XTAL1 High to ETALRM High	TXAL	3003	-	AUXTAL = 1 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	-	105	ns
583 to 585	XTAL1 High to TVLD Valid	TXV	3003	-	AUXTAL = 1 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	-	104	ns
586 to 588	XTAL1 High to PFGPHOUT Valid	TXPH	3003	-	AUXTAL = 1 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	-	104	ns
589 to 591	XTAL1 High to PFGWAVE Valid	TXWV	3003	-	AUXTAL = 1 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	-	104	ns
592 to 594	XTAL1 High to EXTCOUNT Valid	TXXC	3003	-	AUXTAL = 1 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	-	94	ns

NOTES: See Page 32.

TABLE 3(b) - ELECTRICAL MEASUREMENTS AT LOW TEMPERATURE - a.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	MIL-STD 883 TEST METHOD	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
595 to 597	XTAL1 High EXTSHTEN Valid	TXSH	3003	-	AUXTAL = 1 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	-	118	ns
598 to 600	XTAL1 High to EXTDATA Valid	TXDT	3003	-	AUXTAL = 1 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	-	118	ns
601 to 603	XTAL1 High to EXTDEMUX Valid	TXDMX	3003	-	AUXTAL = 1 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	-	118	ns
604 to 606	XTAL1 High to EXTCLK Valid	TXXCK	3003	-	AUXTAL = 1 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	-	64	ns
607 to 609	XTAL1 High to EXTETID Low	TXLDF	3003	-	AUXTAL = 1 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	-	81	ns
610 to 612	XTAL1 High to EXTETID High	TXLDR	3003	-	AUXTAL = 1 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	-	111	ns
613 to 615	BUSCLK to MEANFREQ	TBDPR	3003	-	AUXTAL = 0 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	-	42	ns
616 to 618	BUSCLK to DPHASE	TBDP	3003	-	AUXTAL = 0 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	-	42	ns
619 to 621	BUSCLK High to WINDOW Valid	TBWD	3003	-	AUXTAL = 0 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	-	74	ns
622 to 624	BUSCLK High to ETALRM High	TBAL	3003	-	AUXTAL = 0 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	-	75	ns

NOTES: See Page 32.

TABLE 3(b) - ELECTRICAL MEASUREMENTS AT LOW TEMPERATURE - a.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	MIL-STD 883 TEST METHOD	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
625 to 627	BUSCLK High to TVLD Valid	TBV	3003	-	AUXTAL = 0 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	-	74	ns
628 to 630	BUSCLK High to PFGPHOUT Valid	TBPH	3003	-	AUXTAL = 0 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	-	74	ns
631 to 633	BUSCLK to EXTCOUNT	TBXC	3003	-	AUXTAL = 0 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	-	62	ns
634 to 636	BUSCLK Low to EXTSHTEN Valid	TBSH	3003	-	AUXTAL = 0 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	-	87	ns
637 to 639	BUSCLK Low to EXTDATA Valid	TBDT	3003	-	AUXTAL = 0 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	-	87	ns
640 to 642	BUSCLK Low to EXTDEMUX Valid	TBDMX	3003	-	AUXTAL = 0 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	-	87	ns
643 to 645	BUSCLK to EXTCLK	TBXCK	3003	-	AUXTAL = 0 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	-	50	ns
646 to 648	BUSCLK Low to EXTETLD Low	TBLDF	3003	-	AUXTAL = 0 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	-	96	ns
649 to 651	BUSCLK Low to EXTETLD High	TBLDR	3003	-	AUXTAL = 0 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	-	96	ns
652 to 654	DATA Setup to MPROCLK High	t4s	3003	-	I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	6.0	-	ns

NOTES: See Page 32.

TABLE 3(b) - ELECTRICAL MEASUREMENTS AT LOW TEMPERATURE - a.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	MIL-STD 883 TEST METHOD	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
655 to 657	DATA Hold to MPROCLK High	t4h	3003	-	I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	3.0	-	ns
658 to 660	AD Setup to MPROCLK High	t6s	3003	-	I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	0	-	ns
661 to 663	AD Hold to MPROCLK High	t6h	3003	-	I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	11	-	ns
664 to 666	$\overline{CS}$ Setup to MPROCLK Low	t1s	3003	-	MPROC = 0 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	1.0	-	ns
667 to 669	$\overline{CS}$ Hold to MPROCLK Low	t1h	3003	-	MPROC = 0 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	9.0	-	ns
670 to 672	$\overline{RD}$ Setup to MPROCLK Low	t2s	3003	-	MPROC = 0 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	2.0	-	ns
673 to 675	$\overline{RD}$ Hold to MPROCLK Low	t2h	3003	-	MPROC = 0 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	8.0	-	ns
676 to 678	$\overline{WR}$ Setup to MPROCLK Low	t3s	3003	-	MPROC = 0 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	1.0	-	ns
679 to 681	$\overline{WR}$ Hold to MPROCLK Low	t3h	3003	-	MPROC = 0 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	9.0	-	ns
682 to 684	$\overline{CS}$ and $\overline{WR}$ Hold to MPROCLK High	t5s	3003	-	MPROC = 0 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	13	-	ns
685 to 687	$\overline{CS}$ and $\overline{WR}$ Hold to MPROCLK High	t5h	3003	-	MPROC = 0 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	7.0	-	ns

NOTES: See Page 32.

TABLE 3(b) - ELECTRICAL MEASUREMENTS AT LOW TEMPERATURE - a.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	MIL-STD 883 TEST METHOD	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
688 to 690	DATA Enable Delay after MPROCLK Low	t7	3003	-	MPROC = 0 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	58	-	ns
691 to 693	DATA Valid after Deassertion of $\overline{RD}$ or $\overline{CS}$	t9	3003	-	MPROC = 0 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	59	-	ns
694 to 696	AD Hold after Deassertion of $\overline{RD}$ or $\overline{CS}$	t10	3003	-	MPROC = 0 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	19	-	ns
697 to 699	$\overline{RD}$ Setup to MPROCLK High	t11s	3003	-	MPROC = 1 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	9.0	-	ns
700 to 702	$\overline{RD}$ Setup to MPROCLK High	t12s	3003	-	MPROC = 1 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	9.0	-	ns
703 to 705	$\overline{RD}$ Hold to MPROCLK High	t12h	3003	-	MPROC = 1 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	12	-	ns
706 to 708	$\overline{WR}$ Setup to MPROCLK High	t13s	3003	-	MPROC = 1 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	9.0	-	ns
709 to 711	$\overline{WR}$ Low Hold to MPROCLK High	t13h	3003	-	MPROC = 1 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	3.0	-	ns
712 to 714	$\overline{WR}$ High Hold to MPROCLK High	t15h	3003	-	MPROC = 1 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	7.0	-	ns
715 to 717	DATA Enable Delay After Assertion of $\overline{CS}$	t16	3003	-	MPROC = 1 I_{OUT} = ±2.0mA C_L = 100pF ± 20% Note 7	-	50	ns

NOTES: See Page 32.

TABLE 3(b) - ELECTRICAL MEASUREMENTS AT LOW TEMPERATURE - a.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	MIL-STD 883 TEST METHOD	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
718 to 720	DATA Enable after Deassertion of $\overline{RD}$	t17	3003	-	MPROC = 1 I_{OUT} = ±2.0mA C_L = 100pF ±20% Note 7	-	50	ns
721 to 723	DATA Valid after MPROCLK High	t18	3003	-	MPROC = 1 I_{OUT} = ±2.0mA C_L = 100pF ±20% Note 7	-	72	ns
724 to 726	DATA Valid after Deassertion of $\overline{RD}$	t19	3003	-	MPROC = 1 I_{OUT} = ±2.0mA C_L = 100pF ±20% Note 7	-	59	ns
727 to 729	MPROCLK Low to $\overline{READY}$ Valid	t20	3003	-	MPROC = 1 I_{OUT} = ±2.0mA C_L = 100pF ±20% Note 7	-	36	ns
730 to 732	AD Hold after Deassertion of $\overline{RD}$	t22	3003	-	MPROC = 1 I_{OUT} = ±2.0mA C_L = 100pF ±20% Note 7	-	19	ns

NOTES: See Page 32.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS

FIGURE 4(a)(i) - QUIESCENT CURRENT

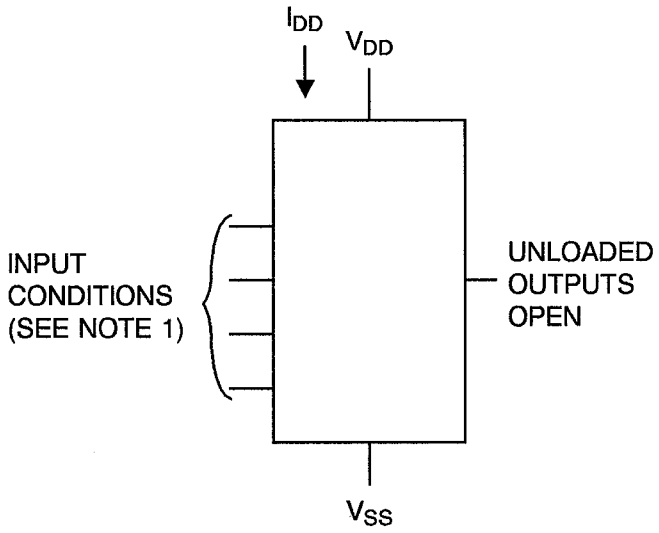
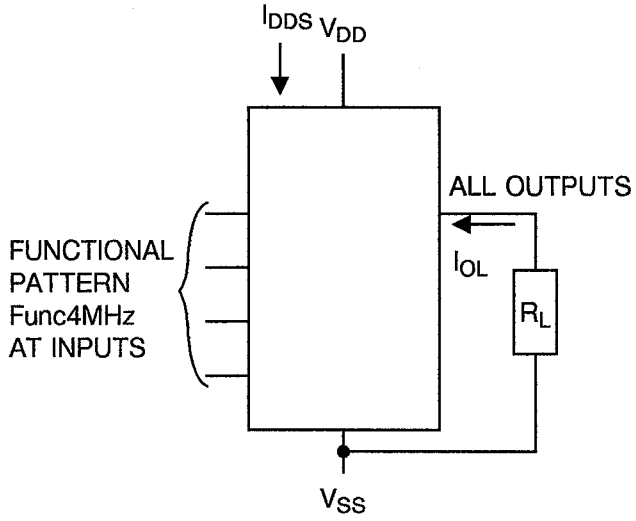
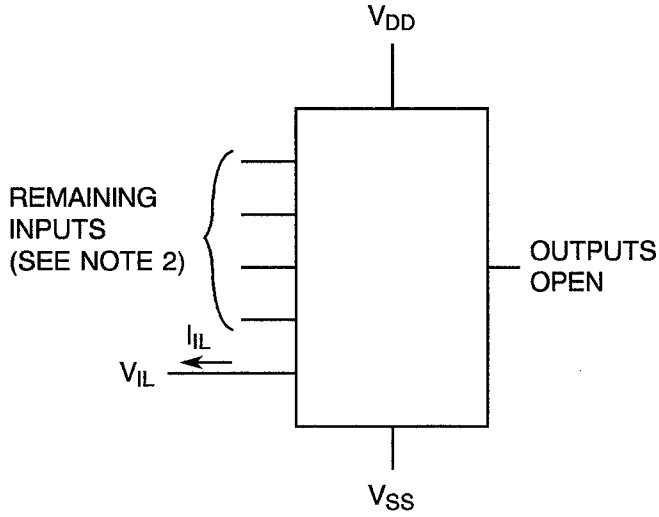


FIGURE 4(a)(ii) - SUPPLY CURRENT



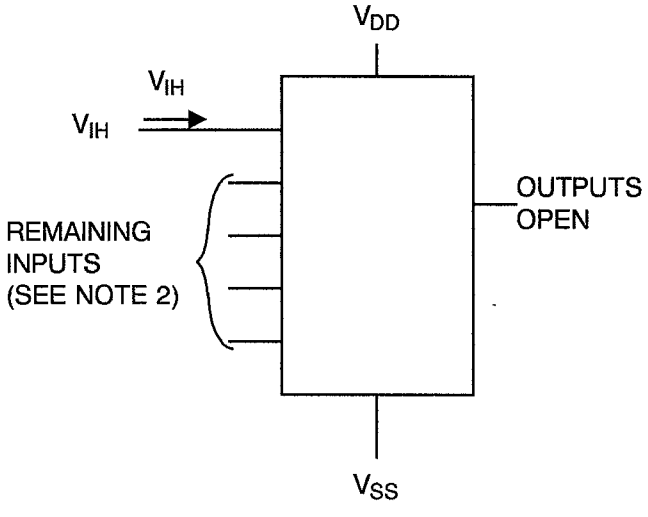
NOTES
1. Input conditions as per Table 2.

FIGURE 4(b) - INPUT CURRENT LOW LEVEL



NOTES
1. Each input to be tested separately.
2. Input conditions as per Table 2.

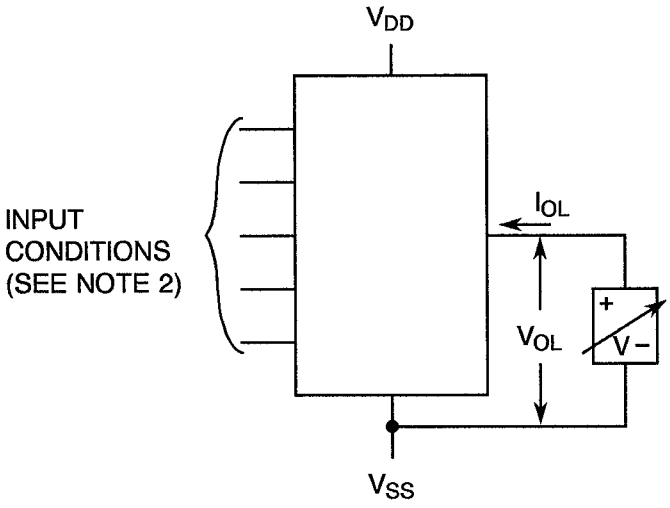
FIGURE 4(c) - INPUT CURRENT HIGH LEVEL



NOTES
1. Each input to be tested separately.
2. Input conditions as per Table 2.

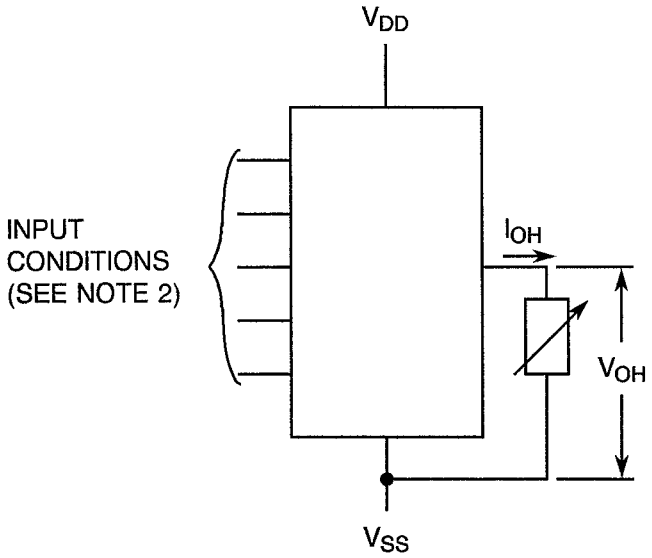
FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(d) - OUTPUT VOLTAGE LOW LEVEL



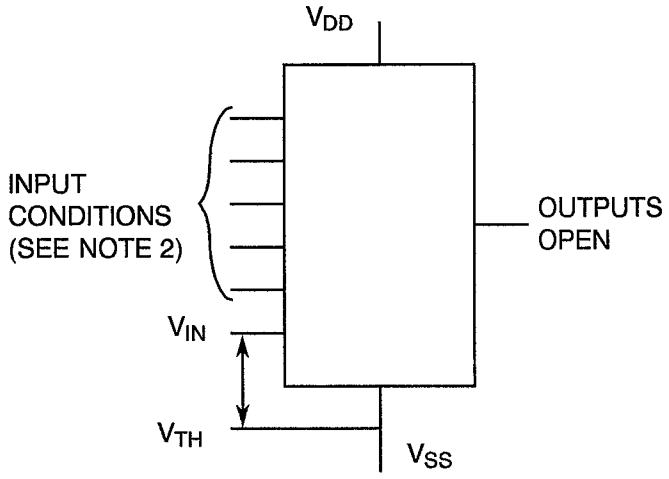
NOTES
1. Each output to be tested separately.
2. Input conditions as per Table 2.

FIGURE 4(e) - OUTPUT VOLTAGE HIGH LEVEL



NOTES
1. Each output to be tested separately.
2. Input conditions as per Table 2.

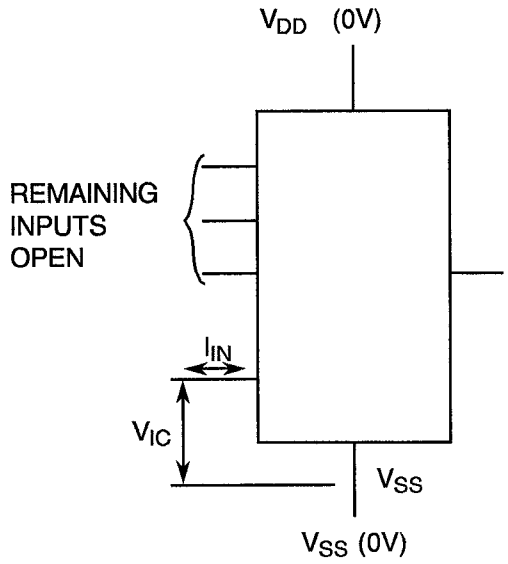
FIGURE 4(f) - THRESHOLD VOLTAGE



NOTES
1. Each input to be tested separately.
2. Input conditions as per Table 2.

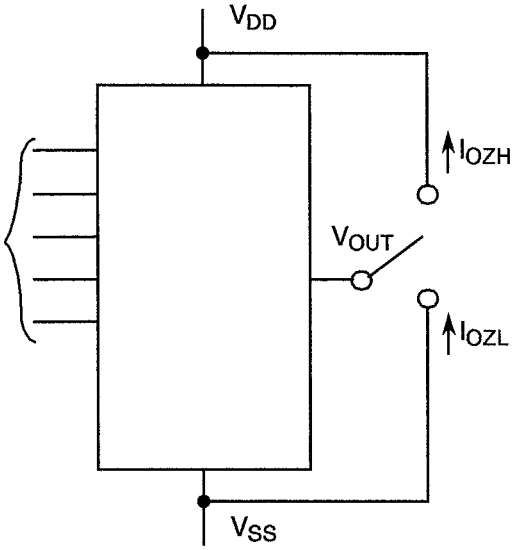
FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(g) - INPUT/OUTPUT CLAMP VOLTAGE



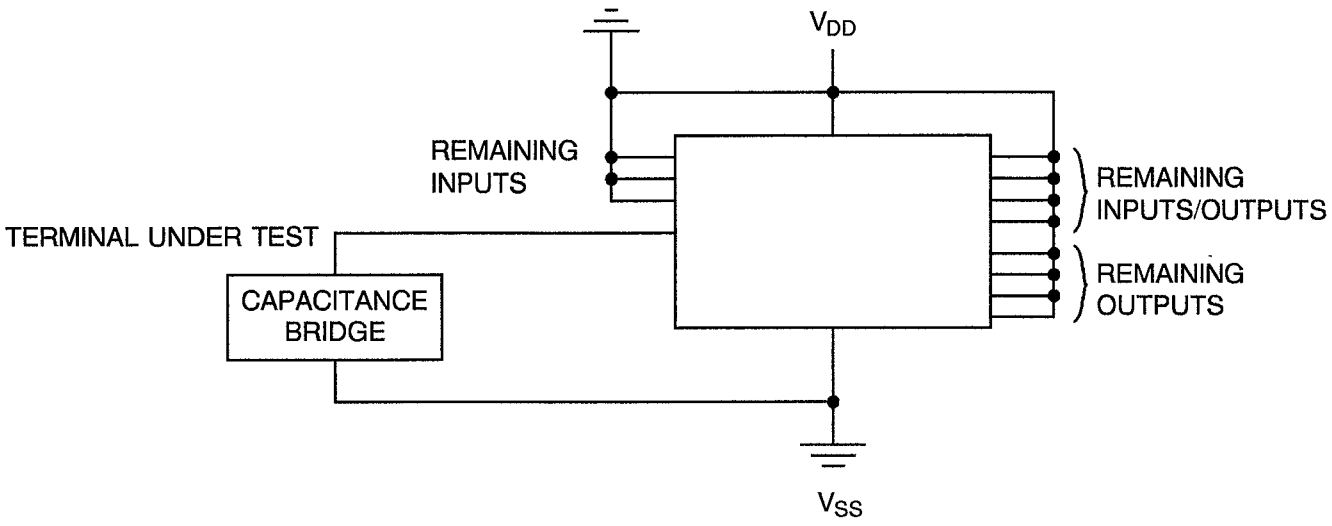
NOTES
1. Each input and output to be tested separately.

FIGURE 4(h) - OUTPUT LEAKAGE CURRENT THIRD STATE



NOTES
1. Each output to be tested separately.
2. Input conditions as per Table 2.

FIGURE 4(i) - INPUT, INPUT/OUTPUT AND OUTPUT CAPACITANCE



NOTES
1. Test frequency = 1.0MHz.
2. Each input, input/output and output is to be tested separately.

TABLE 4 - PARAMETER DRIFT VALUES

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	CHANGE LIMITS (Δ)	UNIT
5	Quiescent Current	I_{DD}	As per Table 2	As per Table 2	±250	µA
6 to 41	Input Current Low Level	I_{IL}	As per Table 2	As per Table 2	±200	nA
42 to 77	Input Current High Level	I_{IH}	As per Table 2	As per Table 2	±200	nA
78 to 110	Output Voltage Low Level 1	V_{OL1}	As per Table 2	As per Table 2	±200	mV
112 to 144	Output Voltage High Level 1	V_{OH1}	As per Table 2	As per Table 2	±300	mV
461 to 477	Output Leakage Current Third State (Low Level Applied)	I_{OZL}	As per Table 2	As per Table 2	±2.0	µA
478 to 494	Output Leakage Current Third State (High Level Applied)	I_{OZH}	As per Table 2	As per Table 2	±2.0	µA

TABLE 5(a) - CONDITIONS FOR HIGH TEMPERATURE REVERSE BIAS BURN-IN

Not applicable.

TABLE 5(b) - CONDITIONS FOR POWER BURN-IN AND OPERATING LIFE TESTS

No.	CHARACTERISTICS	SYMBOL	CONDITION	UNIT
1	Ambient Temperature	T_{amb}	+125 (+0 −5)	°C
2	Outputs - (Pins 26-27-57-58-59-62-63-64-65-68-69-76-77-80-81-82-83)	V_{OUT}	$V_{DD/2}$	V
3	Inputs - (Pins 37-38-52-53)	V_{IN}	V_{SS}	V
4	Inputs - (Pins 28-39-44-45-46-54-71-72)	V_{IN}	V_{DD}	V
5	Input - (Pin 75)	V_{IN}	V_{GEN1}	Vac
6	Input - (Pin 36)	V_{IN}	V_{GEN2}	Vac
7	Input - (Pin 73)	V_{IN}	V_{GEN3}	Vac
8	Inputs - (Pins 2-3-4-5-8-9-10-11-14-15-16-17-20-21-22-23-29-30-31-32-33-34-35)	V_{IN}	V_{GEN4}	Vac
9	Inputs - (Pins 40-41-42-43-47-48-49-50-51-55-56-70-74)	V_{IN}	V_{GEN5}	Vac
10	Pulse Voltage	V_{GEN}	0V to V_{DD}	Vac
11	Timing	t1 t2 t3 t4 t5	4.0 8.0 12 16 4.0	µs µs µs µs ms
12	Pulse Square Wave	GEN1	t1 = low to high transition t2 = high to low transition t4 = period time repeated continuously	-
13	Pulse Square Wave	GEN2	t3 = low to high transition t4 = high to low transition t4 = period time repeated continuously	-
14	Pulse Square Wave	GEN3	t3 = low to high transition t5 = high to low transition and period time repeated continuously	-
15	Pulse Square Wave	GEN4	t1 = high to low transition t2 = low to high transition t4 = period time repeated continuously	-
16	Pulse Square Wave	GEN5	t3 = high to low transition t5 = low to high transition and period time repeated continuously	-
17	Positive Supply Voltage (Pins 1-7-13-19-25-61-67-79)	V_{DD}	5.5 (+0 −0.5)	V
18	Negative Supply Voltage (Pins 6-12-18-24-60-66-78-84)	V_{SS}	0	V

NOTES: See Page 64.

TABLE 5(b) - CONDITIONS FOR POWER BURN-IN AND OPERATING LIFE TESTS (CONT'D)

NOTES

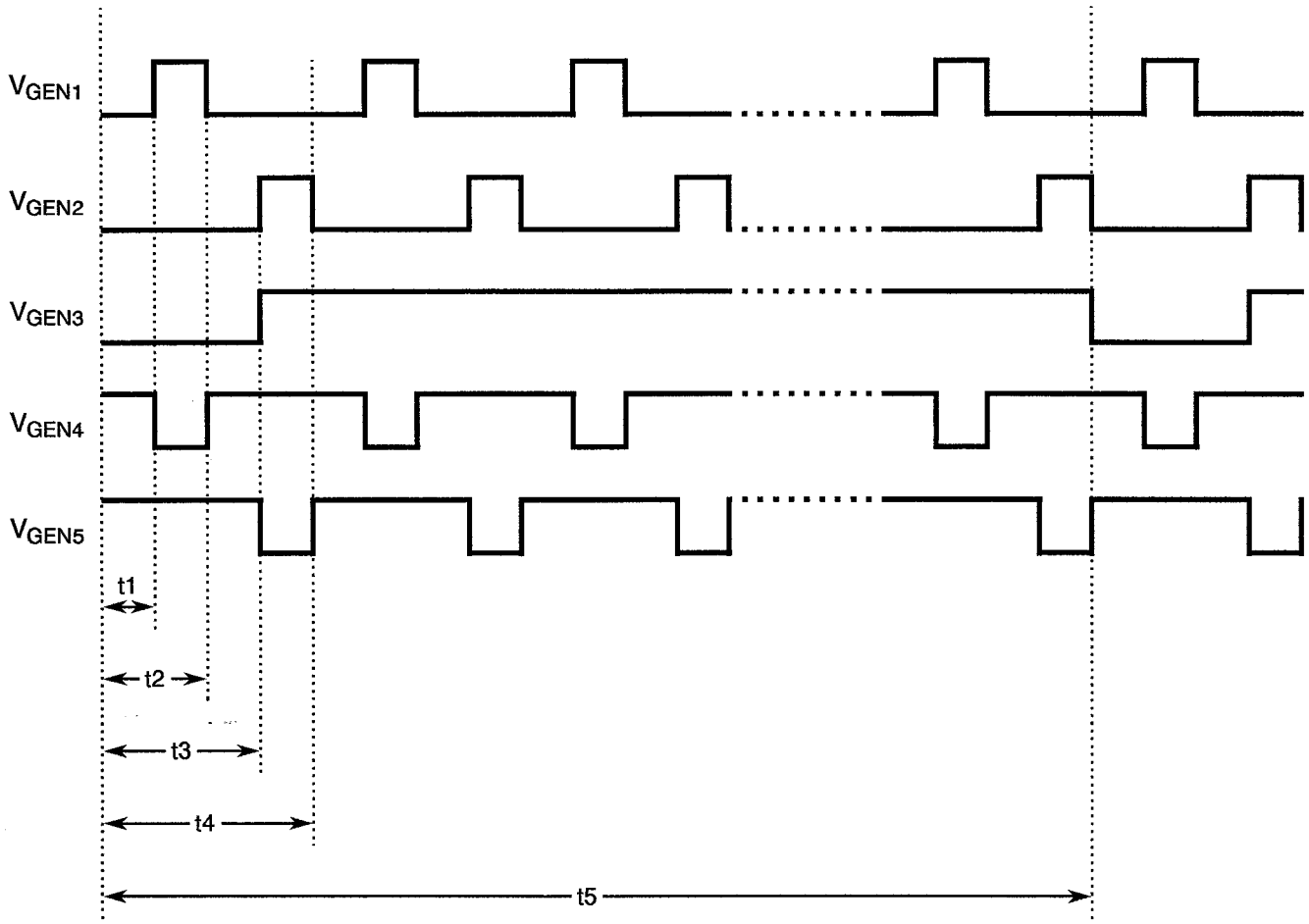
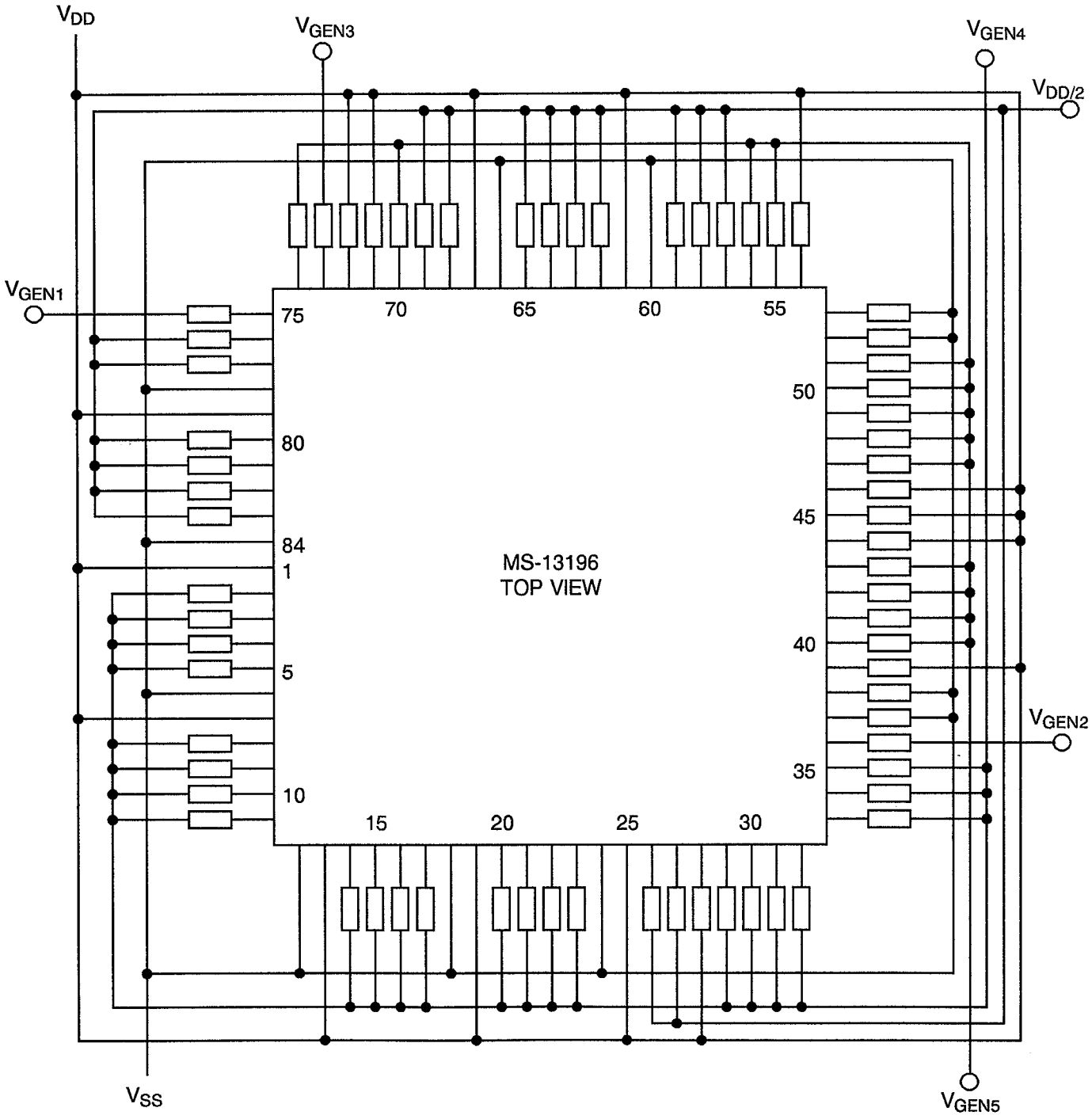


FIGURE 5(a) - ELECTRICAL CIRCUIT FOR HIGH TEMPERATURE REVERSE BIAS BURN-IN

Not applicable.

FIGURE 5(b) - ELECTRICAL CIRCUIT FOR POWER BURN-IN AND OPERATING LIFE TESTS



NOTES

1. Protection resistor for Pin 76 = 56kΩ. Protection/Load resistors for remaining pins = 10kΩ.

4.8 ENVIRONMENTAL AND ENDURANCE TESTS (CHARTS IV AND V OF ESA/SCC GENERIC SPECIFICATION NO. 9000)

4.8.1 Electrical Measurements on Completion of Environmental Tests

The parameters to be measured on completion of environmental tests are scheduled in Table 6. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.8.2 Electrical Measurements at Intermediate Points during Endurance Tests

The parameters to be measured at intermediate points during endurance tests are as scheduled in Table 6 of this specification. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.8.3 Electrical Measurements on Completion of Endurance Tests

The parameters to be measured on completion of endurance testing are as scheduled in Table 6 of this specification. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.8.4 Conditions for Operating Life Tests

The requirements for operating life testing are specified in Section 9 of ESA/SCC Generic Specification No. 9000. The conditions for operating life testing shall be as specified in Table 5(b) of this specification.

4.8.5 Electrical Circuits for Operating Life Tests

Circuits for use in performing the operating life tests are shown in Figure 5(b) of this specification.

4.8.6 Conditions for High Temperature Storage Test

The requirements for the high temperature storage test are specified in ESA/SCC Generic Specification No. 9000. The temperature to be applied shall be the maximum storage temperature specified in Table 1(b) of this specification.

4.9 TOTAL DOSE IRRADIATION TESTING

4.9.1 Application

If specified in Para. 4.2.1 of this specification, total dose irradiation testing shall be performed in accordance with the requirements of ESA/SCC Basic Specification No. 22900.

4.9.2 Bias Conditions

Continuous bias shall be applied during irradiation testing as shown in Figure 6.

4.9.3 Electrical Measurements

The parameters to be measured prior to irradiation exposure are scheduled in Table 2 of this specification. Only devices which meet the requirements of Table 2 shall be scheduled in the test sample.

The parameters to be measured during and on completion of irradiation testing are scheduled in Table 7 of this specification.

TABLE 6 - ELECTRICAL MEASUREMENTS ON COMPLETION OF ENVIRONMENTAL TESTS AND AT INTERMEDIATE POINTS AND ON COMPLETION OF ENDURANCE TESTING

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	LIMITS		UNIT
					MIN.	MAX.	
1	Functional Test 1 (Basic)	-	As per Table 2	As per Table 2	-	-	-
2	Functional Test 2 (Nominal Voltage)	-	As per Table 2	As per Table 2	-	-	-
3	Functional Test 3 (High Voltage)	-	As per Table 2	As per Table 2	-	-	-
4	Functional Test 4 (Low Voltage)	-	As per Table 2	As per Table 2	-	-	-
5	Quiescent Current	I_{DD}	As per Table 2	As per Table 2	-	10	mA
6 to 41	Input Current Low Level	I_{IL}	As per Table 2	As per Table 2	-	−2.0	µA
42 to 77	Input Current High Level	I_{IH}	As per Table 2	As per Table 2	-	2.0	µA
78 to 110	Output Voltage Low Level 1	V_{OL1}	As per Table 2	As per Table 2	-	0.4	V
111	Output Voltage Low Level 2	V_{OL2}	As per Table 2	As per Table 2	-	0.4	V
112 to 144	Output Voltage High Level 1	V_{OH1}	As per Table 2	As per Table 2	3.9	-	V
145 to 177	Output Voltage High Level 2	V_{OH2}	As per Table 2	As per Table 2	4.2	-	V
178	Output Voltage High Level 3	V_{OH3}	As per Table 2	As per Table 2	3.9	-	V
179 to 214	Threshold Voltage Low Level 1 (CMOS Inputs)	V_{THN1}	As per Table 2	As per Table 2	1.3	-	V
215 to 250	Threshold Voltage High Level 1 (CMOS Inputs)	V_{THP1}	As per Table 2	As per Table 2	-	3.2	V
251 to 286	Threshold Voltage Low Level 2 (CMOS Inputs)	V_{THN2}	As per Table 2	As per Table 2	1.7	-	V
287 to 322	Threshold Voltage High Level 2 (CMOS Inputs)	V_{THP2}	As per Table 2	As per Table 2	-	3.9	V

TABLE 6 - ELECTRICAL MEASUREMENTS ON COMPLETION OF ENVIRONMENTAL TESTS AND AT INTERMEDIATE POINTS AND ON COMPLETION OF ENDURANCE TESTING (CONT'D)

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	LIMITS		UNIT
					MIN.	MAX.	
323 to 391	Input/Output Clamp Voltage (to V_{SS})	V_{IC1}	As per Table 2	As per Table 2	-	−2.0	V
392 to 460	Input/Output Clamp Voltage (to V_{DD})	V_{IC2}	As per Table 2	As per Table 2	-	2.0	V
461 to 477	Output Leakage Current Third State (Low Level Applied)	I_{OZL}	As per Table 2	As per Table 2	-	−30	µA
478 to 494	Output Leakage Current Third State (High Level Applied)	I_{OZH}	As per Table 2	As per Table 2	-	30	µA
495	Supply Current	I_{DDS1}	As per Table 2	As per Table 2	-	50	mA
561 to 563	MPROCLK Low to ETALRM Low	TM	As per Table 2	As per Table 2	-	77	ns
564 to 566	DPLL Delay	TDPLL	As per Table 2	As per Table 2	-	65	ns
568 to 570	XTAL1 to XTALCLK Valid	TXX	As per Table 2	As per Table 2	-	26	ns
571 to 573	XTAL1 High to MEANFREQ Valid	TXDPR	As per Table 2	As per Table 2	-	80	ns
574 to 576	XTAL1 High to DPHASE Valid	TXDP	As per Table 2	As per Table 2	-	80	ns
577 to 579	XTAL1 High to WINDOW Valid	TXWD	As per Table 2	As per Table 2	-	102	ns
580 to 582	XTAL1 High to ETALRM High	TXAL	As per Table 2	As per Table 2	-	105	ns
583 to 585	XTAL1 High to TVLD Valid	TXV	As per Table 2	As per Table 2	-	104	ns
586 to 588	XTAL1 High to PFGPHOUT Valid	TXPH	As per Table 2	As per Table 2	-	104	ns
589 to 591	XTAL1 High to PFGWAVE Valid	TXWV	As per Table 2	As per Table 2	-	104	ns

TABLE 6 - ELECTRICAL MEASUREMENTS ON COMPLETION OF ENVIRONMENTAL TESTS AND AT INTERMEDIATE POINTS AND ON COMPLETION OF ENDURANCE TESTING (CONT'D)

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	LIMITS		UNIT
					MIN	MAX	
592 to 594	XTAL1 High to EXTCOUNT Valid	TXXC	As per Table 2	As per Table 2	-	94	ns
595 to 597	XTAL1 High EXTSHTEN Valid	TXSH	As per Table 2	As per Table 2	-	118	ns
598 to 600	XTAL1 High to EXTDATA Valid	TXDT	As per Table 2	As per Table 2	-	118	ns
601 to 603	XTAL1 High to EXTDEMUX Valid	TXDMX	As per Table 2	As per Table 2	-	118	ns
604 to 606	XTAL1 High to EXTCLK Valid	TXXCK	As per Table 2	As per Table 2	-	64	ns
607 to 609	XTAL1 High to EXTETID Low	TXLDF	As per Table 2	As per Table 2	-	81	ns
610 to 612	XTAL1 High to EXTETID High	TXLDR	As per Table 2	As per Table 2	-	111	ns
613 to 615	BUSCLK to MEANFREQ	TBDPR	As per Table 2	As per Table 2	-	42	ns
616 to 618	BUSCLK to DPHASE	TBDP	As per Table 2	As per Table 2	-	42	ns
619 to 621	BUSCLK High to WINDOW Valid	TBWD	As per Table 2	As per Table 2	-	74	ns
622 to 624	BUSCLK High to ETALRM High	TBAL	As per Table 2	As per Table 2	-	75	ns
625 to 627	BUSCLK High to TVLD Valid	TBV	As per Table 2	As per Table 2	-	74	ns
628 to 630	BUSCLK High to PFGPHOUT Valid	TBPH	As per Table 2	As per Table 2	-	74	ns
631 to 633	BUSCLK to EXTCOUNT	TBXC	As per Table 2	As per Table 2	-	62	ns

TABLE 6 - ELECTRICAL MEASUREMENTS ON COMPLETION OF ENVIRONMENTAL TESTS AND AT INTERMEDIATE POINTS AND ON COMPLETION OF ENDURANCE TESTING (CONT'D)

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	LIMITS		UNIT
					MIN	MAX	
634 to 636	BUSCLK Low to EXTSHTEN Valid	TBSH	As per Table 2	As per Table 2	-	87	ns
637 to 639	BUSCLK Low to EXTDATA Valid	TBDT	As per Table 2	As per Table 2	-	87	ns
640 to 642	BUSCLK Low to EXTDEMUX Valid	TBDMX	As per Table 2	As per Table 2	-	87	ns
643 to 645	BUSCLK to EXTCLK	TBXCK	As per Table 2	As per Table 2	-	50	ns
646 to 648	BUSCLK Low to EXTETLD Low	TBLDF	As per Table 2	As per Table 2	-	96	ns
649 to 651	BUSCLK Low to EXTETLD High	TBLDR	As per Table 2	As per Table 2	-	96	ns
652 to 654	DATA Setup to MPROCLK High	t4s	As per Table 2	As per Table 2	6.0	-	ns
655 to 657	DATA Hold to MPROCLK High	t4h	As per Table 2	As per Table 2	3.0	-	ns
658 to 660	AD Setup to MPROCLK High	t6s	As per Table 2	As per Table 2	0	-	ns
661 to 663	AD Hold to MPROCLK High	t6h	As per Table 2	As per Table 2	11	-	ns
664 to 666	$\overline{CS}$ Setup to MPROCLK Low	t1s	As per Table 2	As per Table 2	1.0	-	ns
667 to 669	$\overline{CS}$ Hold to MPROCLK Low	t1h	As per Table 2	As per Table 2	9.0	-	ns
670 to 672	$\overline{RD}$ Setup to MPROCLK Low	t2s	As per Table 2	As per Table 2	2.0	-	ns

TABLE 6 - ELECTRICAL MEASUREMENTS ON COMPLETION OF ENVIRONMENTAL TESTS AND AT INTERMEDIATE POINTS AND ON COMPLETION OF ENDURANCE TESTING (CONT'D)

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	LIMITS		UNIT
					MIN	MAX	
673 to 675	$\overline{RD}$ Hold to MPROCLK Low	t2h	As per Table 2	As per Table 2	8.0	-	ns
676 to 678	$\overline{WR}$ Setup to MPROCLK Low	t3s	As per Table 2	As per Table 2	1.0	-	ns
679 to 681	$\overline{WR}$ Hold to MPROCLK Low	t3h	As per Table 2	As per Table 2	9.0	-	ns
682 to 684	$\overline{CS}$ and $\overline{WR}$ Hold to MPROCLK High	t5s	As per Table 2	As per Table 2	13	-	ns
685 to 687	$\overline{CS}$ and $\overline{WR}$ Hold to MPROCLK High	t5h	As per Table 2	As per Table 2	7.0	-	ns
688 to 690	DATA Enable Delay after MPROCLK Low	t7	As per Table 2	As per Table 2	58	-	ns
691 to 693	DATA Valid after Deassertion of $\overline{RD}$ or $\overline{CS}$	t9	As per Table 2	As per Table 2	59	-	ns
694 to 696	AD Hold after Deassertion of $\overline{RD}$ or $\overline{CS}$	t10	As per Table 2	As per Table 2	19	-	ns
697 to 699	$\overline{RD}$ Setup to MPROCLK High	t11s	As per Table 2	As per Table 2	9.0	-	ns
700 to 702	$\overline{RD}$ Setup to MPROCLK High	t12s	As per Table 2	As per Table 2	9.0	-	ns
703 to 705	$\overline{RD}$ Hold to MPROCLK High	t12h	As per Table 2	As per Table 2	12	-	ns
706 to 708	$\overline{WR}$ Setup to MPROCLK High	t13s	As per Table 2	As per Table 2	9.0	-	ns
709 to 711	$\overline{WR}$ Low Hold to MPROCLK High	t13h	As per Table 2	As per Table 2	3.0	-	ns
712 to 714	$\overline{WR}$ High Hold to MPROCLK High	t15h	As per Table 2	As per Table 2	7.0	-	ns

TABLE 6 - ELECTRICAL MEASUREMENTS ON COMPLETION OF ENVIRONMENTAL TESTS AND AT INTERMEDIATE POINTS AND ON COMPLETION OF ENDURANCE TESTING (CONT'D)

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	LIMITS		UNIT
					MIN	MAX	
715 to 717	DATA Enable Delay After Assertion of $\overline{CS}$	t16	As per Table 2	As per Table 2	-	50	ns
718 to 720	DATA Enable after Deassertion of $\overline{RD}$	t17	As per Table 2	As per Table 2	-	50	ns
721 to 723	DATA Valid after MPROCLK High	t18	As per Table 2	As per Table 2	-	72	ns
724 to 726	DATA Valid after Deassertion of $\overline{RD}$	t19	As per Table 2	As per Table 2	-	59	ns
727 to 729	MPROCLK Low to $\overline{READY}$ Valid	t20	As per Table 2	As per Table 2	-	36	ns
730 to 732	AD Hold after Deassertion of $\overline{RD}$	t22	As per Table 2	As per Table 2	-	19	ns

FIGURE 6 - BIAS CONDITIONS FOR IRRADIATION TESTING

No.	CHARACTERISTICS	SYMBOL	CONDITION	UNIT
1	Ambient Temperature	T_{amb}	+125 (+0−5)	°C
2	Outputs - (Pins 26-27-57-58-59-62-63-64-65-68-69-76-77-80-81-82-83)	V_{OUT}	$V_{DD/2}$	V
3	Inputs - (Pins 37-38-52-53)	V_{IN}	V_{SS}	V
4	Inputs - (Pins 28-39-44-45-46-54-71-72)	V_{IN}	V_{DD}	V
5	Input - (Pin 75)	V_{IN}	V_{GEN1}	Vac
6	Input - (Pin 36)	V_{IN}	V_{GEN2}	Vac
7	Input - (Pin 73)	V_{IN}	V_{GEN3}	Vac
8	Inputs - (Pins 2-3-4-5-8-9-10-11-14-15-16-17-20-21-22-23-29-30-31-32-33-34-35)	V_{IN}	V_{GEN4}	Vac
9	Inputs - (Pins 40-41-42-43-47-48-49-50-51-55-56-70-74)	V_{IN}	V_{GEN5}	Vac
10	Pulse Voltage	V_{GEN}	0V to V_{DD}	Vac
11	Timing	t1 t2 t3 t4 t5	4.0 8.0 12 16 4.0	µs µs µs µs ms
12	Pulse Square Wave	GEN1	t1 = low to high transition t2 = high to low transition t4 = period time repeated continuously	-
13	Pulse Square Wave	GEN2	t3 = low to high transition t4 = high to low transition t4 = period time repeated continuously	-
14	Pulse Square Wave	GEN3	t3 = low to high transition t5 = high to low transition and period time repeated continuously	-
15	Pulse Square Wave	GEN4	t1 = high to low transition t2 = low to high transition t4 = period time repeated continuously	-
16	Pulse Square Wave	GEN5	t3 = high to low transition t5 = low to high transition and period time repeated continuously	-
17	Positive Supply Voltage (Pins 1-7-13-19-25-61-67-79)	V_{DD}	5.5 (+0−0.5)	V
18	Negative Supply Voltage (Pins 6-12-18-24-60-66-78-84)	V_{SS}	0	V

NOTES: See Page 74.

FIGURE 6 - BIAS CONDITIONS FOR IRRADIATION TESTING (CONT'D)

NOTES

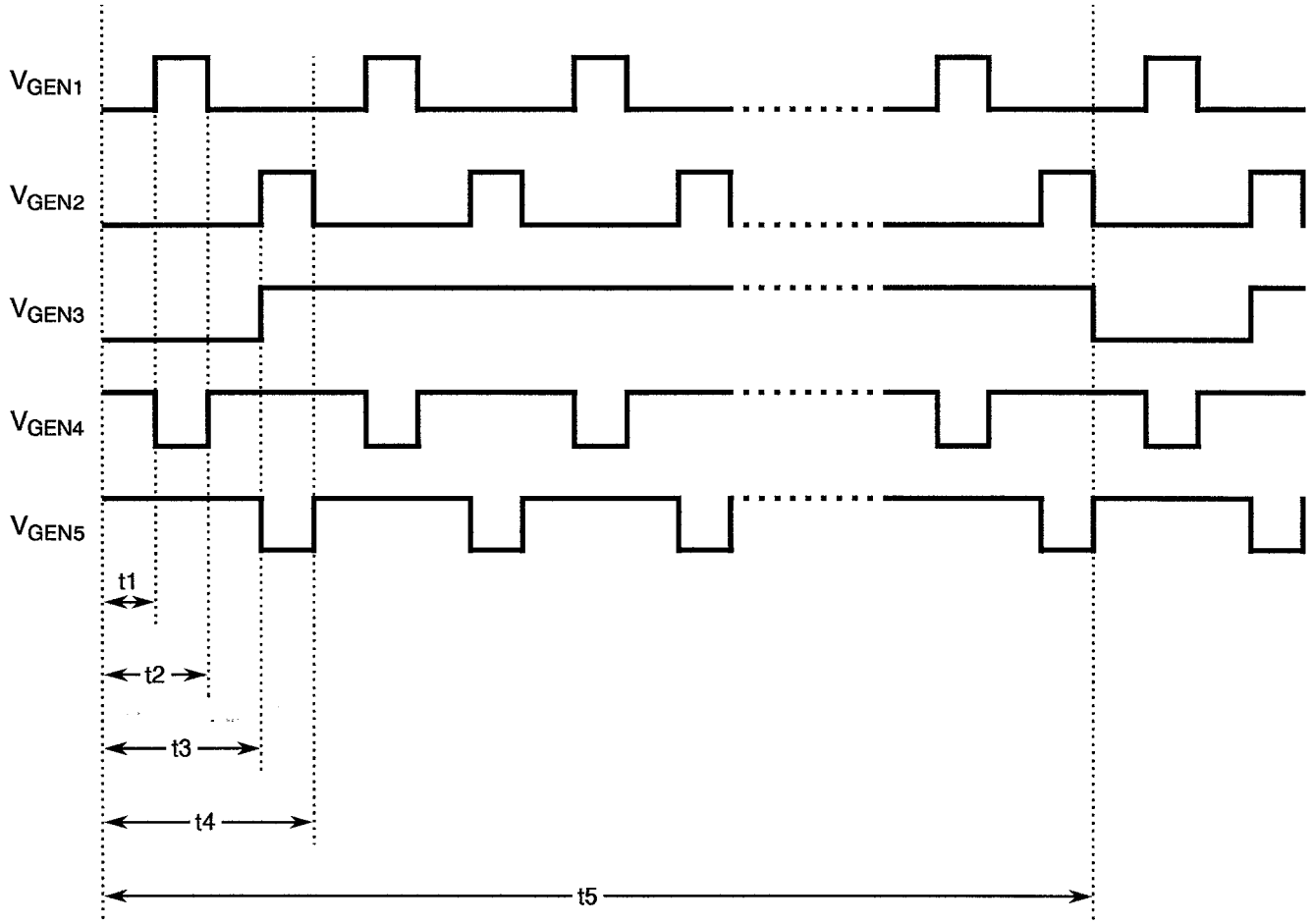
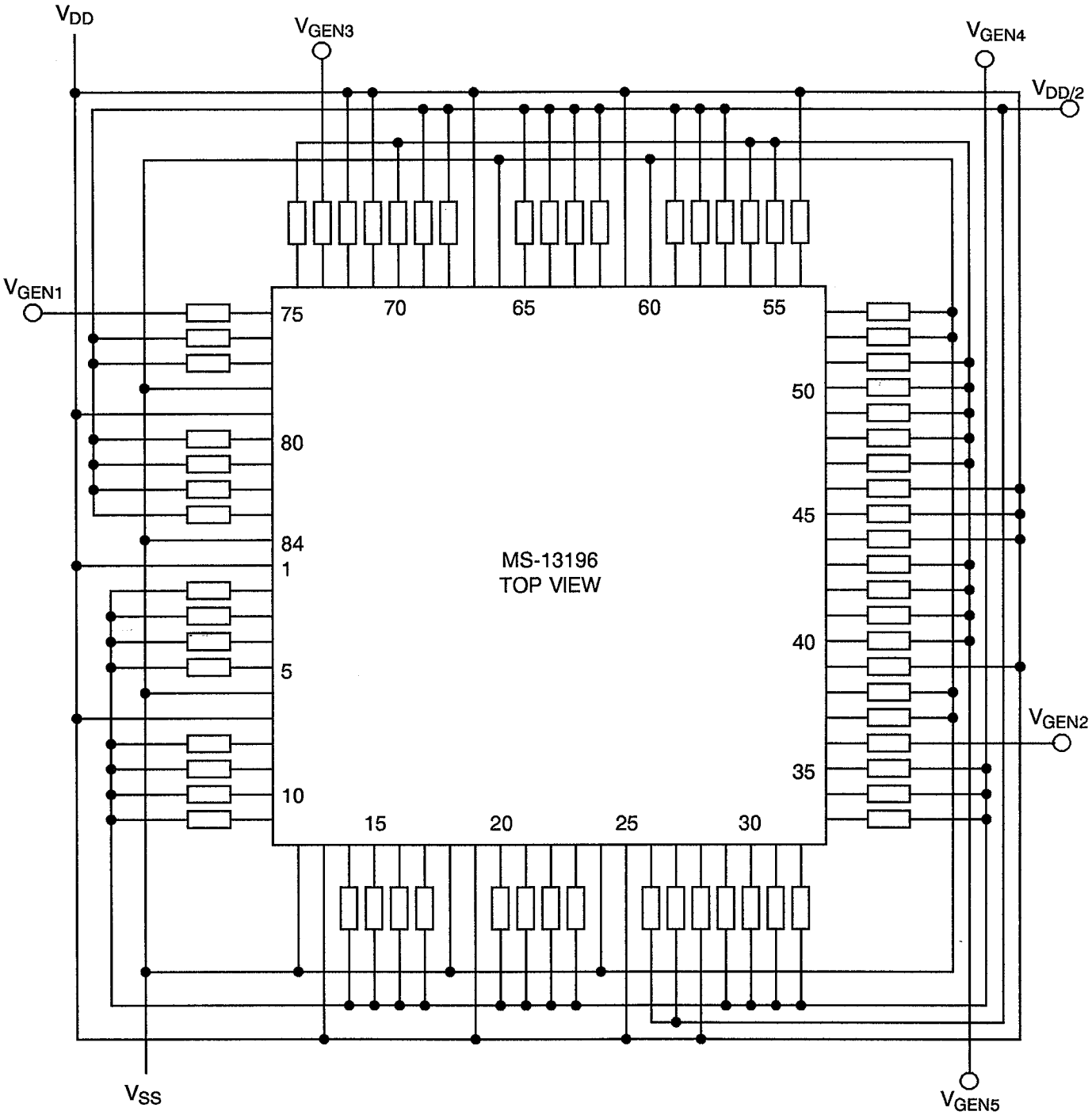


FIGURE 6 - BIAS CONDITIONS FOR IRRADIATION TESTING (CONT'D)



NOTES

1. Protection resistor for Pin 76 = 56kΩ. Protection/Load resistors for remaining pins = 10kΩ.

TABLE 7 - ELECTRICAL MEASUREMENTS DURING AND ON COMPLETION OF IRRADIATION TESTING

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	LIMITS		UNIT
					MIN.	MAX.	
1	Functional Test 1 (Basic)	-	As per Table 2	As per Table 2	-	-	-
2	Functional Test 2 (Nominal Voltage)	-	As per Table 2	As per Table 2	-	-	-
3	Functional Test 3 (High Voltage)	-	As per Table 2	As per Table 2	-	-	-
4	Functional Test 4 (Low Voltage)	-	As per Table 2	As per Table 2	-	-	-
5	Quiescent Current	I_{DD}	As per Table 2	As per Table 2	-	10	mA
6 to 41	Input Current Low Level	I_{IL}	As per Table 2	As per Table 2	-	−10	µA
42 to 77	Input Current High Level	I_{IH}	As per Table 2	As per Table 2	-	10	µA
78 to 110	Output Voltage Low Level 1	V_{OL1}	As per Table 2	As per Table 2	-	0.4	V
111	Output Voltage Low Level 2	V_{OL2}	As per Table 2	As per Table 2	-	0.4	V
112 to 144	Output Voltage High Level 1	V_{OH1}	As per Table 2	As per Table 2	3.9	-	V
145 to 177	Output Voltage High Level 2	V_{OH2}	As per Table 2	As per Table 2	4.2	-	V
178	Output Voltage High Level 3	V_{OH3}	As per Table 2	As per Table 2	3.9	-	V
179 to 214	Threshold Voltage Low Level 1 (CMOS Inputs)	V_{THN1}	As per Table 2	As per Table 2	1.3	-	V
215 to 250	Threshold Voltage High Level 1 (CMOS Inputs)	V_{THP1}	As per Table 2	As per Table 2	-	3.2	V
251 to 286	Threshold Voltage Low Level 2 (CMOS Inputs)	V_{THN2}	As per Table 2	As per Table 2	1.7	-	V
287 to 322	Threshold Voltage High Level 2 (CMOS Inputs)	V_{THP2}	As per Table 2	As per Table 2	-	3.9	V

TABLE 7 - ELECTRICAL MEASUREMENTS DURING AND ON COMPLETION OF IRRADIATION TESTING (CONT'D)

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	LIMITS		UNIT
					MIN.	MAX.	
323 to 391	Input/Output Clamp Voltage (to V_{SS})	V_{IC1}	As per Table 2	As per Table 2	-	−2.0	V
392 to 460	Input/Output Clamp Voltage (to V_{DD})	V_{IC2}	As per Table 2	As per Table 2	-	2.0	V
461 to 477	Output Leakage Current Third State (Low Level Applied)	I_{OZL}	As per Table 2	As per Table 2	-	−100	µA
478 to 494	Output Leakage Current Third State (High Level Applied)	I_{OZH}	As per Table 2	As per Table 2	-	100	µA
495	Supply Current	I_{DDS1}	As per Table 2	As per Table 2	-	50	mA
561 to 563	MPROCLK Low to ETALRM Low	TM	As per Table 2	As per Table 2	-	77	ns
564 to 566	DPLL Delay	TDPLL	As per Table 2	As per Table 2	-	65	ns
568 to 570	XTAL1 to XTALCLK Valid	TXX	As per Table 2	As per Table 2	-	26	ns
571 to 573	XTAL1 High to MEANFREQ Valid	TXDPR	As per Table 2	As per Table 2	-	80	ns
574 to 576	XTAL1 High to DPHASE Valid	TXDP	As per Table 2	As per Table 2	-	80	ns
577 to 579	XTAL1 High to WINDOW Valid	TXWD	As per Table 2	As per Table 2	-	102	ns
580 to 582	XTAL1 High to ETALRM High	TXAL	As per Table 2	As per Table 2	-	105	ns
583 to 585	XTAL1 High to TVLD Valid	TXV	As per Table 2	As per Table 2	-	104	ns
586 to 588	XTAL1 High to PFGPHOUT Valid	TXPH	As per Table 2	As per Table 2	-	104	ns
589 to 591	XTAL1 High to PFGWAVE Valid	TXWV	As per Table 2	As per Table 2	-	104	ns

TABLE 7 - ELECTRICAL MEASUREMENTS DURING AND ON COMPLETION OF IRRADIATION TESTING (CONT'D)

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	LIMITS		UNIT
					MIN	MAX	
592 to 594	XTAL1 High to EXTCOUNT Valid	TXXC	As per Table 2	As per Table 2	-	94	ns
595 to 597	XTAL1 High EXTSHTEN Valid	TXSH	As per Table 2	As per Table 2	-	118	ns
598 to 600	XTAL1 High to EXTDATA Valid	TXDT	As per Table 2	As per Table 2	-	118	ns
601 to 603	XTAL1 High to EXTDEMUX Valid	TXDMX	As per Table 2	As per Table 2	-	118	ns
604 to 606	XTAL1 High to EXTCLK Valid	TXXCK	As per Table 2	As per Table 2	-	64	ns
607 to 609	XTAL1 High to EXTETID Low	TXLDF	As per Table 2	As per Table 2	-	81	ns
610 to 612	XTAL1 High to EXTETID High	TXLDR	As per Table 2	As per Table 2	-	111	ns
613 to 615	BUSCLK to MEANFREQ	TBDPR	As per Table 2	As per Table 2	-	42	ns
616 to 618	BUSCLK to DPHASE	TBDP	As per Table 2	As per Table 2	-	42	ns
619 to 621	BUSCLK High to WINDOW Valid	TBWD	As per Table 2	As per Table 2	-	74	ns
622 to 624	BUSCLK High to ETALRM High	TBAL	As per Table 2	As per Table 2	-	75	ns
625 to 627	BUSCLK High to TVLD Valid	TBV	As per Table 2	As per Table 2	-	74	ns
628 to 630	BUSCLK High to PFGPHOUT Valid	TBPH	As per Table 2	As per Table 2	-	74	ns
631 to 633	BUSCLK to EXTCOUNT	TBXC	As per Table 2	As per Table 2	-	62	ns

TABLE 7 - ELECTRICAL MEASUREMENTS DURING AND ON COMPLETION OF IRRADIATION TESTING (CONT'D)

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	LIMITS		UNIT
					MIN	MAX	
634 to 636	BUSCLK Low to EXTSHTEN Valid	TBSH	As per Table 2	As per Table 2	-	87	ns
637 to 639	BUSCLK Low to EXTDATA Valid	TBDT	As per Table 2	As per Table 2	-	87	ns
640 to 642	BUSCLK Low to EXTDEMUX Valid	TBDMX	As per Table 2	As per Table 2	-	87	ns
643 to 645	BUSCLK to EXTCLK	TBXCK	As per Table 2	As per Table 2	-	50	ns
646 to 648	BUSCLK Low to EXTETLD Low	TBLDF	As per Table 2	As per Table 2	-	96	ns
649 to 651	BUSCLK Low to EXTETLD High	TBLDR	As per Table 2	As per Table 2	-	96	ns
652 to 654	DATA Setup to MPROCLK High	t4s	As per Table 2	As per Table 2	6.0	-	ns
655 to 657	DATA Hold to MPROCLK High	t4h	As per Table 2	As per Table 2	3.0	-	ns
658 to 660	AD Setup to MPROCLK High	t6s	As per Table 2	As per Table 2	0	-	ns
661 to 663	AD Hold to MPROCLK High	t6h	As per Table 2	As per Table 2	11	-	ns
664 to 666	$\overline{CS}$ Setup to MPROCLK Low	t1s	As per Table 2	As per Table 2	1.0	-	ns
667 to 669	$\overline{CS}$ Hold to MPROCLK Low	t1h	As per Table 2	As per Table 2	9.0	-	ns
670 to 672	$\overline{RD}$ Setup to MPROCLK Low	t2s	As per Table 2	As per Table 2	2.0	-	ns

TABLE 7 - ELECTRICAL MEASUREMENTS DURING AND ON COMPLETION OF IRRADIATION TESTING (CONT'D)

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	LIMITS		UNIT
					MIN	MAX	
673 to 675	$\overline{RD}$ Hold to MPROCLK Low	t2h	As per Table 2	As per Table 2	8.0	-	ns
676 to 678	$\overline{WR}$ Setup to MPROCLK Low	t3s	As per Table 2	As per Table 2	1.0	-	ns
679 to 681	$\overline{WR}$ Hold to MPROCLK Low	t3h	As per Table 2	As per Table 2	9.0	-	ns
682 to 684	$\overline{CS}$ and $\overline{WR}$ Hold to MPROCLK High	t5s	As per Table 2	As per Table 2	13	-	ns
685 to 687	$\overline{CS}$ and $\overline{WR}$ Hold to MPROCLK High	t5h	As per Table 2	As per Table 2	7.0	-	ns
688 to 690	DATA Enable Delay after MPROCLK Low	t7	As per Table 2	As per Table 2	58	-	ns
691 to 693	DATA Valid after Deassertion of $\overline{RD}$ or $\overline{CS}$	t9	As per Table 2	As per Table 2	59	-	ns
694 to 696	AD Hold after Deassertion of $\overline{RD}$ or $\overline{CS}$	t10	As per Table 2	As per Table 2	19	-	ns
697 to 699	$\overline{RD}$ Setup to MPROCLK High	t11s	As per Table 2	As per Table 2	9.0	-	ns
700 to 702	$\overline{RD}$ Setup to MPROCLK High	t12s	As per Table 2	As per Table 2	9.0	-	ns
703 to 705	$\overline{RD}$ Hold to MPROCLK High	t12h	As per Table 2	As per Table 2	12	-	ns
706 to 708	$\overline{WR}$ Setup to MPROCLK High	t13s	As per Table 2	As per Table 2	9.0	-	ns
709 to 711	$\overline{WR}$ Low Hold to MPROCLK High	t13h	As per Table 2	As per Table 2	3.0	-	ns
712 to 714	$\overline{WR}$ High Hold to MPROCLK High	t15h	As per Table 2	As per Table 2	7.0	-	ns

TABLE 7 - ELECTRICAL MEASUREMENTS DURING AND ON COMPLETION OF IRRADIATION TESTING (CONT'D)

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	LIMITS		UNIT
					MIN	MAX	
715 to 717	DATA Enable Delay After Assertion of $\overline{CS}$	t16	As per Table 2	As per Table 2	-	50	ns
718 to 720	DATA Enable after Deassertion of $\overline{RD}$	t17	As per Table 2	As per Table 2	-	50	ns
721 to 723	DATA Valid after MPROCLK High	t18	As per Table 2	As per Table 2	-	72	ns
724 to 726	DATA Valid after Deassertion of $\overline{RD}$	t19	As per Table 2	As per Table 2	-	59	ns
727 to 729	MPROCLK Low to $\overline{READY}$ Valid	t20	As per Table 2	As per Table 2	-	36	ns
730 to 732	AD Hold after Deassertion of $\overline{RD}$	t22	As per Table 2	As per Table 2	-	19	ns

APPENDIX 'A'

AGREED DEVIATIONS FOR MITEL (S)

ITEMS AFFECTED	DESCRIPTION OF DEVIATIONS
Para. 4.2.2	Paragraph 4.4 - Marking (plus Serialisation for Level B): May be performed to follow Paragraph 9.3 (Encapsulation). Paragraph 9.1 - Visual Inspection MIL-STD-883C, Method 2010.10, Paragraph 3.1.3: Scribing and die defects, "high magnification": Clauses c and d shall not be applicable for the device. Instead, the following criteria shall be used: - No device shall be acceptable if it exhibits cracks that:- (a) Come closer than 0.25mil to any operating metallisation or other functional circuit element. (b) Exceed 3.0mil in length pointing toward any operating metallisation or other functional circuit element. - For areas which are metallised, MIL-STD-883C, Method 2010.10, Paragraph 3.1.3 d is applicable without exception.
Para. 4.2.3	Paragraph 9.12 - Radiographic Inspection (a) ESA/SCC Basic Specification No. 20990, Paragraph 4.1: Inspection for foreign particles, voids and seal defects only may be performed.
Para's 4.2.4 and 4.2.5	Paragraph 9.18 - Solderability (a) A manually controlled dipping device may be used.