ESCC
European Space Components Coordination

Pages 1 to 28

# REQUIREMENTS FOR THE

# TECHNOLOGY FLOW QUALIFICATION

# OF MONOLITHIC MICROCIRCUITS

# ESCC Basic Specification No. 2549000

**ISSUE 1**

**April 2003**

esa

Document Custodian: European Space Agency - see https://escies.org

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| DCR No. | CHANGE DESCRIPTION |
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## 1. PURPOSE

This specification provides additional information and requirements for the Qualification Approval of Monolithic Microcircuit Technology Flows and Components and their inclusion on the ESCC Qualified Manufacturer's List (QML). It outlines the additional monolithic microcircuit specific requirements for the definition of Technology Flow and its boundaries, the establishment of a Quality Management Programme, the preparation of a Process Capability and Reliability Assessment Programme, an Evaluation Test Programme and Qualification Test Programme, and the performance of an On-site Validation Audit.

This specification shall be read in conjunction with ESCC Basic Specification No. 25400.

This specification does not directly define detailed requirements for a monolithic microcircuit Manufacturer, but instead defines the points which the Manufacturer must address in his Quality Management Programme.

## 2. APPLICABLE DOCUMENTS

The following ESCC Specifications form part of, and shall be read in conjunction with, this specification. The relevant issues shall be those in effect at the date of commencement of the Technology Flow certification.

### 2.1 ESCC SPECIFICATIONS

No. 22900, Total Dose Steady State Irradiation Test Method.

No. 25100, Single Event Effects Test Method and Guidelines.

No. 25400, Requirements for the Technology Flow Qualification of Electronic Components for Space Application.

No. 9000, Integrated Circuits, Monolithic.

No. 9010, Monolithic Microwave Integrated Circuits (MMICs).

### 2.2 OTHER (REFERENCE) DOCUMENTS

| | |
|---|---|
| MIL-STD-883 | Test Methods and Procedures for Micro-electronics. |
| EIA/JESD 57 | Test Procedure for the Management of Single-Event Effects in Semiconductor Devices from Heavy Ion Irradiation. |

## 3. TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

The terms, definitions, abbreviations, symbols and units specified in ESCC Basic Specification No. 21300 shall apply. In addition, the following shall apply:-

Abbreviations

| | |
|---|---|
| MTTF | Mean time to failure. |
| PIPL | Post-irradiation parameter limits. |
| RHA | Radiation hardness assurance (or assured). |
| RHACL | Radiation hardness assurance capability level. |
| TDDB | Time dependant dielectric breakdown. |

Definitions

| | |
|---|---|
| Parametric monitor | A special test structure which is built into and can be used to measure the parameters of processed materials used in component manufacture. |
| Radiation hardness assurance | The portion of product assurance which assures that parts |

continue to perform as specified or degrade in a specified manner when subjected to the specified radiation environment stress.

| | |
|---|---|
| Radiation hardness assurance capability level | The radiation level which the Manufacturer chooses for each radiation environment, appropriate to his technology, as a consistently achievable exposure level that does not cause degradation in the microcircuit beyond the specified level of performance. |
| Radiation hardness assured part | A part to which the Manufacturer has assigned an RHACL. |

## 4. INTRODUCTION

ESCC Technology Flow qualification is the status granted to a Manufacturer's specified Technology Flow after successful completion of an evaluation, certification and qualification programme as defined in ESCC Basic Specification No. 25400, the relevant parts of ESCC Generic Specification No. 9000 and this specification. It is also the status granted to any component type which is both:

- Manufactured using, and within the boundaries defined for, a qualified Technology Flow,
- Defined by, and meets the requirements of, ESCC Generic Specification No. 9000 and the relevant ESCC Detail Specification.

## 5. DEFINITION OF TECHNOLOGY FLOW AND BOUNDARIES

### 5.1 GENERAL

The Manufacturer shall define the Technology Flow for which certification and qualification is sought as required by ESCC Basic Specification No. 25400.

This Technology Flow definition shall also form the basis of a Process Identification Document (PID) to be produced by the Manufacturer which shall fulfil all of the requirements of ESCC Basic Specification No. 21700 in terms of content and configuration control.

This definition has to demonstrate that the Technology Flow and its corresponding boundaries represent a structured, properly controlled and monitored design methodology and manufacturing process for monolithic integrated circuit technologies.

To meet these requirements the definition should, as a minimum, address the areas listed in the following paragraphs at least to the extent detailed therein. The definition should cover all elements of the Technology Flow where a change could affect product performance and would therefore need to be reviewed by the Technology Review Board (TRB) before being introduced. Additional information should be supplied whenever necessitated by the particular nature of the technology under approval. Within the definition of the Technology Flow, seven areas are of particular concern:

- The physical design and procedures which are closely related to the manufacturing process.
- The design system and procedures used to implement the circuit design methodology.
- The fabrication processes.
- The assembly processes.
- The package.
- The test facility.
- Traceability.

These areas are addressed in the subsequent paragraphs.

### 5.2 PHYSICAL DESIGN

The physical design is governed by a set of technology specific rules and parameters, commonly called 'Design Rules'. These rules define the construction and composition of all structures foreseen for the design and manufacture of a monolithic integrated circuit in a specific technology. The description of the physical design requires the definition of at least the following characteristics.

The layout design rule set which specifies the topology of all physical structures, including those for alignment and test purposes in terms of:

- Function (e.g. diffusion, conductor, contact, dielectric, etc.).
- Shape (e.g. aspect ratios, polygon, angles, etc.).
- Size (e.g. minimum/maximum, width/length/depth, etc.).
- Positioning (e.g. overlaps of compound structures, spacing between structures of equal or different nature).
- The vertical dimensions of all layers (e.g. depth of diffusion, trenches, thickness of polysilicon, metallisation, etc.).
- Radiation hardness assurance considerations, if applicable.

The electrical rule and parameter set in terms of:

- Sheet resistivities of layers used for resistors.
- The current carrying capability of conductive layers.
- Sheet and edge capacitances.
- Dielectric breakdown voltages.
- Transistor and diode parameters and associated simulation models.
- Critical distance between components (e.g. coupling etc.)

Other relevant parameters or restrictions not covered in the previous points like suitability to implement analogue/digital circuits or special circuit design techniques.

Gate arrays and similar type integrated circuits exhibiting a partially fixed topology require a complete description of all masters to be included in the Technology Flow which includes the layout of elementary cells, the pad arrangement and a detailed presentation of the power and ground routing.

5.3 DESIGN SYSTEM

The design methodology is defined by the design system and all other procedures applied in the design of an integrated circuit. The design system comprises all software, basic design data and the hardware platform.

Technology Flow Qualification of a design system requires as a minimum:-

(1) The implementation of a configuration control guaranteeing the traceability of all software and data forming part of the system and,

(2) The application of a quality assurance system addressing at least documentation procedures, acceptance testing prior to system release and the organisation of error reporting and corrective action procedures.

Both systems shall be fully documentated and their application has to be evident.

At least the following items shall be covered in the PID

(a) A general description of the design system including block diagrams representing:
- The software structure of the system.
- The design flow, distinguishing between interactive and automatic actions.
- The data flow within the system, with emphasis on the dynamics of the accumulated design data.

(b) A description of the hardware platform (e.g. work stations, memory requirements, LAN, host computers etc.).

(c) The library of fixed cells, including pad cells, shall be described at least in terms of the following relevant details:

- The circuit symbol characterised by its name and input/output connections with signal names and

associated function.

- The logic diagram and truth table supplemented by a state diagram for sequential circuits.
- All relevant electrical and timing parameters including the driving capability and short circuit protection of outputs and the static and dynamic power consumption.
- The detailed circuit schematic including effective transistor sizes.
- The final layout after completion of all postprocessing steps like compaction or shrinking. It shall be presented in the form of a coloured plot on a scale allowing distinction of all structures.

  The development process of the cell library shall be described in terms of geometrical, functional, electrical and timing checks performed for verification.

(d) Software and associated data shall be described in terms of:

- The origin and version of the programme.
- A comprehensive description of its functional scope.
- The programming language and the amount of code.
- The memory requirement.
- Definition of data formats and description languages.
- Definition of programme interfaces.
- A description of the human interface with admitted or required interactivity and output format.
- All software serving simulation type purposes requires a detailed description of the underlying models and their parametric capability.
- Parametrisable, flexible circuits which are based on a dedicated library of subcells different from the library of fixed cells addressed earlier, shall be defined in terms of all characteristics listed in this paragraph.

(e) A description of the configuration control system.

(f) A description of the quality assurance system.

For custom and semi-custom devices, where a design group external to the Manufacturer might be active in component design, the Manufacturer shall be responsible for ensuring that all design activities are completely within the boundaries defined for the qualified Technology Flow. To achieve this, the Manufacturer should produce a suitable Design Compliance Matrix (checklist) which will form part of the Technology Flow Description. For components with an external design input, the Design Compliance Matrix should be jointly completed by the Manufacturer and Designer and should then be formally approved by the Manufacturer as a basis for later issuing Certificates of Conformity for the components.

5.4 FABRICATION PROCESSES

The fabrication processes to be covered by the description should include, but not be limited to, the following areas:

- Fabrication process sequence and limits.
- Fabrication process materials and material specifications, including epitaxial layer thickness.

  Quality control of incoming materials.
- Traceability and control of stored materials, especially limited shelf life items.
- Photoresistive materials and material specifications.
- Doping material source, concentration and process technique.
- Cross section diffusion profile.
- Passivation or glassivation material, thickness and technique.
- Metallisation system (pattern, material, deposition and etching technique, line width and thickness).

- Conductor, resistor and dielectric materials.
- Physical location of wafer fabrication line.
- Passivation and glassivation process temperature and time.
- Oxidation process, oxide composition and thickness, oxidation temperature and time.
- Sintering and annealing temperature and time.
- Standard Evaluation Circuit (SEC) and how it is tested.
- Method of mask generation and identification.
- Parametric monitor and how it is tested.
- Wafer acceptance criteria.
- Technology Characterisation Vehicle (TCV) and how it is tested.
- Sample plans (quantity and acceptance numbers).
- Gate formation process, material and technique.
- Backside process including wafer thinning and backside metallisation.
- Ohmic contact formation.
- Starting material qualification (e.g. silicon boule).
- Lot formation.
- Probing.
- Cleanroom conditions.
- Wafer handling and storage conditions.

5.5 ASSEMBLY PROCESSES

The assembly processes to be covered by the description should include, but not be limited to, the following areas:

- Die attach material, method and location.
- Wire/ribbon bond interconnect method.
- Seal technique (materials, sealing process and gas composition).
- Selection and specification of assembly materials.
- Quality control of incoming materials.
- Traceability and control of stored materials, especially limited shelf life items.
- Implementation procedure for internal visual and other test methods.
- Assembly flow.
- Physical location of assembly operation.
- Scribing and die separation method (dicing of wafers).
- Die size.
- Periodic test and inspection procedures.
- Screening tests.
- Sample plans (quantity and acceptance numbers).
- Die back surface preparation.
- Bond pad geometry, spacing and metallisation.

- Moulding material and method.
- Die encapsulation/coating material and technique.
- Internal water vapour control programme.
- Device marking process.
- Lot formation.

5.6 PACKAGE

The package characteristics to be covered by the description should include, but not be limited to, the following areas:

- Vendor.
- Specification.
- Lot size.
- Incoming inspection.
- External dimensions.
- Cavity dimensions.
- Number of leads or terminals.
- Lead or terminal dimensions.
- Lead or terminal base material.
- Lead or terminal plating material.
- Body material.
- Body plating material.
- Body plating thickness.
- Die pad material.
- Die pad plating.
- Die pad plating thickness.
- Lid material.
- Lid plating materials.
- Lid plating thickness.
- Lid seal (preform) material.
- Lid glass seal material.
- Lid glass seal thickness.
- Lead glass seal material.
- Lead glass seal thickness.
- Leads or terminals spacing.
- Lead configuration.
- Maximum allowable die size.
- Device marking process.
- Lead attachment.

5.7 TEST FACILITY

The test facility characteristics to be covered by the description should include, but not be limited to, the following areas:

- Implementation procedures for external visual or other test methods.
- Testing flow.
- Physical location of test facility.
- Sample plans (quantity and acceptance numbers).
- Test procedures (including test vector generation).
- Lot formation.

The Manufacturer shall describe inspection and test methods giving references to the documents specifying the methods. The following areas shall be covered as a minimum:

- Incoming inspection.
- In-process inspection.
- Wafer acceptance testing.
- Precap inspection (if applicable).
- Screening and associated electrical tests.
- Qualification testing.
- Lot Acceptance or Periodic Testing or Conformance Inspection.

5.8 TRACEABILITY

A traceability system must be defined which includes the maintenance of records which allow traceability from the device serial number to a specific wafer lot, or to a specific wafer for parts where any testing (e.g. irradiation testing) is performed on a wafer by wafer basis. Equivalent traceability must also exist for any test structures which are used.

At least the following points shall be addressed by such a traceability system:

- The use of purchase orders and specifications.
- The use of route sheets and travellers.
- The traceability of test structures.

## 6. QUALITY MANAGEMENT PROGRAMME

The following requirements, which are additional to the general requirements given in Section 6 of ESCC Basic Specification No. 25400, should be addressed in the Quality Management Programme for monolithic microcircuit technologies:-

(a) **Conversion of Customer Requirements**

Mask generation procedure within the controlled design procedures of the previous point.

Baselined wafer fabrication and assembly capabilities.

(b) **Listing of Major Tests**

Listing of major tests for which the ESCC Executive may request data to be submitted, including, where appropriate:

- Wafer (lot) acceptance.
- SEM or non-destructive SEM.
- Internal visual.

- Particle impact noise detection.
- Fine and gross leak.
- Radiographic inspection.
- Radiation testing.
- Preconditioning.
- Temperature/humidity testing.
- Temperature cycle.
- Burn-in.
- Life tests.

(c) Electrostatic discharge sensitivity programme

## 7. PARAMETRIC MONITORS, TECHNOLOGY CHARACTERISATION VEHICLES AND STANDARD EVALUATION CIRCUITS

### 7.1 PARAMETRIC MONITORS

The Manufacturer should have parametric monitor test structures to be used for measuring electrical characteristics of each wafer type in a specified technology. The parametric monitor test structures can be incorporated into the grid, within a device die, as a dedicated drop-in die or any combination thereof. Location of the parametric monitor test structures should be optimally positioned to allow for the determination of uniformity across the wafer.

The Manufacturer should establish and document reject limits and procedures for parametric measurements including which parameters will be routinely monitored and which will be included in the SPC programme. Documentation of the parametric monitor should also include parametric monitor test structure design and test procedure, including electrical measurements at temperature, if any and the relationship between the measured limits and those determined in the Manufacturer's circuit simulations, design and process rules. Alternative measurement techniques, such as in-line monitors are acceptable if properly documented. The following parameters are intended as a guideline to be used by the Manufacturer's TRB in formulating suitable parametric monitors:-

#### 7.1.1 General Electrical Parameters

7.1.1.1 Sheet resistance

Structures should be included to measure the sheet resistance of all conducting layers.

7.1.1.2 Junction breakdown

Structures should be included to measure junction breakdown voltages for all diffusions.

7.1.1.3 Contact resistance

Structures should be included to measure contact resistance of all inter-level contacts.

7.1.1.4 Ionic contamination and minority carrier lifetime

Structures should be included to measure ionic contamination, such as sodium, in the gate, field and inter-metal dielectrics and to measure minority carrier lifetime.

#### 7.1.2 MOS Parameters

7.1.2.1 Gate oxide thickness

Structures should be included to measure gate oxide thickness for both n and p gate oxides as applicable.

7.1.2.2 MOS transistor parameters

A minimum set of test transistors should be included for the measurement of transistor parameters. The minimum transistor set should include a large geometry transistor of sufficient size that short channel and narrow width effects are negligible and transistors that can separately demonstrate the maximum short channel effects and narrow width effects allowed by the geometric design rules. Both "N" and "P" transistors should be included for a CMOS technology. If there is more than one nominal threshold voltage for either the "N" or "P" transistor type the minimum set should be included for each threshold. The transistor parameters to be measured are given below:

- Threshold voltage. The linear threshold voltage ($V_T$) for each transistor in the minium set of transistors should be measured.
- Linear transconductance. The linear transconductance ($g_m$) for a full minimum set of transistors should be measured.
- Effective channel length. The effective channel length for the minimum channel length of each transistor type should be measured.
- $I_{ON}$. $I_{ON}$ shall be measured for representative transistors in the set.
- $I_{OFF}$. $I_{OFF}$ shall be measured for representative transistors in the set.
- Propagation delay. A test structure shall be available in the form of a functional circuit from which propagation delay information can be measured at room temperature.
- Field leakage. Field transistor leakage for the minimum spaced adjacent transistors at the maximum allowed voltage should be measured.

7.1.3 Bipolar Parameters

Note that care must be taken in the manner and sequence in which breakdown voltage and current measurements are taken so as to not permanently alter the device for other measurements.

7.1.3.1 Sheet resistance

Structures should be included which can be used to measure sheet resistance of all doped regions (e.g. emitter, buried collector).

7.1.3.2 Schottky diode parameters

The following measurements should be made on Schottky diodes representative of the size used in the technology:

- Reverse Leakage. The reverse leakage current ($I_R$) should be measured at a specified reverse voltage.
- Reverse Breakdown. The reverse breakdown voltage ($V_{BR}$) should be measured at a specified current.
- Forward Voltage. The forward voltage ($V_F$) should be measured at a specified current.

7.1.3.3 Bipolar transistor parameters

The following measurements should be made on bipolar transistors representative of the size and type used in the technology. The types should include NPN, Schottky clamped NPN, vertical PNP, substrate PNP and lateral PNP as applicable:

- Transistor gain. The common emitter current DC gain, ($h_{FE}$), should be measured on representative transistors at three decades of collector current, the centre of which is at the rated current of the device.
- Leakage currents. The leakage currents ($I_{CEO}$, $I_{CBO}$ and $I_{EBO}$) should be measured on representative transistors at a specified voltage.
- Breakdown voltages. The breakdown voltages ($V_{(BR)EBO}$, $V_{(BR)CBO}$ and $V_{(BR)CEO}$) should be measured on representative transistors at the specified currents.
- Forward voltages. The forward voltages ($V_{BEO}$ and $V_{BCO}$) should be measured on

representative transistors at the rated currents.

- Propagation delay. A test structure should be available in the form of a functional circuit from which propagation delay information can be measured at room temperature.

7.1.3.4 Isolation leakage

The isolation leakage current ($I_L$) between minimum spaced adjacent transistor collectors should be measured at a specified voltage.

7.1.4 Fast-test Reliability Structures

Fast-test reliability structures are structures meant to evaluate, within a few seconds of testing, a particular known reliability failure mechanism to ensure that the processing which an individual wafer received is consistent with the reliability goals of the technology. When fast-tests are used, documentation should be available which shows the correlation between them and the results of more traditional accelerated ageing tests performed on the TCV.

7.2 TCV PROGRAMME

A TCV programme should be implementated by the Manufacturer for the technology or process being considered for certification. The programme should contain, as a minimum, those test structures needed to characterise a technology's susceptibility to intrinsic reliablity failure mechanisms such as electromigration, time dependent dielectric breakdown, gate sinking, ohmic contact degradation, sidegating/backgating and hot carrier ageing. If other wear-out mechanisms are discovered as integrated circuit technology continues to mature, test structures for the new wear-out mechanisms should be added to the TCV programme.

The TCV test structures do not have to be a single die or location, but can appear on the parametric monitor, the SEC or the device itself. The TCV programme should, however, indicate where the structures are located and how they are tested and analysed.

All of the TCV test structures must be packaged using the same materials and assembly procedures as standard circuits in the technology. If for any reason this is not possible, the TCV should be packaged in a suitable package to allow for the evaluation of the die technology without adversely affecting the outcome of the test. The TCV structures need not use a fully qualified package as these will tend to have lead counts far in excess of those needed for intrinsic reliability studies. The packaging requirements for the TCV may be waived by the ESCC Executive if the Manufacturer can supply documentation showing the equivalence of wafer level and packaged accelerated ageing results.

Generally TCV test structures shall be provided to verify all relevant material, process and device parameters such as:

- Interface properties.
- Crystalline defects in the semiconductor material.
- Sheet resistance for each non-dielectric layers (e.g. diffused or implanted regions, polysilicon metal or other).
- Contact resistance.
- Dielectric isolation (breakdown voltage).
- Transistor and diode parameters.
- Carrier mobilities.
- Minimum line width.
- Interface state densities.
- Doping profiles.
- Leakage currents.
- Wire bonding.

- Die bonding.
- Junction and metallisation alignment.

In addition, the minimum requirements to be addressed for the TCV test structures for specific mechanisms are given as follows.

7.2.1 Hot Carrier Ageing

The TCV should use structures that monitor hot carrier ageing applicable to the technology to be used in ESCC QML microcircuits. Device degradation is to be characterised in terms of both linear transconductance ($g_m$) and threshold voltage ($V_T$) and the resistance to hot carrier ageing is to be based on whichever parameter experiences the Manufacturer's specified degradation limit for the minimum channel length and width allowed in the technology. A wafer level fast-test screen should be established for technologies that are susceptible to hot carrier ageing and this test should then be part of the wafer acceptance criteria.

7.2.1.1 MOS

The TCV should have structures to characterise the effects of hot carrier ageing as a function of channel length for MOS transistors for each of the nominal threshold voltages used in the technology. Degradation should be characterisable in terms of $g_m$ and $V_T$.

7.2.1.2 Bipolar

The TCV should contain structures for characterising hot carrier ageing of diodes in bipolar technologies.

7.2.2 Electromigration

The TCV should contain structures for the worst case characterisation of metal electromigration over:

- Flat surfaces.
- Worst case non-contact topography.
- Through contacts between conductive layers.
- Contacts to substrate.

The current density and temperature acceleration factors for electromigration should be determined and an MTTF and failure distribution determined for the worst case current, temperature and layout geometry allowed in the technology. From the MTTF and failure distribution, a failure rate for electromigration in the technology should be calculated.

7.2.3 Time Dependent Dielectric Breakdown (MOS)

The TCV should contain structures for characterising TDDB of gate oxides. The structures should have gate oxide area and perimeter dominated structures. Separate perimeter structures should be used for the gate ending on a source or drain boundary and where the gate terminates over the transistor to transistor isolation oxide. The electric field and temperture acceleration factors for TDDB should be determined and an MTTF and failure distribution determined for the worst case voltage conditions and thinnest gate oxide allowed in the technology. From the MTTF, a failure rate for TDDB in the technology should be calculated.

7.2.4 TCV Fast-test Structure Requirements

The structures to be used for the fast-test reliability monitoring of hot electron ageing should be included in the TCV programme so that correlation of the fast-test measurements with the accelerated ageing results may be made. It is also recommended that the fast-test intrinsic reliability structures for electromigration and TDDB are included in the TCV programme so that correlation can be made with longer term ageing experiments.

7.2.5 Ohmic Contact Degradation

The TCV should have a structure for assessing the degradation of ohmic contacts with time at temperature.

7.3 SEC PROGRAMME

The Manufacturer should have an SEC for the technology or process being considered for certification. A Manufacturer's SEC should be used to demonstrate fabrication process reliability for the technology. The SEC design documentation should address the:

- Design methodology.
- Software tools used in the design.
- Functions it is to perform.
- Size in terms of utilised transistor or gate count.
- Simulations of its performance.

Documentation procedures for the SEC and standard production devices should be the same so that correlation can be made. The SEC may be designed soley for its role as a quality and reliability monitoring vehicle or it may be a product intended for system use.

The SEC should address the following requirements:-

(a) **Complexity**

The complexity of the SEC for digital microcircuits should be such as to contain, as a minimum, one half the number of transistors expected to be used in the largest microcircuits to be built on the ESCC QML line. For analogue microcircuits the SEC should exercise the functionality of the process Technology Flow, be of a representative complexity and be comprised of major circuit element types.

(b) **Functionality**

The SEC should contain fully functional circuits capable of being tested and screened in a manner identical to the ESCC QML microcircuits.

(c) **Design**

The SEC should be designed to stress the design capabilities of the process. The architecture of the SEC should be designed so that failures can be easily diagnosed.

(d) **Fabrication**

The SEC should be processed on a wafer fabrication line which is intended to be, or already is, a certified ESCC QML line.

(e) **Packaging**

The SEC should be packaged in a package qualified in accordance with the requirements of the ESCC System.

Note that a different SEC might be required whenever the design rules, the materials, the basic processes or the basic functionality of the technology differ.

## 8. PROCESS CAPABILITY AND RELIABILITY ASSESSMENT PLAN AND EVALUATION TEST PLAN

8.1 GENERAL

As part of evaluation the Manufacturer shall build devices and special test structures, perform tests and analyses and run software benchmarks. These actions shall be designed to demonstrate, together with any existing information, the capabilities of the total manufacturing process with regard to quality, reliability and producibility and its suitablity for producing space level components. The necessary activities shall be described in either a process capability and reliability assessment plan and/or an evaluation test plan which should cover all design, fabrication, assembly, test and control processes which comprise the total manufacturing process.

As a minimum the plans must generate sufficient information to allow for a process capability demonstration covering:-

(a) Design

Circuit and package.

(b) Wafer fabrication.

(c) SPC and in-process monitoring programmes including parametric monitors and the TCV and SEC programmes.

(d) Wafer acceptance.

(e) Assembly and packaging.

(f) Radiation hardness assurance, if applicable (see Section 11).

8.2 DESIGN

In the plan(s), the Manufacturer should address the methodology for the following areas of design, (this is also applicable if a third party design centre is used). The design procedure and tools should be controlled in such a manner that the ensueing microcircuit design performs only with limits that have been shown to be reliable for the technology being used, within the constraints of established design rules (electric, geometric and reliability).

8.2.1 Circuit Design

The plan(s) should address the information needed in the following areas of circuit design requirements and performance characteristics.

8.2.1.1 Model verification

It must be demonstrated that all models utilised in the design process are functional, predictable and accurate over the worst case temperature and electrical extremes. Examples of these models are : transistor behavioural, logic, fault, timing, simulation, fabrication, assembly and package.

8.2.1.2 Layout verification

It must be demonstrated that the automated or manual procedures routinely used for design, electrical and reliability rule checking are capable of catching all known errors singly and combinationally. These rules cover, as a minimum:

(a) **Design Rules Check** : Geometric and physical.

(b) **Electrical Rules Check** : Shorts, opens and connectivity.

(c) **Reliability Rules**

Electromigration and current density, $I_R$ drops, latch-up, SEU, hot electrons, ESD and burnout backgating.

8.2.1.3 Performance verification

The Manufacturer should design and construct a die or set of dice to assess process capability to perform routing and to accurately predict post-routing performance. The Manufacturer should demonstrate that the actual measured performance for each function over temperature and voltage falls between the two worst case CAD simulation performance limits. All critical minimum geometric and electrical design rules should be stressed via devices or structures located on the SEC, TCV and/or parametric monitors. The electrical stress requirements for the transistor and interconnects on these structures should be worst case conditions. Failure analysis should be conducted to identify all failure mechanisms occuring in the failed devices and structures and actions should be taken to correct any problems found.

8.2.1.4 Testability and fault coverage verification

If applicable for his product the Manufacturer should demonstrate a design style and a design-for-test methodology which, in conjunction with demonstrated CAD for test tools, can provide 99% or greater fault coverage on a design of reasonable complexity. The Manufacturer should demonstrate the fault coverage measurement (fault simulation, test algorithm analysis, etc.)

capability which is used to provide fault coverage statistics of the design that uses the demonstrated design style, design-for-test method and CAD for test tools. Measurement of fault coverage should be in accordance with the procedures defined in MIL-STD-883, Test Method 5012 or any equivalent test method. For non-digital circuits, the fault coverage requirement might not be applicable, but should be supplemented, as measures of analogue fault coverage become better defined. For microcircuits with both analogue and digital functions this requirement applies fully to the digital part of the microcircuit.

8.2.2 Package Design and Characterisation

The plan(s) should address the information needed in the following areas of circuit design requirements and performance characteristics. Characterisation of the package can be performed by the microcircuit Manufacturer, by an external test house or by the package supplier. The Manufacturer is responsible for maintaining documented validation of all characterisation methods used, including all supporting data.

8.2.2.1 Thermal characterisation

The thermal resistance should be determined for all packages used in the manufacture of ESCC QML components. This value may be obtained by direct or indirect measurements, or by simulation tools or calculations. MIL-STD-883, Test Method 1012 or any equivalent test method may be used for this calculation. If the thermal resistance is obtained by a calculation or simulation tool, this procedure should be certified. To certify such a method of theoretical estimation, the Manufacturer must demonstrate a correlation between the theoretically estimated value and the actual measured value for at least one package of the same style with equal or greater pin count.

8.2.2.2 Electrical characterisation

The following electrical characterisation parameters should be addressed:-

(a) **Ground and Power Supply Impedance**

Packages used in the manufacture of ESCC QML microcircuits should be minimal contributors to ground and power supply noise. The requirement can be covered either through the use of documented package design rules or through testing of the packages, either individually or by similarity, in accordance with MIL-STD-883, Test Method 3019 or any equivalent test method.

(b) **Cross-coupling Effects**

Cross-coupling of wideband digital signals and noise between pins in packages used for digital ESCC QML circuits should be minimised. This requirement can be covered either through the use of documented package design rules or through testing the packages, either individually or by similarity, in accordance with MIL-STD-883, Test Method 3017 or 3018 or any equivalent test method.

(c) **High Voltage Effects**

The voltage applied to an ESCC QML package should not produce a surface or bulk leakage between adjacent package conductors (including leads or terminals). This requirement can be covered either through the use of documented high voltage package design rules aimed at minimising bulk or surface leakage, or through testing of the high voltage packages, either individually or by similarity, in accordance with MIL-STD-883, Test Method 3013 or any equivalent method.

8.3 MASK AND WAFER FABRICATION

The mask fabrication facility should be controlled such that an error free mask is produced from the microcircuit design database. This should include monitoring, controlling and reducing defect density.

The Manufacturer should identify a specific technology of technologies for the wafer fabrication. A technology consists of the fabrication sequence, design rules and electrical characteristics. The wafer fabrication process should then be controlled with the following:-

(a) In-line statistical control.

(b) A parametric monitor structure for measuring electrical parameters.

(c) A TCV structure to study intrinsic reliability mechanisms.

(d) An SEC to monitor the fabrication process and serve as a surrogate microcircuit for reliability testing.

Demonstration of wafer fabrication capability is covered in more detail in the following sections.

8.4 SPC AND IN-PROCESS MONITORING PROGRAMME

The Manufacturer should have an in-process monitoring system to control key processing steps to ensure device yield, reliability and radiation hardness assurance, if applicable.

The critical operations to be monitored should be determined by the Manufacturer based on his experience and knowledge of his processes. The resulting data should be analysed by appropriate SPC methods, in accordance with the requirements of EIA-557-A or an equivalent document, to determine control effectiveness.

The following should, as a minimum, be addressed for the wafer fabrication process by the Manufacturer:

- Incoming mask and fabrication process materials.
- Equipment used for wafer fabrication.
- Doping material concentration.
- Cross section diffusion or concentration profile and epitaxial layer.
- Passivation or glassivation.
- Metallisation deposition.
- Photolithography and resultant line width.
- Passivation process temperature and time.
- Diffusion, implant anneal process temperature and time, or both.
- Sintering or annealing temperature and time.
- All reliability test data including the SEC.
- Mask inspection and defect density data.
- Parametric monitor test data.
- Wafer acceptance data.
- TCV.
- Photoresistive processing, including rework procedures.
- Ion implant.
- Wafer backside preparation.
- Wafer probe acceptance criteria.
- Rework.
- Oxide process.
- Gate formation.
- Via hole process.

8.4.1 TCV Testing

As part of evaluation, as a minimum, the quantity of TCV test structures for each wear-out mechanism,

as specified in the Process Capability and Reliability Assessment Programme or the Evaluation Test Programme, should be subjected to accelerated ageing tests. The TCV test structures should be randomly chosen from, and evenly distributed over, three homogeneous wafer lots in the technology to be certified and from the fabrication facility to be certified. These wafers must have passed wafer or wafer lot acceptance requirements, including all appropriate testing of parametric monitors. The accelerated ageing experiments should provide an estimate of the mean time to failure and a distribution of the failure times under worst case operating conditions and circuit layout consistent with the design rules for each wear-out mechanism. From the MTTF and distribution of failures a worst case operating lifetime or a worst case failure rate can be predicted. Test structures should be from completed wafers which have been passivated/glassivated. A summary of the accelerated ageing data and analysis should be prepared in a suitable form for review by the ESCC Executive. The initial evaluation MTTF, failure distribution and acceleration factors should be retained and used as benchmarks for the technology with which subsequent TCV results will be compared.

8.4.2 SEC Testing

As part of evaluation, as a minimum, the quantity of SEC devices specified in the Process Capability and Reliability Assessment Programme or the Evaluation Test Programme is required randomly chosen from, and evenly distributed over, three homogeneous wafer lots in the technology to be certified and from the fabrication facility to be certified. These wafers must have passed wafer or wafer lot acceptance requirements, including all appropriate testing of parametric monitors. The number of SEC device failures will serve as a qualification benchmark for the technology. Failure analysis should be performed on failed SECs to determine each failure category and action should be proposed and taken for correcting any problems found. For technologies which are intended to have a radiation hardness assurance level, the SEC should be subjected to irradiation testing. The SEC reliability data, including failure analysis results, should be prepared in a suitable form for review by the ESCC Executive.

8.5 WAFER ACCEPTANCE PLAN

The Manufacturer shall have a wafer acceptance plan based on electrical and radiation (if applicable) measurement of parametric monitors. This plan should utilise the parametric monitors and should include visual criteria, if applicable. In addition the plan should address the concerns detailed in MIL-STD-883, Test Method 2018 or equivalent test methods (e.g. metallisation, step coverage). The use of Test Method 2018 or an equivalent test method is encouraged, however alternative procedures utilising parametric monitors and in-line monitors can be proposed by the Manufacturer. The plan can be either a wafer by wafer acceptance plan or a wafer lot acceptance plan.

The test sequence given in Chart III(a) of ESCC Generic Specification No. 9010 can also be used by Manufacturers as a baseline guide to suitable test sequences.

8.6 ASSEMBLY AND PACKAGING

The Manufacturer should demonstrate the capability of the assembly and package processes by performing a qualification exercise on the SEC package or an actual product package.

8.6.1 Assembly Processes

The Manufacturer should list the assembly processes (die attachment, wire/ribbon bonding, sealing and marking) that are expected to be listed in the ESCC QML and used in ESCC QML microcircuit assembly and should then qualify these processes by the testing of fully assembled packages in accordance with appropriate tests for the assembly/packaging technology used. The assembly process related tests given in ESCC Basic Specification No. 22600 and the appropriate ancillary Basic Specification and ESCC Generic Specification No. 9000, can be used by Manufacturers as a baseline guide to suitable qualification tests. Sample sizes should be defined by the TRB.

8.6.2 Package Technology Styles

The Manufacturer should document how packages used in the manufacture of ESCC QML products are qualified. In particular, the Manufacturer should document his criteria for deciding which packages can be treated as similar and show how these are grouped together for qualification and change

control purposes. Package technology style qualification test methodologies, vehicles and results should be available. Key package characteristics for which testing must be addressed on each ESCC QML package technology style are:

- Dimensions.
- Resistance to moisture.
- Susceptibility to corrosion.
- Lead integrity.
- Thermal resistance.
- Flammability (for plastic encapsulated devices).
- Outgassing (for plastic encapsulated devices).

The package technology related test given in ESCC Basic Specification No. 22600 and the appropriate ancillary Basic Specification and ESCC Generic Specification No. 9000, can be used by Manufacturers as a baseline guide to suitable testing. Sample sizes should be defined by the TRB.

## 9. ON-SITE VALIDATION AUDIT

### 9.1 GENERAL

The validation by the ESCC Executive will make use of the checklist given in ESCC Basic Specification No. 20200 and the appropriate ancillary Basic Specification and will cover, as a minimum, the following applicable areas of the Manufacturer's facility:

- Management.
- Quality assurance.
- Design.
- Mask manufacture.
- Wafer fabrication.
- Assembly and package.
- Electrical test.

The on-site validation will be performed only after a satisfactory review of the Manufacturer's QM plan and self-validation results.

### 9.2 TECHNOLOGY VALIDATION

A satisfactory review of the following areas during validation by the ESCC Executive, where applicable, is seen as critical for ESCC QML certification and should cover:

- Design centre procedures.
- Design review procedures.
- Model verification.
- Software configuration and configuration management.
- Testability procedures.
- Archival system.
- Mask inspection procedures TCV, SEC and parametric monitor tests and data.
- Fabrication rework procedures.
- SPC programme.
- Design rule documentation.

- Clean room procedures.
- Wafer traceability.
- Wafer and boule evaluation procedures.
- Assembly rework procedures.
- Die attach procedures.
- Wire/ribbon bonding.
- Device traceability and travellers.
- Lot formation (wafer, device and inspection).
- Assembly area environmental control.
- Internal water vapour control programme.
- Electrostatic discharge control and testing.
- Visual inspection.
- Human contamination prevention procedures.
- Equipment calibration and maintenance.
- Training policy and procedures.
- Electrical test procedures.
- Screening procedures.
- Periodic testing procedures.
- Third party design centre procedures.
- Die encapsulation/moulding.
- Qualification test plan.

## 10. QUALIFICATION TEST PLAN

### 10.1 QUALIFICATION TEST VEHICLES

The qualification test programme should define the relevant number of qualification test vehicles to cover the certified Technology Flow which the Manufacturer will produce on the certified manufacturing line. The qualification test vehicles should be of such complexity as to be representative of the ESCC QML microcircuits to be supplied by the Manufacturer. Each vehicle should operate and perform in compliance with the device specification and to the RHACL for a radiation hardened process, and should be manufactured in packages which are suitable for space use and which will not induce additional failures.

### 10.2 QUALIFICATION TEST PLAN

The qualification test plan should detail the test flow, test limits, test data to be measured, recorded and analysed, test sampling techniques and traceability records. As a baseline, the test flow should be based on the qualification testing specified in ESCC Generic Specification No. 9000 and the electrical measurements should be those given in the appropriate Detail Specification. The qualification test plan must be agreed and approved between the Manufacturer and the ESCC Executive.

### 10.3 QUALIFICATION TEST REPORT

The Manufacturer should present to the ESCC Executive an analysis of the qualifying data. The aim of this analysis is to show that all process variables are under control and repeatable within the certified technology and that parametric monitor, TCV and SEC data monitoring is adequate and correlatable to the process. The ESCC Executive should be notified of any improvements/changes to the certified ESCC QML Technology Flow as a result of evaluation of the qualification test results. The following

data, if applicable, should be addressed and retained by the Manufacturer to support the results:

- Simulation results from the design process.
- Parametric monitor test data.
- Results of each subgroup test conducted, both initial and any resubmissions.
- Number of devices tested and rejected.
- Failure mode and mechanism for each rejected device.
- Read and record variables data on all specified electrical parameter measurements.
- Where delta limits are specified, variable data, identified to the microcircuit serial number, should be provided for initial and final measurements.
- If physical dimensions are checked, the actual dimensions of three randomly selected microcircuits should be recorded, except where verification of dimensions by calibrated gauges, overlays, or other comparative dimensions verification devices has been approved.
- For bond strength testing, the forces at the time of failure and the failure category, or the minimum and maximum readings of the microcircuits if no failures occur.
- For die shear or stud pull strength testing, the forces at the time of the failure and the failure category, or the die shear or stud pull reading if no separation occurs.
- For RHA testing, pre and post test end-point electrical parameters, transient and SEP responses and test conditions (if applicable).
- For lid torque strength testing, the forces at the time of failure or the actual torque if no failure occurs.
- For internal water vapour content readings, report of all gases found.

10.4 QUALIFICATION TEST FAILURES

If any particular testing results are not successful, the Manufacturer should perform failure analysis and take any necessary corrective action after consultation with the ESCC Executive. The Manufacturer should notify the ESCC Executive of any decision not to pursue qualification of any material or manufacturing construction technique previously certified. After corrective actions have been implemented, qualification testing should restart.

## 11. RADIATION HARDNESS ASSURANCE

11.1 GENERAL

This section is only applicable for technologies and devices which are specifically designed and supplied as Radiation Hardness Assured (RHA). It defines additional procedures and requirements which are necessary for establishing a Radiation Hardness Assurance Capability Level (RHACL) for the technology. The defined changes and additions affect the following areas:

- The Quality Management Plan.
- Parametric monitors, TCVs and SECs.
- The Evaluation Test Plan.
- Radiation verification testing.

All of the general requirements given in ESCC Basic Specification No. 25400 and the previous sections of this specification shall continue to be applicable, unless specifically excluded.

The main concern with RHA is whether the device specification accurately describes the device performance in the radiation environment specified. This will initially require some actual device radiation testing, but it should be possible to reduce or eleminate many device orientated tests once the correlation data for appropriate models and test structures has been established by the TRB.

11.2 QUALITY MANAGEMENT PLAN

The QM Plan should specifically address RHA testing, characterisation and verification for the manufacturing processes and components manufactured using them. It should establish the procedures to be followed to ensure that devices meet the RHACL. It is the responsibility of the manufacturer's TRB to evaluate the test methods to be used.

11.3 SPECIAL TEST CIRCUITS

11.3.1 Parametric Monitors

The parametric monitor is an integral part of a technology's RHA SPC programme for in-line process monitoring. The structures must be carefully designed and configured to ensure the accurate characterisation of a technology's radiation performance and capability. The parametric monitor shall support wafer acceptance testing and periodic testing.

Where RHA ia a requirement of the ESCC QML line then, as a minimum, process monitors for RHA qualified technologies shall include test structures to support the following:-

(a) **MOS RHA Parameters**

1. Gate oxide thickness. Structures shall be included to ensure gate oxide thickness since this is a critical parameter affecting radiation performance.
2. The following parameters shall be measured as a function of total ionising dose:
   - Threshold voltage ($V_T$). The linear $V_T$ for each transistor in a cell.
   - Linear transconductance ($g_m$). The linear $g_m$ for a set of transistors.
   - $I_{on}/I_{off}$ (leakage current).
   - Propagation delay time ($t_p$). A test structure in the form of a functional circuit such as in inverter or register chain shall be available to support this measurement.
   - Field transistor leakage. Field transistor leakage for the minimum design/layout rules.

(b) **Bipolar Parameters**

The bipolar parameters defined in Para. 7.1(c) shall be measured as a function of ionising dose and neutron/proton fluence, as appropriate.

(c) **Radiation Hardness Assurance**

When RHA is a requirement of the technology, the parametric monitor shall include test structures to monitor the following phenomena, as applicable:

- Dose-rate latch-up.
- Dose-rate upset.
- Single-event effects.
- Total ionising dose.
- Displacement damage from neutron or proton irradiation.

(d) **Other RHA Considerations**

In addition, test structures to monitor and characterise radiation response mechanisms and for linear circuit applications shall be included, as appropriate. These structures would include but not be limited to:

- Matched transistor pairs for offset current and voltage characterisation.
- Annular and dual or multi-edged transistor sets for sub-threshold I-V characterisation.

- Four contact devices for charge pumping measurements.

11.3.2 TCV Testing

The TCV programme is an integral part of a technology's RHA and must be carefully configured to ensure the accurate characterisation of a technology's radiation capability. The TCV programme shall be designed to support:

- RHA activities.
- Parametric extraction.
- Model development and validation.
- SPC.
- Failure mode analysis.

To determine that the RHACL is appropriate for the technology, the Manufacturer shall irradiate the TCV to 2x the RHACL or until failure to determine failure mode and mechanisms. Failure can be either functional or pararnetric. Also, the bounds of radiation response shall be determined by testing the appropriate TCV test structures for worst case bias conditions, annealing conditions and temperature.

11.3.3 SEC Testing

The SEC shall utilise all radiation hardness assurance design rules and shall be used to demonstrate the specified level of performance at the RHACL. When radiation hardness assurance is a requirement of the technology, the SEC shall be used to certify and monitor the RHACL of a specific fabrication technology in a specific fabrication facility. The SEC shall be designed so that it can be used to assess and monitor the radiation hardness of the fabrication process and the design rules. All SEC reliability data, including failure analysis results, shall be made available for review by the ESCC Executive. For RHA environments, the Manufacturer shall irradiate SEC to 2x the requested RHACL or to failure, whichever occurs first, under worst case bias, annealing and temperature conditions as a demonstration of the technology's capability to meet the RHACL. A different SEC might be required whenever the design rules, materials, basic processes or the basic functionality of the technology differ.

11.4 RADIATION TEST PLAN

11.4.1 General

An RHACL shall be established for the environments selected by the TRB and consistently demonstrated for a technology at the specified level of electrical performance. Changes in the RHACL may require re-evaluation of these capabilities by the TRB. The following radiation requirements shall be addressed:

- Total ionising dose and time dependant effects for ioising radiation.
- Single event effects (SEE), including upset, latch-up, burnout, gate rupture caused by galactic cosmic rays, solar enhanced particles and energetic neutrons and protons.
- Displacement damage caused by energetic neutrons and protons.

11.4.2 Design

The Manufacturer shall address the design methodology for the following areas of design:-

(a) **Model Verification**

Model verification shall provide evidence that models defining device response in radiation environments accurately predict the nominal and worst case circuit response over operating voltage limits and over the temperature range selected for the technology at the RHACL.

(b) **Design Rule Verification**

The Manuafacturer shall document his design rules for radiation hardening his technology and the

procedures for verifying rule compliance.

(c) **Performance Verification**

The Manufacturer shall demonstrate his ability to predict the response of the post-irradiation performance at the RHACL including the effects of the specified limits for temperature and voltage variations and the influence of process variations.

11.4.3 SPC and In-process Monitoring Programme

SPC is especially critical for maintaining a technology's RHACL. This is because relatively minor changes in a process flow can drastically affect device radiation performance. The Manufacturer shall identify and document all critical process nodes associated with RHA.

11.4.4 Wafer Acceptance Plan

The TRB shall develop and demonstrate a wafer acceptance plan based on electrical and radiation measurement of parametric monitors. Parametric monitors shall be used to determine wafer and wafer lot uniformity and latch-up immunity, when specified. Further testing of actual devices to Table 1 might also be required. As an option to actual device testing, after initial establishment of the device specification and Post-irradiation Parameter Limits (PIPL), additional procedures based on parametric monitor testing could be adopted.

The following procedures are presented as examples for the specified radiation environments:-

(a) **Latch-up**

The parametric monitor should utilise worst case latch-up structures to determine latch-up holding voltage at maximum temperature. The holding voltage must be greater than the maximum rated voltage.

(b) **SEE**

The parametric monitor should utilise SEE structures such as cross-coupling resistors to memory cells to assure critical parameters agree with worst case acceptance criteria.

(c) **Dose Rate**

The parametric monitor should utilise structures to ensure rail span collapse does not cause upset or burnout or both and that the metallisation resistivity, contact resistance, via resistance, epi, substrate resistivity and minority carrier lifetime specifications are met.

(d) **Total Ionising Dose**

The parametric monitor should utilise structures such as capacitors and transistors to ensure that critical parameters agree with worst case PIPL values.

11.4.5 Assembly and Packaging

Packages used for RHA microcircuits shall be characterised for effects which might influence the hardness of packaged product. Characterisation shall include impedance of the power and ground distribution network, impendance contributions of bond wires and die attach and the impedance associated with any passive elements included as integral parts of the package. Qualification of the same die in different packages shall require demonstration either by test or similarity analysis.

The qualification test vehicles shall be manufactured in packages which have passed the requirements of this paragraph. For technology which has dice as its primary product, the qualification test vehicles shall be suitably packaged to allow evaluation of the technology without adversely affecting the outcome of the tests.

11.5 RADIATION VERIFICATION TESTING

11.5.1 Traceability

Traceability to at least the wafer lot shall be provided for all delivered microcircuits. Traceability shall document, as a minimum, the completion of each step required in design (where applicable),

fabrication, assembly, test and any applicable qualified rework procedure.

11.5.2 Design Requirements

The Manufacturer shall show evidence that all ESCC QML/RHA product has been through the qualified RHA Technology Flow. For RHA devices, sample testing of each design to verify PIPL shall be conducted to determine total dose hardness level, dose rate upset threshold, latch-up immunity when specified, at maximum temperature and voltage and Linear Energy Transfer Threshold ($LET_{TH}$) for upset and latch-up as well as the cross section for SEE. If simulation models can be verified by test to address these concerns, they would be acceptable. It is anticipated that several different designs will be tested for any ASIC family.

11.5.3 Radiation Response Characterisation

When specified in the Radiation Test Plan, radiation response characterisation data shall be provided for ESCC QML microcircuits in those environments specified in the device specification. The characterisation shall be obtained in increments of irradiation levels to failure or to a radiation level at or beyond the specification level as determined by the TRB. The characterisation data shall be accompanied by the mean and standard deviation of the critical parameters. The results obtained from the Table 1 testing herein shall be periodically added to the characterisation data at fluence level, dose rate and parameter levels defined in the device specification test conditions.

11.5.4 End-of-line Lot Radiation Verification Testing (Option 1)

End-of-line RVT shall include hardness assurance tests on each wafer lot. The PIPL, transient and Single Event Phenomenon (SEP) response (as applicable) and test conditions shall be as specified in the device specification. All RVT shall be performed on microcircuit types which are to be supplied as RHA ESCC QML microcircuits.

RVT is required only for parts intended to be marked as radiation hardness assured. RHA quality conformance sample tests are to be performed in accordance with Table 1 herein. The applicable subgroups shall be performed when the Manufacturer states that his components are RHA. The actual devices used for testing shall be assembled in a qualified package and, as a minimum and prior to irradiation, shall pass any room temperature static, functional and switching electrical tests which are defined in the Detail Specification. After irradiation testing, the devices shall meet the electrical requirements defined in the Detail Specification for post-irradiation testing.

If a Manufacturer elects to eliminate an end-of-line test by substituting an in-process control or statistical process control procedure, the Manufacturer is, with the approval of the ESCC Executive, only relieved of the responsibility of performing that actual test. The Manufacturer is still responsible for providing a product which meets all of the performance, quality and reliability requirements herein and in the device specification. Documentation supporting substitution for end-of-line testing shall be retained by the Manufacturer and be available to the ESCC Executive on request. For some devices there are differences in the total dose radiation response before and after burn-in. Unless it has been shown by prior characterisation or by design that burn-in has negligible effect (parameters remain within post-irradiation electrical limits) on the total dose radiation response, then one of the following must be done:-

(a) The Manufacturer shall subject the radiation samples to the specified burn-in conditions prior to conducting total dose radiation testing.

(b) The Manufacturer shall develop a correction factor (which is acceptable to the parties to the test) taking into account the changes in total dose response resulting from subjecting the product to burn-in. The correction factor shall then be used to accept product for total dose response without subjecting the test samples to burn-in.

11.5.5 In-line Testing (Option 2)

In-line control testing shall be performed through the use of the approved SEC or ESCC QML microcircuit. The following shall be addressed for RHA devices; the testing described in Para. 11.5.4 shall be performed on the SEC, or product meeting SEC complexity, at intervals set by the TRB in the QM plan. Burn-in shall be addressed as per (a) or (b) in Para. 11.5.4.

## 12. PROCUREMENT

Procurement of components manufactured within the boundaries of the qualified Technology Flow shall be in accordance with the requirements of ESCC Generic Specification No. 9000.

**TABLE 1 - RADIATION VERIFICATION TESTING**

| Subgroup | Test | Test Method (Note 1) | RHACL/Spec (Note 2) | Quantity (Accept No.) (Note 3) | Notes |
|---|---|---|---|---|---|
| 1 | Total ionisation dose | ESCC No. 22900, MIL-STD-883 Method 1019 or equivalent | >10 | No testing required | |
| | | | >1=10 | 2(0) devices/wafer or | 4, 9 |
| | | | | 22(0) devices/wafer lot | 4 |
| | | | >1=10 (>100 000 equivalent transistors per die) | 1(0) devices/wafer plus 4(0) test structures/wafer or | 4, 5 |
| | | | | 5(0) devices/wafer lot plus 4(0) test structures/wafer | 4, 5 |
| 2 | Transient ionisation | MIL-STD-883 Method 1021, Method 1023 or equivalent | | 2(0) devices/wafer or | 6 |
| | | | | 11(0) devices/wafer lot | 6 |
| 3 | Dose-rate latch-up | MIL-STD-883 Method 1020 or equivalent | | As specified in the device specification | 6, 7 |
| 4 | Single-event effects | ESCC No. 25100, EIA/JESD 57 or equivalent | | 4(0) devices/wafer | 6, 8 |

**NOTES**

1. End-point electrical parameter measurements shall be as specified in the Detail Specification.
2. RHACL/spec is the ratio of the radiation hardness capability level established for the technology/component type to the fluence level defined in the specification.
3. A wafer lot may be tested either as a lot, or alternatively on a wafer by wafer basis. If each wafer is individually tested then a PDA, to be agreed between the Manufacturer and the ESCC Executive, shall apply for the number of wafers rejected from the lot.
4. Parts used for one subgroup test shall not be used for other subgroups, but may be used for higher levels in the same subgroup. For subgroup 2, total dose exposure shall not be considered cumulative unless testing is performed within the time limits of the test method.
5. The test structures shall be randomly selected from the wafer. An x-ray source may be used on test structures at the wafer level provided correlation has been established between the x-ray and the cobalt-60 source.
6. Tests to be conducted only when the Manufacturer states that his components are RHA to these effects.
7. Latch-up testing is not required for SOS, SOI and dielectrically isolated technologies when latch-up is physically not possible. Test conditions, sample size, test temperature and the electrical parameters to be measured pre, post and during irradiation shall be specified in the device specification.
8. SEE testing shall be performed during qualification and after any design or process change that might affect SEE response.
9. Traceability to the specific wafer is required.