INTEGRATED CIRCUITS, SILICON MONOLITHIC, 32-BIT

SPARC EMBEDDED PROCESSOR,

BASED ON TYPE TSC695F

ESCC Detail Specification No. 9512/003

Issue 2	February 2006

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DOCUMENTATION CHANGE NOTICE

(Refer to https://escies.org for ESCC DCR content)

DCR No.	CHANGE DESCRIPTION
206, 207	Specification upissued to incorporate editorial and technical changes per DCR.

TABLE OF CONTENTS

1. GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics, test and inspection data for the component type variants and/or the range of components specified below. It supplements the requirements of, and shall be read in conjunction with, the ESCC Generic Specification listed under Applicable Documents.

1.2 APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:

(a) ESCC Generic Specification No. 9000.
(b) MIL-STD-883, Test Methods and Procedures for Microelectronics.

1.3 TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESCC Basic Specification No. 21300 shall apply.

1.4 THE ESCC COMPONENT NUMBER AND COMPONENT TYPE VARIANTS

1.4.1 The ESCC Component Number

The ESCC Component Number shall be constituted as follows:
Example: 951200301R

- Detail Specification Reference: 9512003
- Component Type Variant Number: 01 (as required)
- Total Dose Radiation Level Letter: R (as required)

1.4.2 Component Type Variants

The component type variants applicable to this specification are as follows:

Variant Number	Based on Type	Case	Terminal Material and Finish	Weight Max g	Total Dose Radiation Level Letter
01	TSC695F	MQFP-F256	G2	15	R[100kRAD(Si)]

The terminal material and finish shall be in accordance with the requirements of ESCC Basic Specification No. 23500.
The total dose radiation level letter shall be as defined in ESCC Basic Specification No. 22900. If an alternative radiation test level is specified in the Purchase Order the letter shall be changed accordingly.

1.5 MAXIMUM RATINGS

The maximum ratings shall not be exceeded at any time during use or storage. Functional performance for extended periods at the maximum ratings may adversely affect device reliability.
Maximum ratings shall only be exceeded during testing to the extent specified in this specification and when stipulated in Test Methods and Procedures of the ESCC Generic Specification.

Characteristics	Symbols	Maximum Ratings	Units	Remarks
Supply Voltage	V_{DD}	-0.5 to +7	V	1
Input Voltage Range	V_{IN}	-0.5 to V_{DD} +0.5	V	2
Input Current per Signal pin per Power pin	I_{IN}	 -10 to +10 -50 to +50	mAdc	
Output Current	I_{OUT}	-90 to +110	mAdc	3
Device Power Dissipation	P_D	1.5	W	
Operating Temperature	T_{op}	-55 to +125	°C	T_{amb}
Storage Temperature	T_{stg}	-65 to +150	°C	
Junction Temperature	T_j	165	°C	
Thermal Resistance	$R_{th(j-c)}$	3	°C/W	
Soldering Temperature	T_{sol}	265	°C	4

NOTES:

1. Device is functional for $4.5 \leq V_{DD} \leq 5.5V$ with reference to V_{SS} = 0V.
2. V_{DD} +0.5V shall not exceed +7V.
3. The maximum output current of any single output for a maximum duration of 1 second.
4. Duration 10 seconds maximum at a distance of not less than 1.6mm from the device body and the same terminal shall not be resoldered until 3 minutes have elapsed.

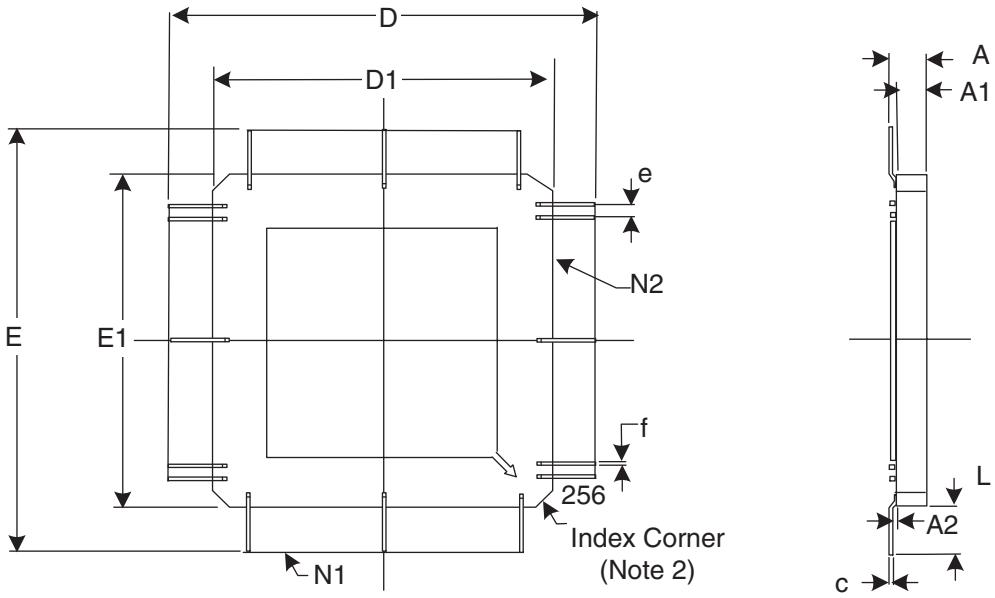
1.6 HANDLING PRECAUTIONS

These devices are susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacture, testing, packaging, shipment and any handling.

These components are categorised as Class 1 per ESCC Basic Specification No. 23800 with a Minimum Critical Path Failure Voltage of 1000 volts.

1.7 PHYSICAL DIMENSIONS AND TERMINAL IDENTIFICATION

Multilayer Quad Flat Package (MQFP-F256) - 256 Flat Leads

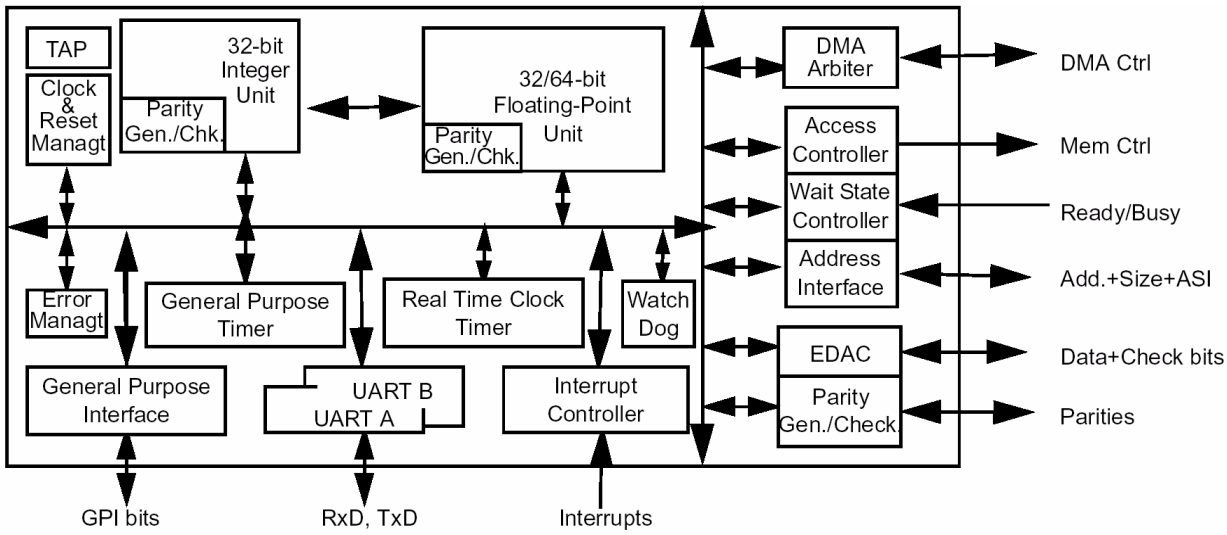


Symbols	Dimensions mm		Notes
	Min	Max	
A	2.41	3.18	
A1	2.06	2.56	
A2	0.05	0.36	
c	0.1	0.2	1
D, E	53.23	55.74	
D1, E1	36.83	37.34	
e	0.508 BSC		1
f	0.15	0.25	1
L	8.2	9.2	1
N1, N2	64		Each Side

NOTES:

1. All leads
2. Terminal identification is specified by reference to the index corner as shown.

1.8 FUNCTIONAL DIAGRAM



1.9 PIN ASSIGNMENT AND DESCRIPTION

Pin	Function
1	GPINNT
2	GPI[7]
3	V_{DDO}
4	V_{SSO}
5	GPI[6]
6	GPI[5]
7	GPI[4]
8	GPI[3]
9	V_{DDO}
10	V_{SSO}
11	GPI[2]
12	GPI[1]
13	GPI[0]
14	D[31]
15	D[30]
16	V_{DDO}
17	V_{SSO}
18	D[29]
19	D[28]
20	V_{DDI}

Pin	Function
21	V_{SSI}
22	D[27]
23	D[26]
24	V_{DDO}
25	V_{SSO}
26	D[25]
27	D[24]
28	D[23]
29	D[22]
30	V_{DDO}
31	V_{SSO}
32	D[21]
33	D[20]
34	D[19]
35	D[18]
36	V_{DDO}
37	V_{SSO}
38	D[17]
39	D[16]
40	V_{DDI}
41	V_{SSI}
42	D[15]
43	D[14]
44	V_{DDO}
45	V_{SSO}
46	D[13]
47	D[12]
48	D[11]
49	D[10]
50	V_{DDO}
51	V_{SSO}
52	D[9]
53	D[8]
54	D[7]
55	D[6]
56	V_{DDO}

Pin	Function
57	V_{SSO}
58	D[5]
59	D[4]
60	D[3]
61	D[2]
62	V_{DDO}
63	V_{SSO}
64	D[1]
65	D[0]
66	RSIZE[1]
67	RSIZE[0]
68	RASI[3]
69	V_{DDO}
70	V_{SSO}
71	RASI[2]
72	RASI[1]
73	RASI[0]
74	RA[31]
75	RA[30]
76	V_{DDO}
77	V_{SSO}
78	RA[29]
79	RA[28]
80	RA[27]
81	V_{DDO}
82	V_{SSO}
83	RA[26]
84	RA[25]
85	RA[24]
86	V_{DDI}
87	V_{SSI}
88	V_{DDO}
89	V_{SSO}
90	RA[23]
91	RA[22]
92	RA[21]

Pin	Function
93	V_{DDO}
94	V_{SSO}
95	RA[20]
96	RA[19]
97	RA[18]
98	V_{DDO}
99	V_{SSO}
100	RA[17]
101	RA[16]
102	RA[15]
103	V_{DDO}
104	V_{SSO}
105	RA[14]
106	V_{DDI}
107	V_{SSI}
108	RA[13]
109	RA[12]
110	V_{DDO}
111	V_{SSO}
112	RA[11]
113	RA[10]
114	RA[9]
115	V_{DDO}
116	V_{SSO}
117	RA[8]
118	RA[7]
119	RA[6]
120	V_{DDO}
121	V_{SSO}
122	RA[5]
123	RA[4]
124	RA[3]
125	V_{DDO}
126	V_{SSO}
127	RA[2]
128	RA[1]

Pin	Function
129	RA[0]
130	V_{DDO}
131	V_{SSO}
132	RAPAR
133	RASPAR
134	DPAR
135	V_{DDO}
136	V_{SSO}
137	SYSCLK
138	TDO
139	$\overline{\text{TRST}}$
140	TMS
141	TDI
142	TCK
143	CLK2
144	$\overline{\text{DRDY}}$
145	DMAAS
146	V_{DDO}
147	V_{SSO}
148	$\overline{\text{DMAGNT}}$
149	$\overline{\text{EXMCS}}$
150	V_{DDI}
151	V_{SSI}
152	$\overline{\text{DMAREQ}}$
153	$\overline{\text{BUSERR}}$
154	$\overline{\text{BUSRDY}}$
155	$\overline{\text{ROMWRT}}$
156	$\overline{\text{NOPAR}}$
157	$\overline{\text{SYSHALT}}$
158	$\overline{\text{CPUHALT}}$
159	V_{DDO}
160	V_{SSO}
161	SYSERR
162	SYSAV
163	EXTINT[4]
164	EXTINT[3]

Pin	Function
165	EXTINT[2]
166	EXTINT[1]
167	EXTINT[0]
168	V_{DDI}
169	V_{SSI}
170	EXTINTACK
171	$\overline{IUERR}$
172	V_{DDO}
173	V_{SSO}
174	CPAR
175	TXA
176	RXA
177	RXB
178	TXB
179	$\overline{IOWR}$
180	$\overline{IOSEL}$[3]
181	V_{DDO}
182	V_{SSO}
183	$\overline{IOSEL}$[2]
184	$\overline{IOSEL}$[1]
185	$\overline{IOSEL}$[0]
186	WRT
187	$\overline{WE}$
188	V_{DDO}
189	V_{SSO}
190	RD
191	RLDSTO
192	LOCK
193	DXFER
194	$\overline{MEXC}$
195	V_{DDO}
196	V_{SSO}
197	$\overline{RESET}$
198	$\overline{SYSRESET}$
199	BA[1]
200	BA[0]

Pin	Function
201	CB[6]
202	CB[5]
203	V_{DDO}
204	V_{SSO}
205	CB[4]
206	CB[3]
207	CB[2]
208	CB[1]
209	V_{DDO}
210	V_{SSO}
211	CB[0]
212	$\overline{ALE}$
213	V_{DDI}
214	V_{SSI}
215	$\overline{PROM8}$
216	$\overline{ROMCS}$
217	$\overline{MEMCS}$[9]
218	V_{DDO}
219	V_{SSO}
220	$\overline{MEMCS}$[8]
221	$\overline{MEMCS}$[7]
222	$\overline{MEMCS}$[6]
223	$\overline{MEMCS}$[5]
224	$\overline{MEMCS}$[4]
225	$\overline{MEMCS}$[3]
226	V_{DDO}
227	V_{SSO}
228	$\overline{MEMCS}$[2]
229	$\overline{MEMCS}$[1]
230	$\overline{MEMCS}$[0]
231	V_{DDI}
232	V_{SSI}
233	$\overline{OE}$
234	V_{DDO}
235	V_{SSO}
236	$\overline{MEMWR}$

Pin	Function
237	$\overline{\text{BUFFEN}}$
238	DDIR
239	V_{DDO}
240	V_{SSO}
241	$\overline{\text{DDIR}}$
242	$\overline{\text{MHOLD}}$
243	$\overline{\text{MDS}}$
244	WDCLK
245	IWDE
246	EWDINT
247	TMODE[1]
248	TMODE[0]
249	DEBUG
250	INULL
251	DIA
252	V_{DDO}
253	V_{SSO}
254	FLUSH
255	INST
256	RTC

Signal	Type	Active	Description	
RA[31-0]	I/O		32-bit registered address bus	Output buffer: 400pF
RAPAR	I/O	High	Registered address bus parity	-
RAS[3-0]	I/O		4-bit registered address space identifier	-
RSIZE[1-0]	I/O		2-bit registered bus transaction size	-
RASPAR	I/O	High	Registered ASI and SIZE parity	-
CPAR	I/O	High	Control bus parity	-
D[31-0]	I/O		32-bit data bus	-
CB[6-0]	I/O		7-bit check-bit bus	-
DPAR	I/O	High	Data bus parity	-
RLDSTO	I/O	High	Registered atomic load-store	-
$\overline{\text{ALE}}$	O	Low	Address latch enable	-
DXFER	I/O	High	Data transfer	-
LOCK	I/O	High	Bus lock	-

Signal	Type	Active	Description	
RD	I/O	High	Read access	-
$\overline{WE}$	I/O	Low	Write enable	-
WRT	I/O	High	Advanced write	-
$\overline{MHOLD}$	O	Low	Memory bus hold	MHOLD + FHOLD + BHOLD + FCCV
$\overline{MDS}$	O	Low	Memory data strobe	-
$\overline{MEXC}$	O	Low	Memory exception	-
$\overline{PROM8}$	I	Low	Select 8-bit wide PROM	-
BA[1-0]	O		Latched address used for 8-bit wide boot PROM	-
$\overline{ROMCS}$	O	Low	PROM chip select	-
$\overline{ROMWRT}$	I	Low	ROM write enable	-
$\overline{MEMCS}$[9-0}	O	Low	Memory chip select	Output buffer: 400pF
$\overline{MEMWR}$	O	Low	Memory write strobe	Output buffer: 400pF
$\overline{OE}$	O	Low	Memory output enable	Output buffer: 400pF
$\overline{BUFFEN}$	O	Low	Data buffer enable	
DDIR	O	High	Data buffer direction	-
$\overline{DDIR}$	O	Low	Data buffer direction	-
$\overline{IOSEL}$[3-0]	O	Low	I/O chip select	-
$\overline{IOWR}$	O	Low	I/O and exchange memory write strobe	-
$\overline{EXMCS}$	O	Low	Exchange memory chip select	-
$\overline{BUSRDY}$	I	Low	Bus ready	-
$\overline{BUSERR}$	I	Low	Bus Error	-
$\overline{DMAREQ}$	I	Low	DMA request	-
$\overline{DMAGNT}$	O	Low	DMA grant	-
DMAAS	I	High	DMA address strobe	-
$\overline{DRDY}$	O	Low	Data ready during DMA access	-
$\overline{IUERR}$	O	Low	IU error	-
$\overline{CPUHALT}$	O	Low	Proecessor (IU & FPU) halt and freeze	-
SYSERR	O	High	System error	-
$\overline{SYSHALT}$	I	Low	System halt	-
SYSAV	O	High	System availability	-
$\overline{NOPAR}$	I	Low	No parity	-
INULL	O	High	Integer unit nullify cycle	-

Signal	Type	Active	Description	
INST	O	High	Instruction fetch	Used to check the execute stage of IU instruction pipeline
FLUSH	O	High	FPU instruction flush	
DIA	O	High	Delay instruction annulled	
RTC	O	High	Real Time Clock Counter output	-
RxA/RxB	I		Receive data UART “A” and “B”	Input trigger
TxA/TxB	O		Transmit data UART “A” and “B”	-
GPI[7-0]	I/O		GPI input/output	Input trigger
GPIINT	O	High	GPI interrupt	-
EXTINT[4-0]	I		External interrupt	Input trigger
EXTINTACK	O	High	External interrupt acknowledge	-
IWDE	I	High	Internal watch dog enable	-
EWDINT	I	High	External watch dog input interrupt	Input trigger
WDCLK	I		Watch dog clock	-
CLK2	I		Double frequency clock	-
SYSCLK	O		System clock	-
$\overline{\text{RESET}}$	O	Low	Output reset	-
$\overline{\text{SYSRESET}}$	I	Low	System input reset	Input trigger
TMODE[1-0]	I		Factory test mode	Functional mode = 00
DEBUG	I	High	Software debug mode	-
TCK	I		Test (JTAG) clock	-
$\overline{\text{TRST}}$	I	Low	Test (JTAG) reset	Pull-up = 37kΩ
TMS	I		Test (JTAG) mode select	Pull-up = 37kΩ
TDI	I		Test (JTAG) data input	Pull-up = 37kΩ
TDO	O		Test (JTAG) data output	-
V_{DDI}/V_{SSI}			Main internal power	-
V_{DDO}/V_{SSO}			Output driver power	-

NOTES:

1. If not specified, the output buffer type is 150pF, the input buffer type is TTL.

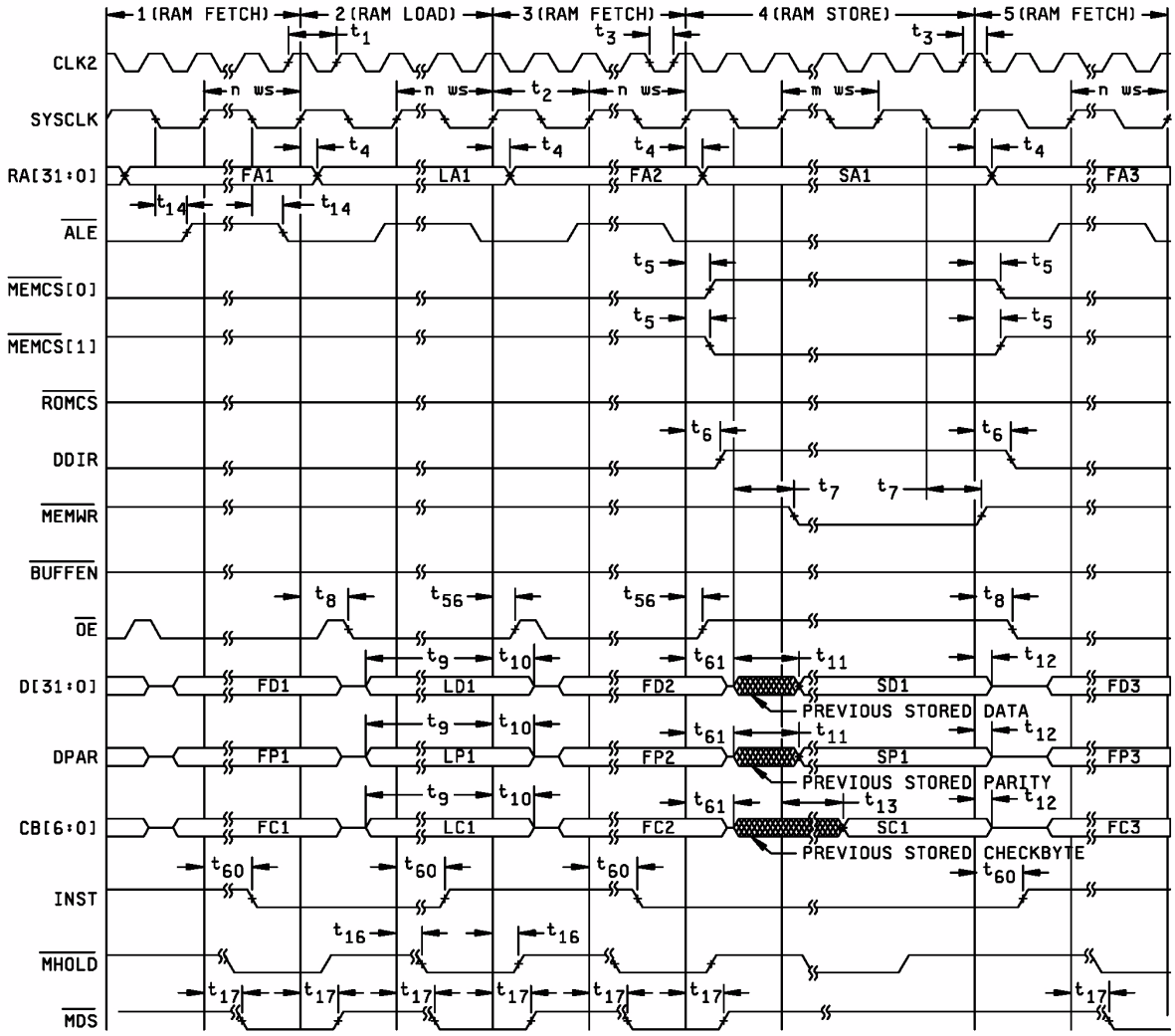
1.10 INSTRUCTION SET AND TIMING DIAGRAM

TSC695F instructions fall into six functional categories: load/store, arithmetic/logical/shift, control transfer, read/write control register, floating-point and miscellaneous. Refer to SPARC 7 Instruction-set Manual.

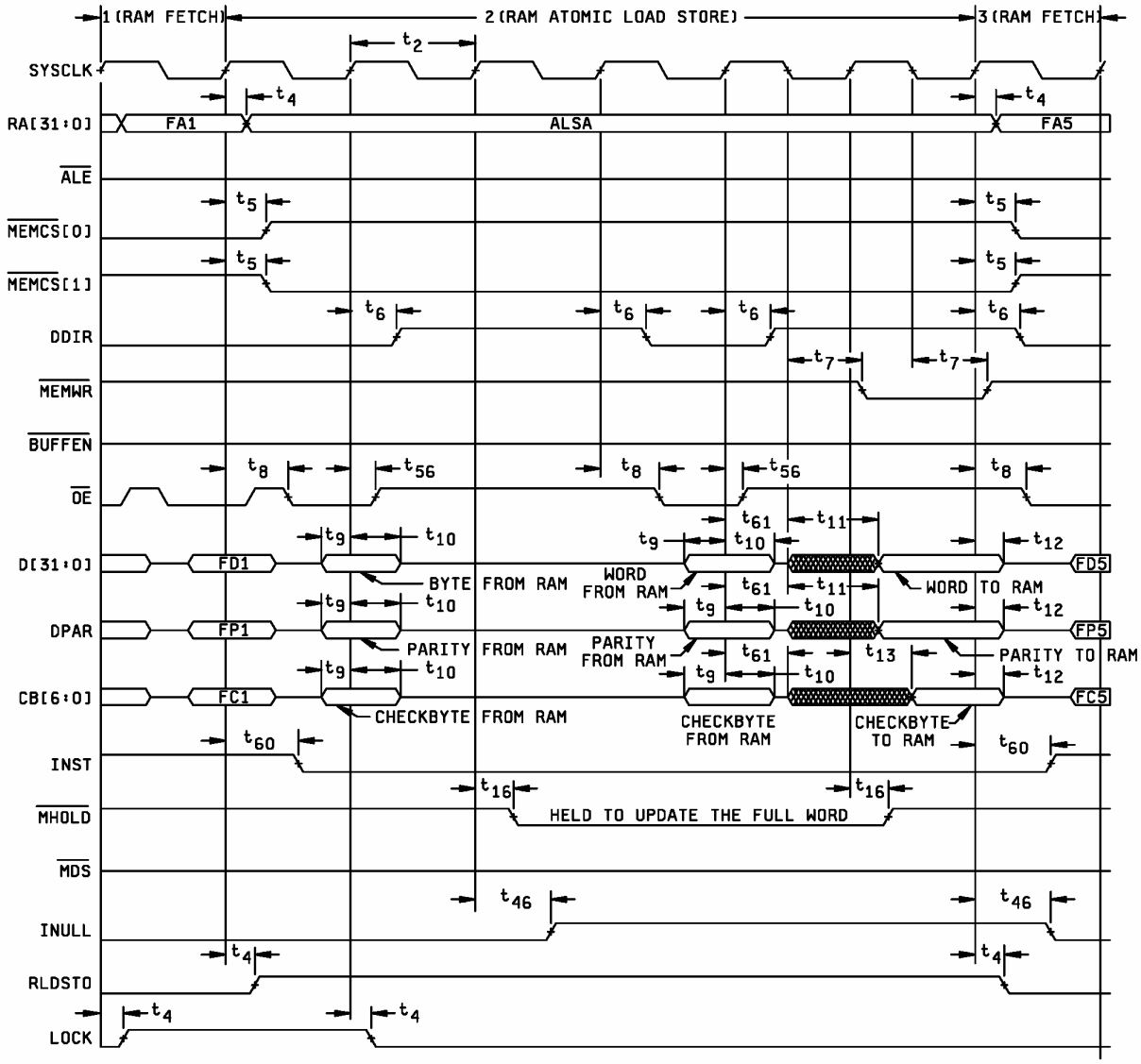
The latest revision of SPARC 7 Instruction-set Manual and the TSC695F SPARC 32-bit Space Processor User Manual are available at www.Atmel.com.

The timing diagrams applicable to parameters specified in this specification are as follows.

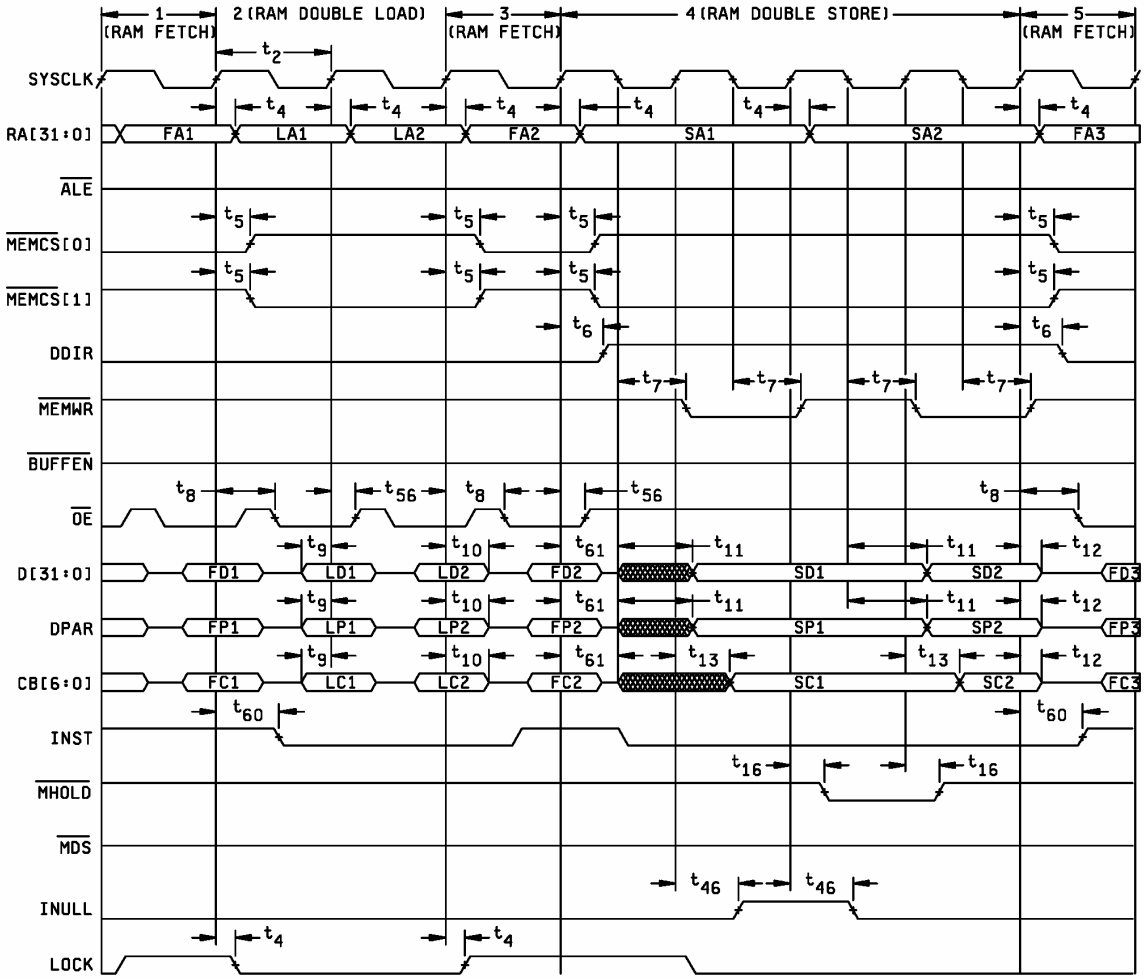
RAM FETCH, RAM LOAD AND RAM STORE SEQUENCE - N WAITSTATES FOR READ, M WAITSTATES FOR WRITE



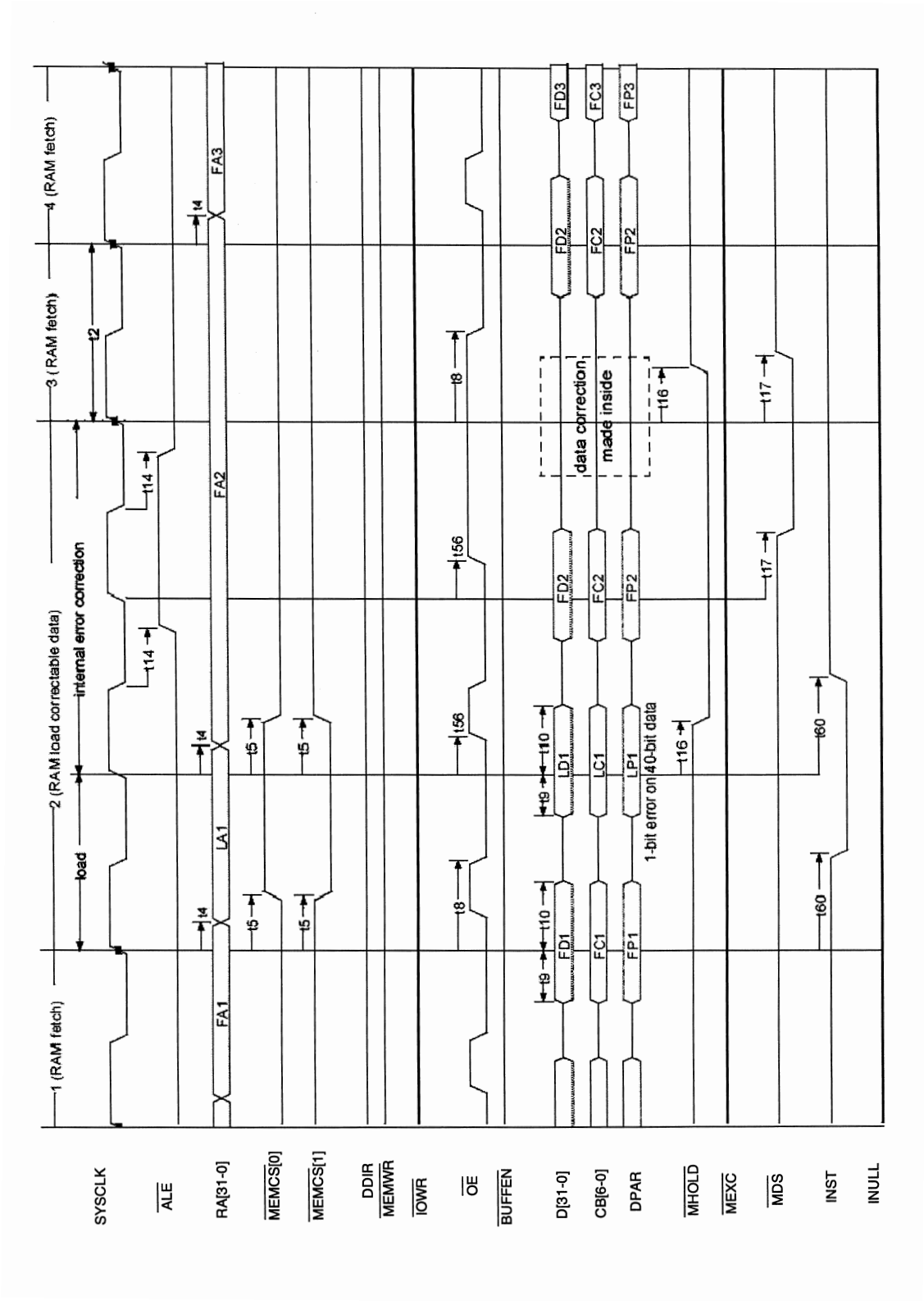
RAM ATOMIC - LOAD - STORE BYTE SEQUENCE - 0 WAITSTATE



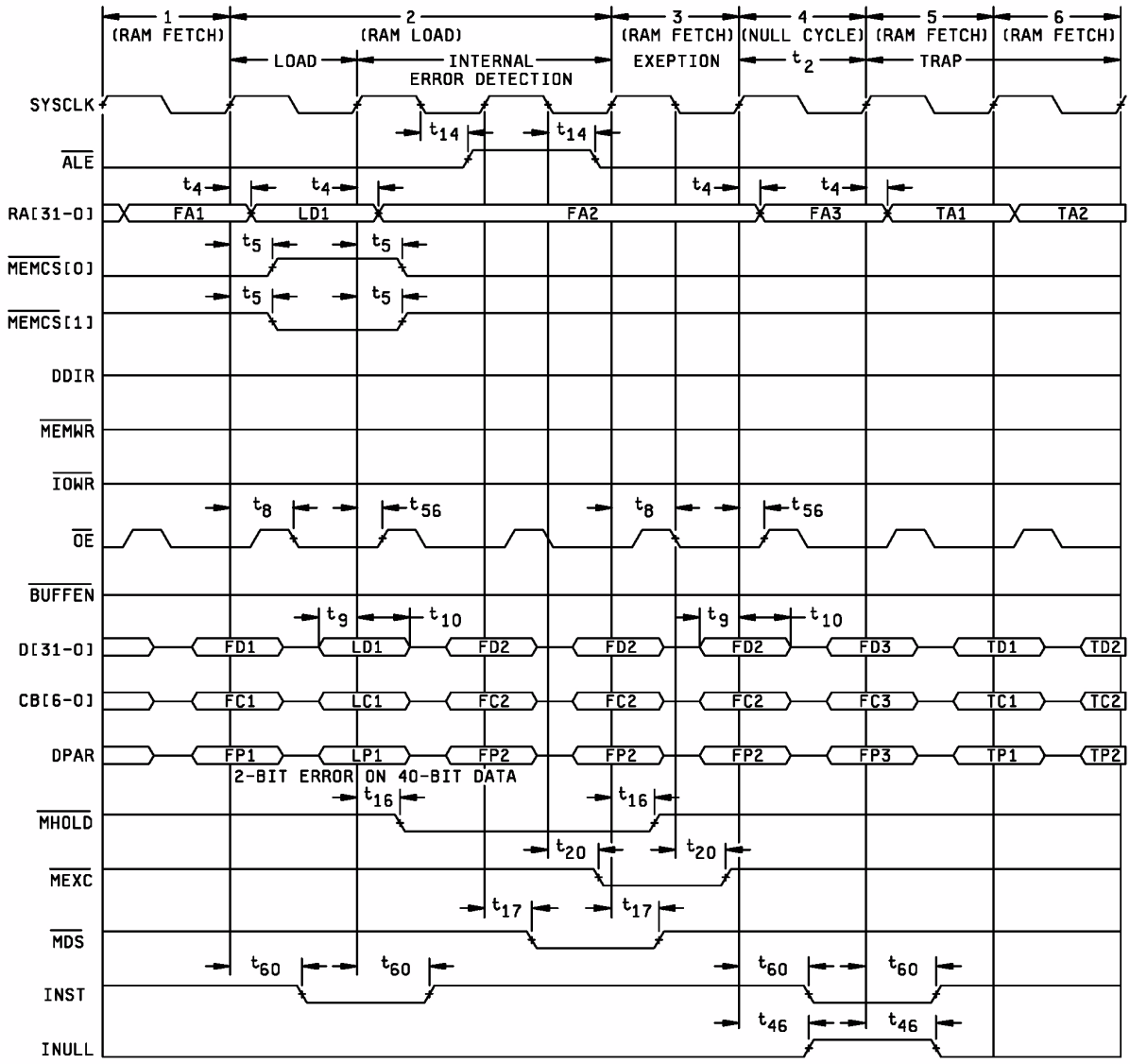
RAM LOAD - DOUBLE AND RAM STORE - DOUBLE SEQUENCE - 0 WAITSTATE



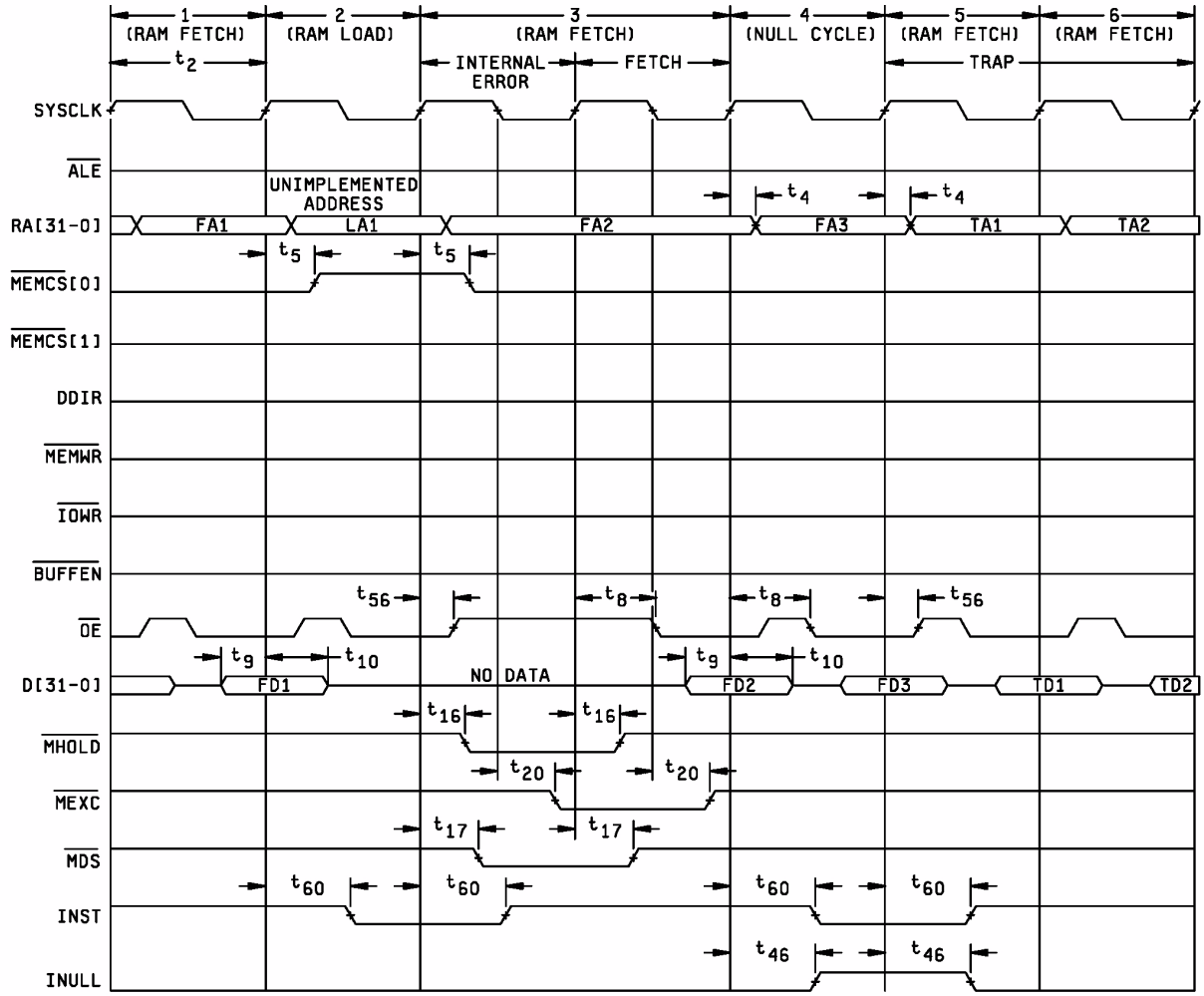
RAM LOAD WITH CORRECTABLE ERROR - 0 WAITSTATE



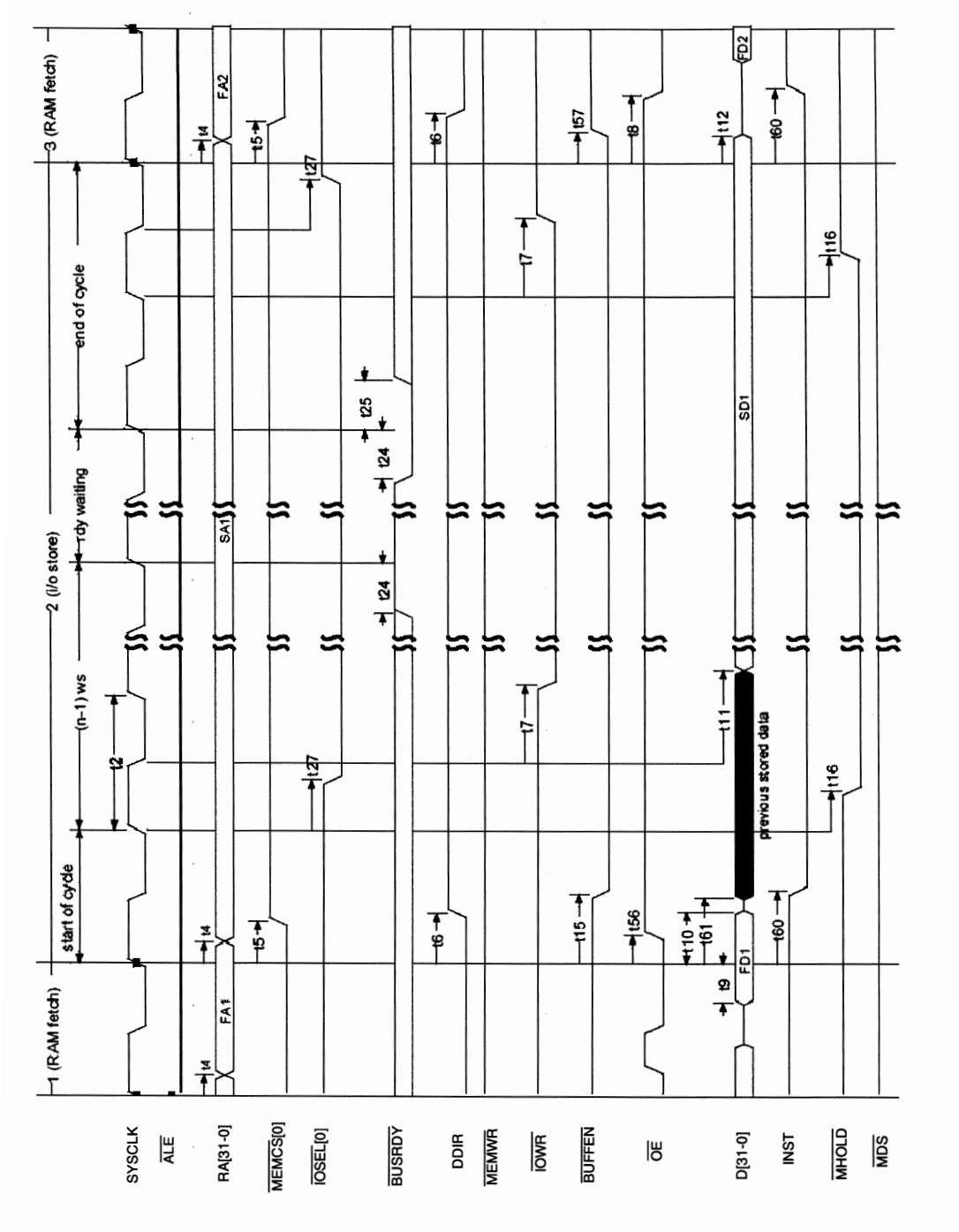
RAM LOAD WITH UNCORRECTABLE ERROR - 0 WAITSTATE



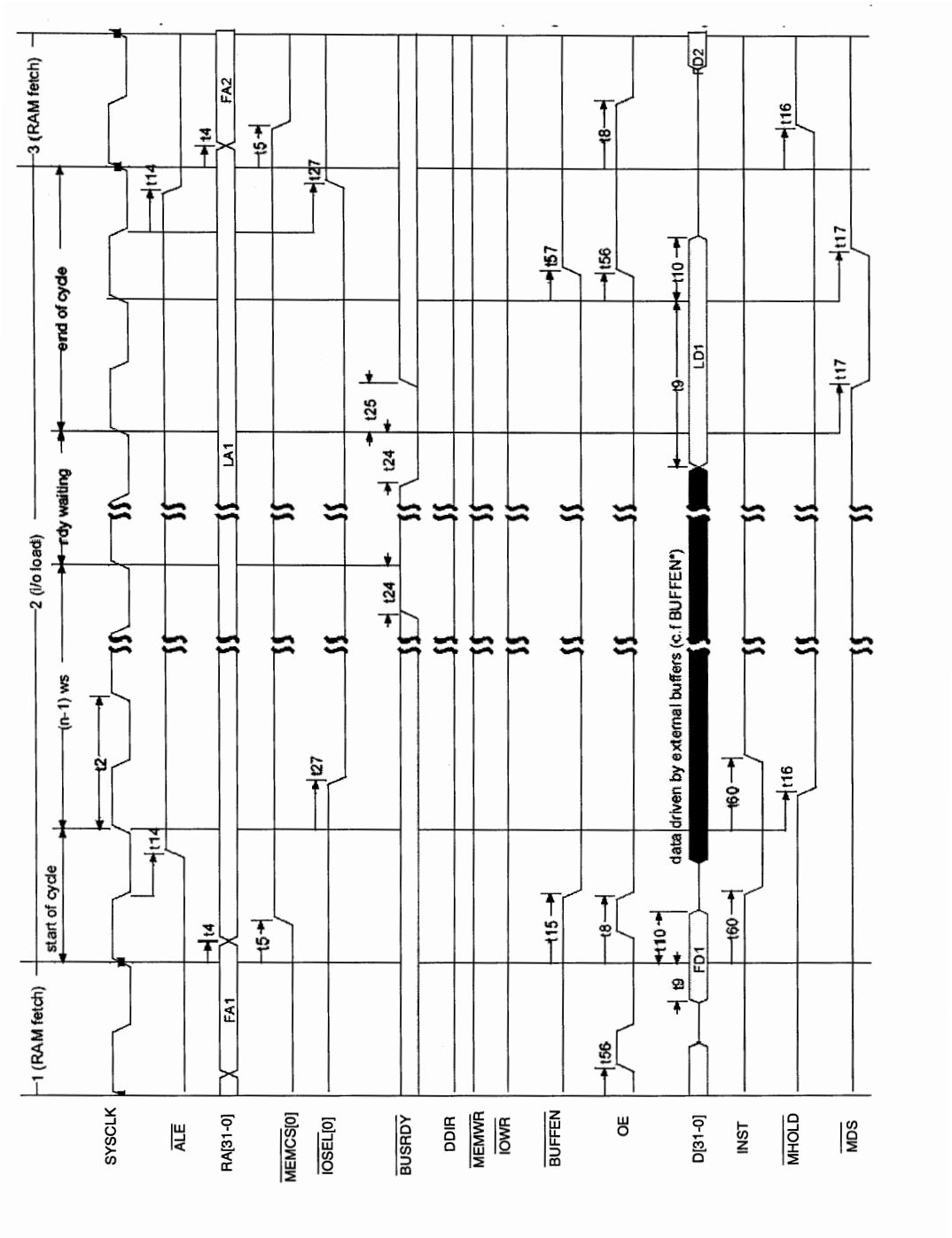
RAM LOAD WITH UNIMPLEMENTED AREA ACCESS - 0 WAISTSTATE



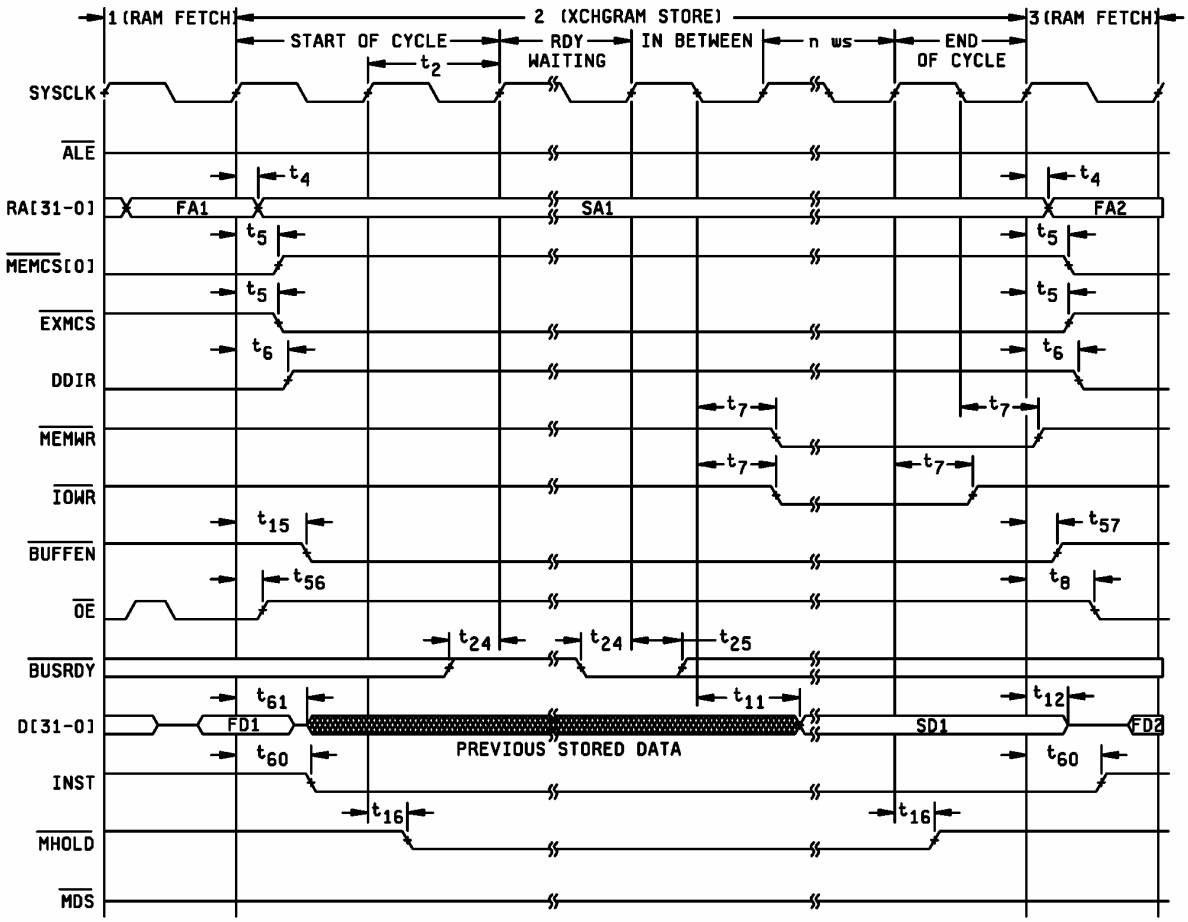
I/O STORE SEQUENCE WITH $\overline{\text{BUSRDY}}$ AND n WAITSTATES (TIMING FOR 0 WAITSTATE = TIMING FOR 1 WAITSTATE)



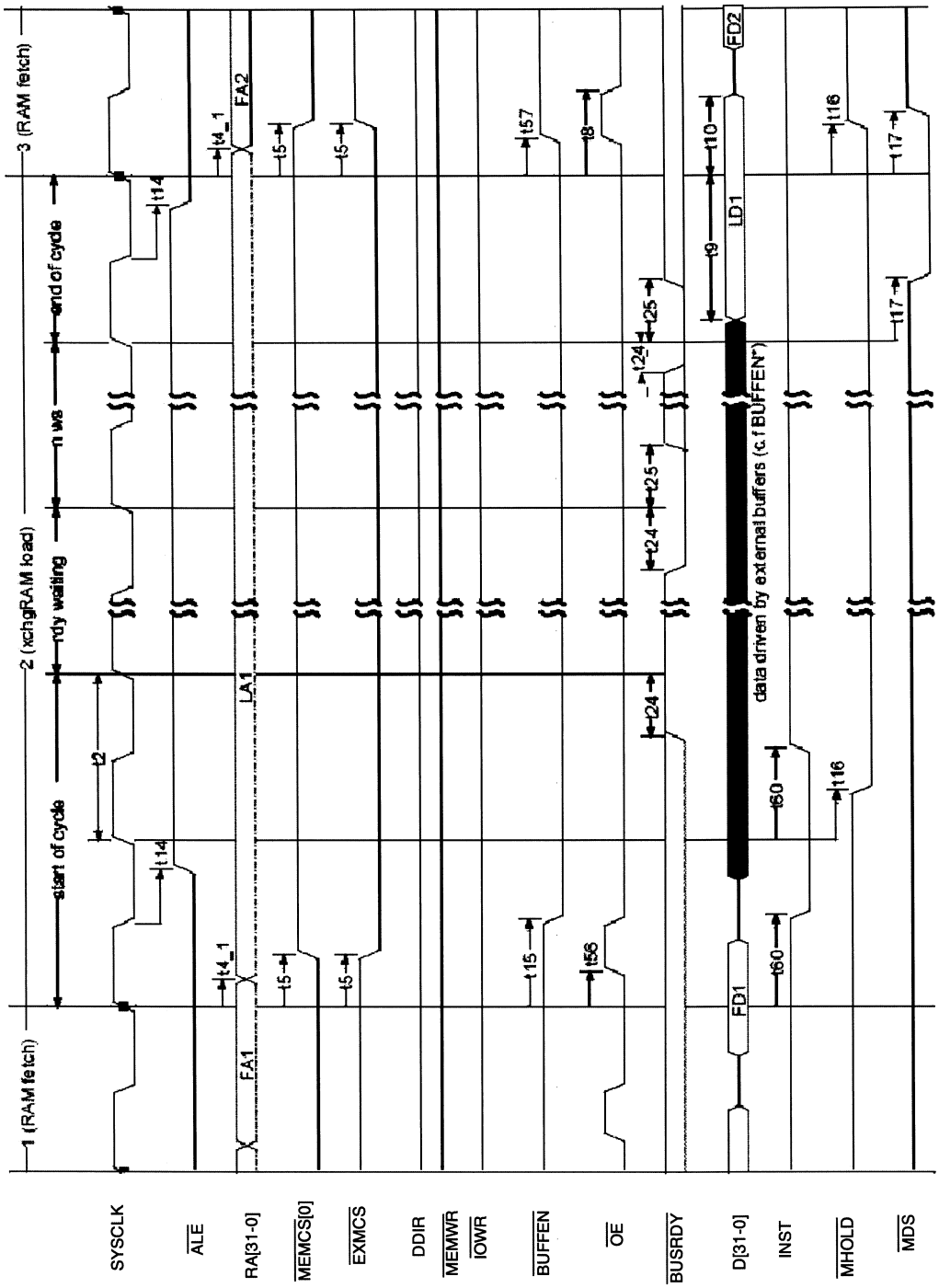
i/O LOAD SEQUENCE WITH $\overline{\text{BUSRDY}}$ AND n WAITSTATES (TIMING FOR 0 WAITSTATE = TIMING FOR 1 WAITSTATE)



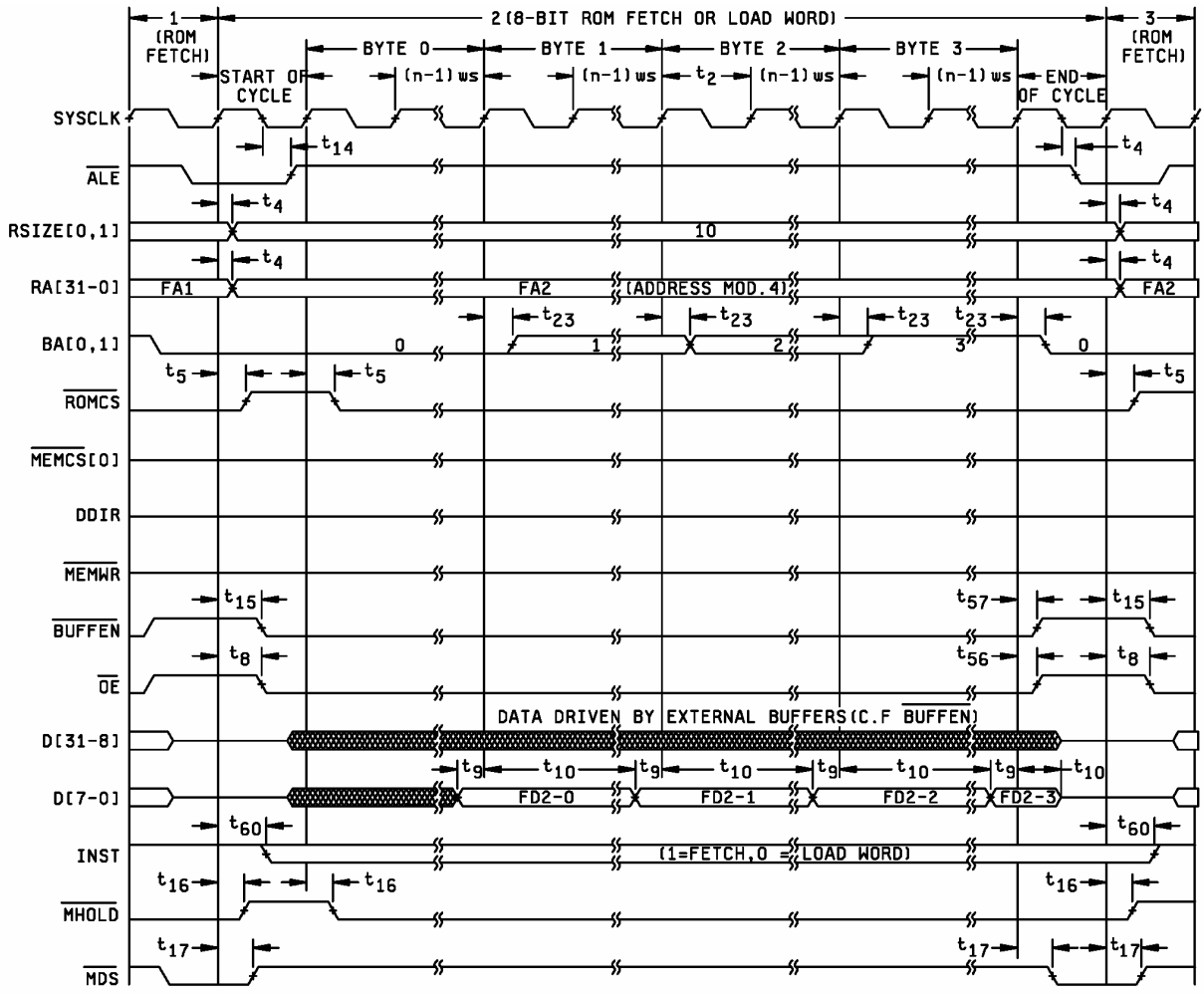
EXCHANGE RAM STORE WITH $\overline{\text{BUSRDY}}$ AND n WAITSTATES



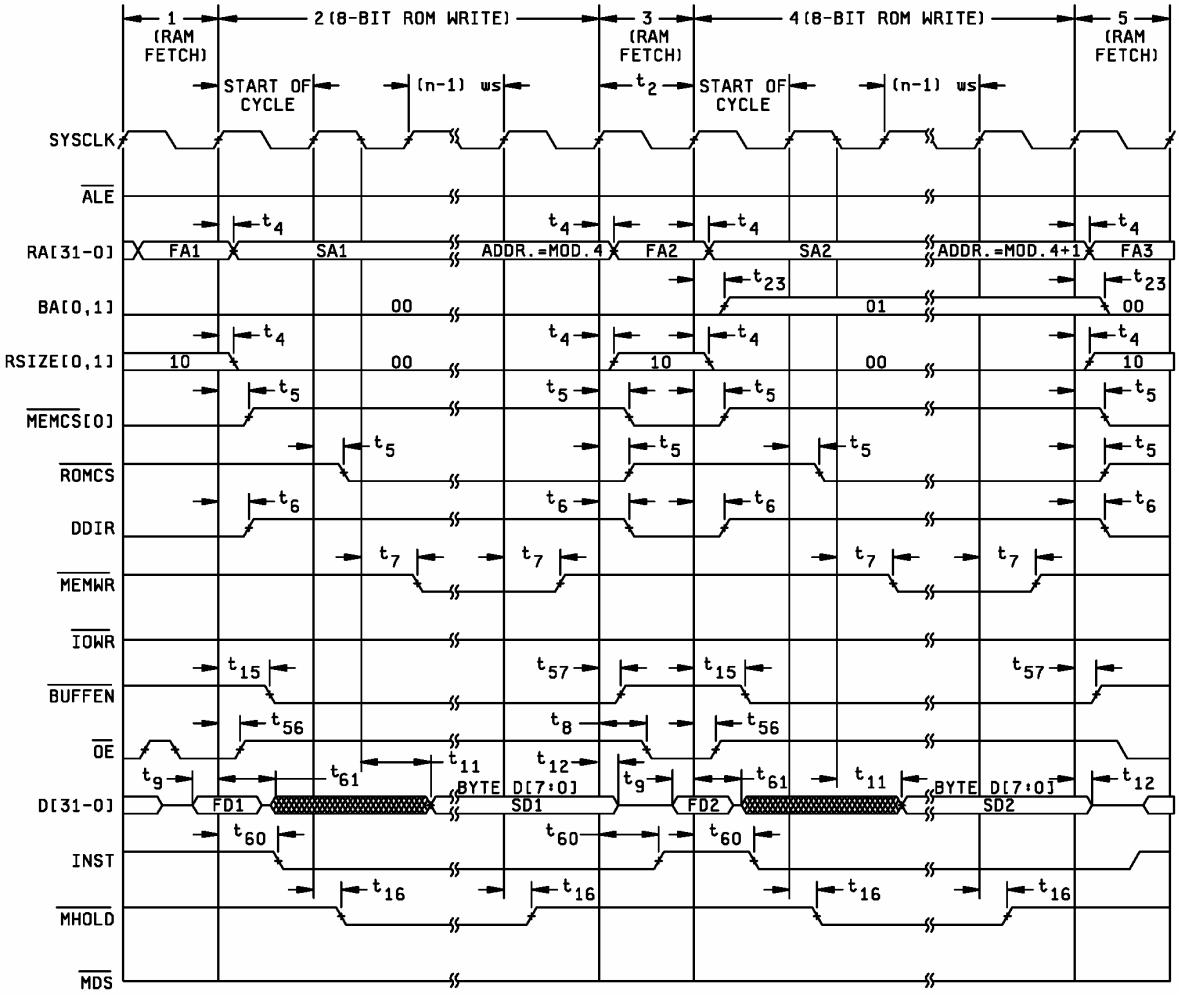
EXCHANGE RAM LOAD WITH $\overline{\text{BUSRDY}}$ AND n WAITSTATES



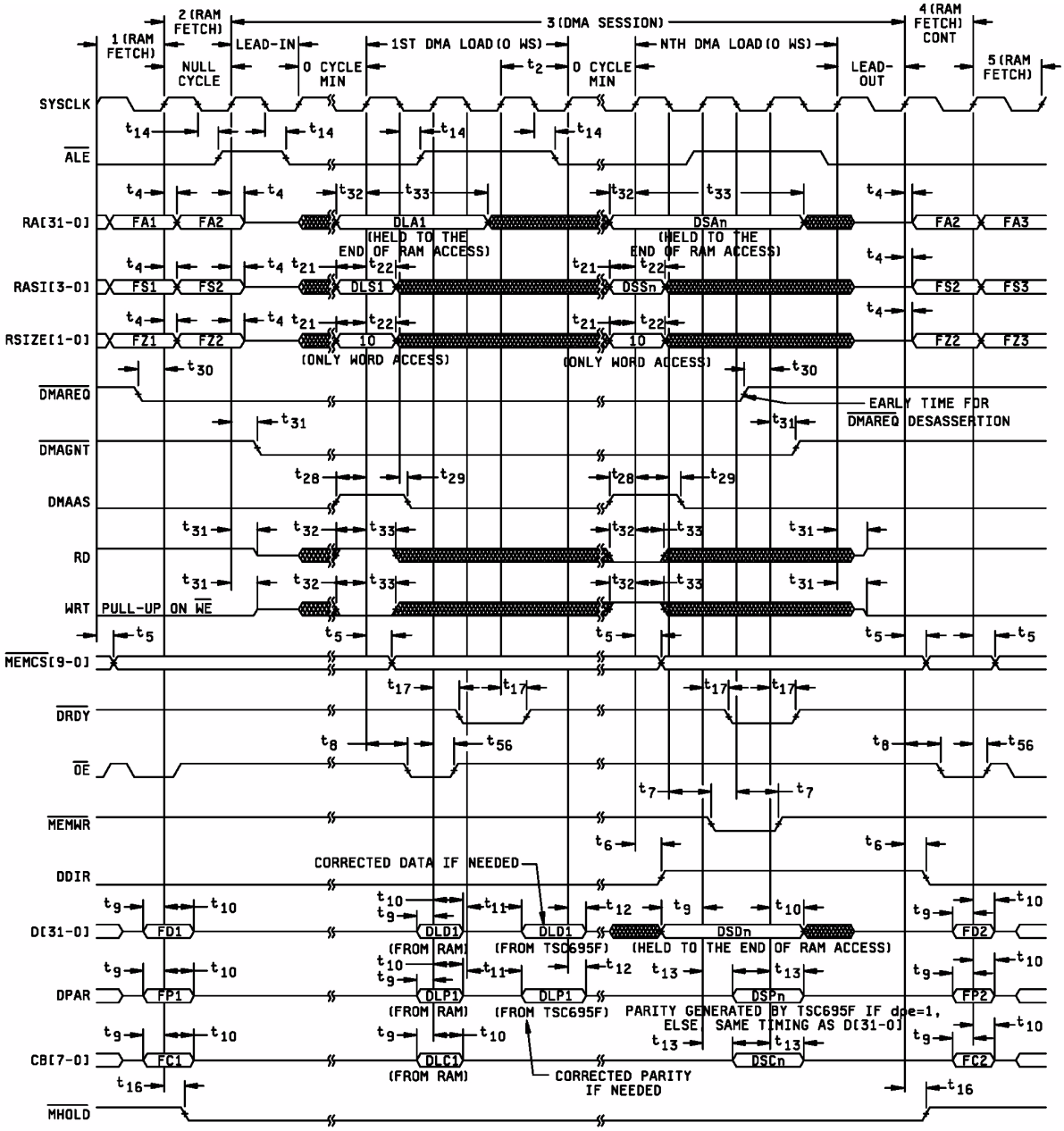
8-BIT BOOT FROM FETCH [OR LOAD WORD] - n WAITSTATES



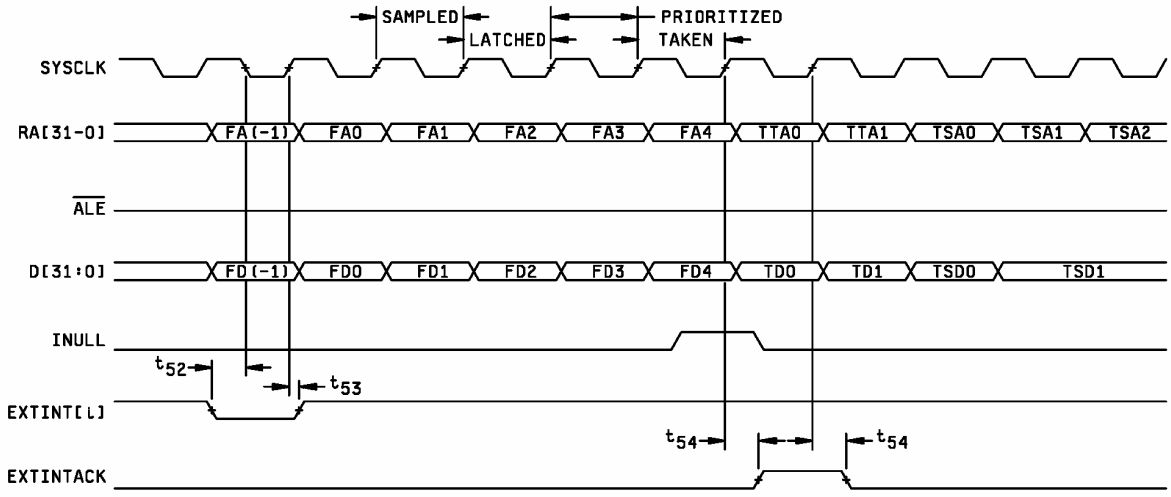
8-BIT BOOT PROM 2x STORE BYTE - n WAITSTATES



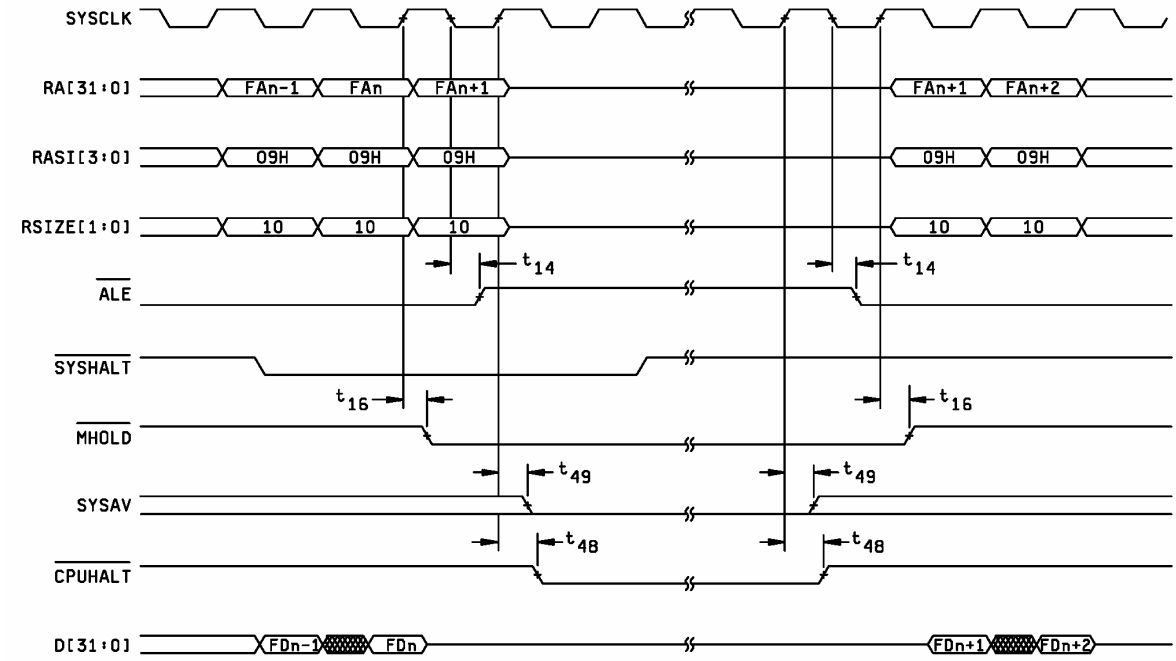
DMA RAM LOAD WITH OR WITHOUT CORRECTABLE ERROR AND DMA RAM STORE - 0 WAITSTATES



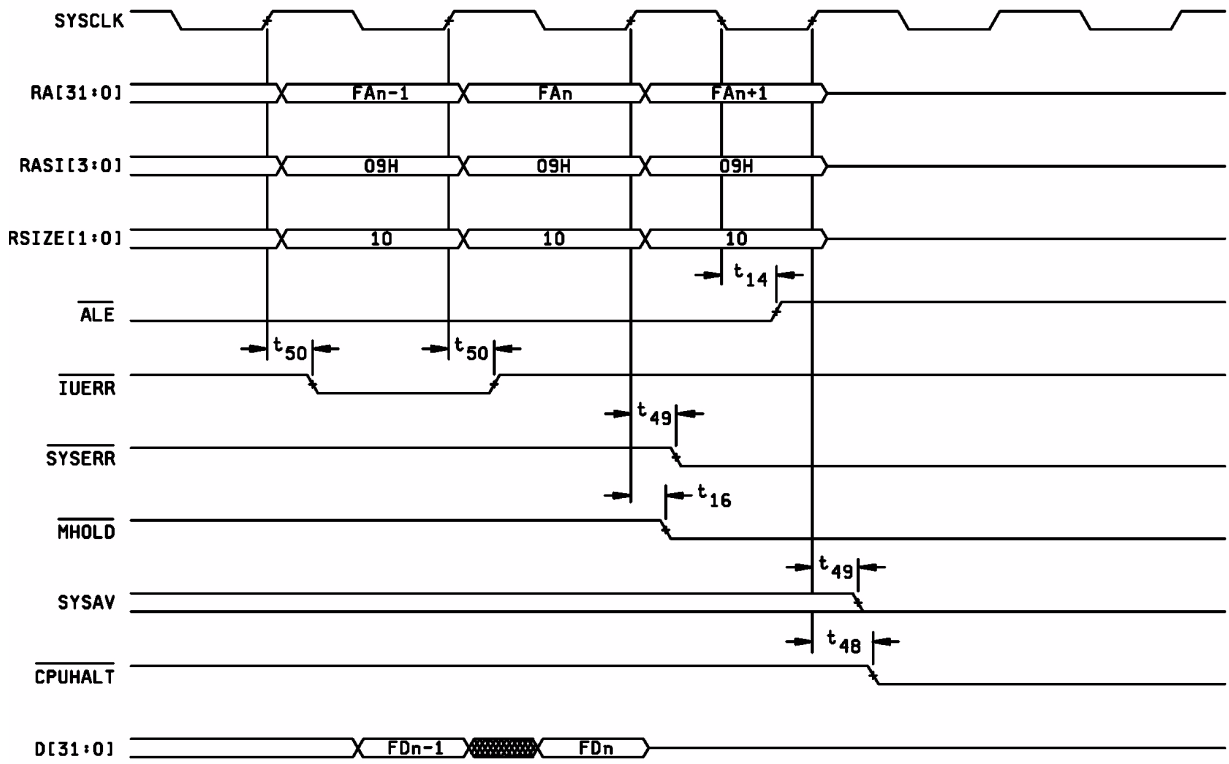
EDGE TRIGGERED INTERRUPT TIMING



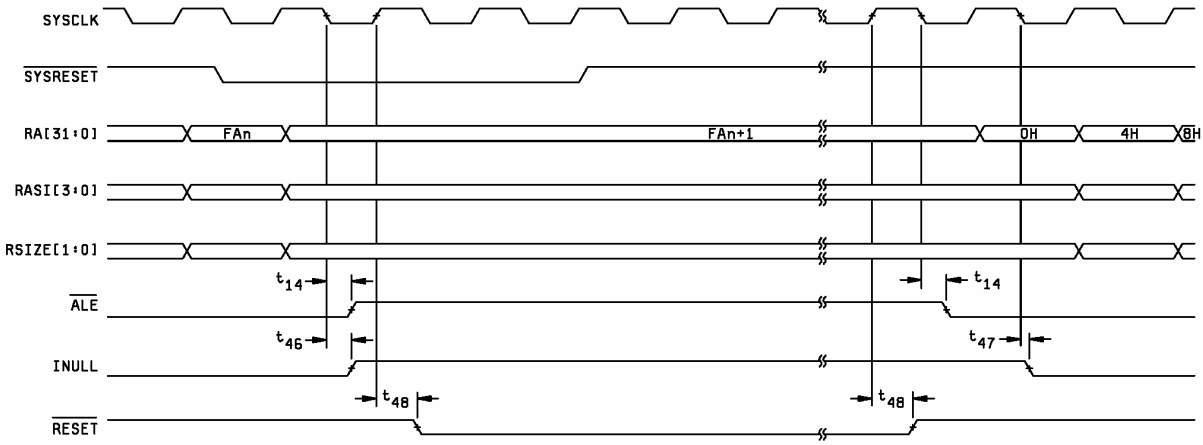
HALT TIMING



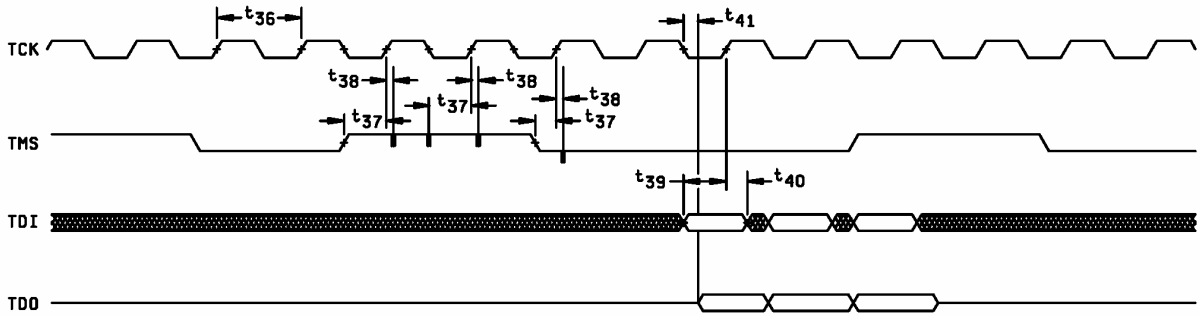
EXTERNAL ERROR WITH HALT TIMING



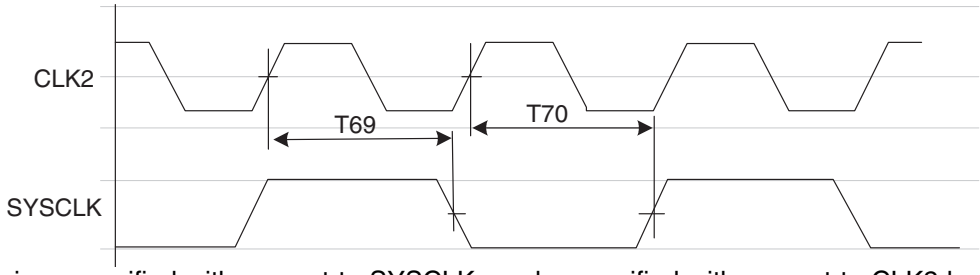
RESET TIMING



TMS, TDI, TDO TIMING

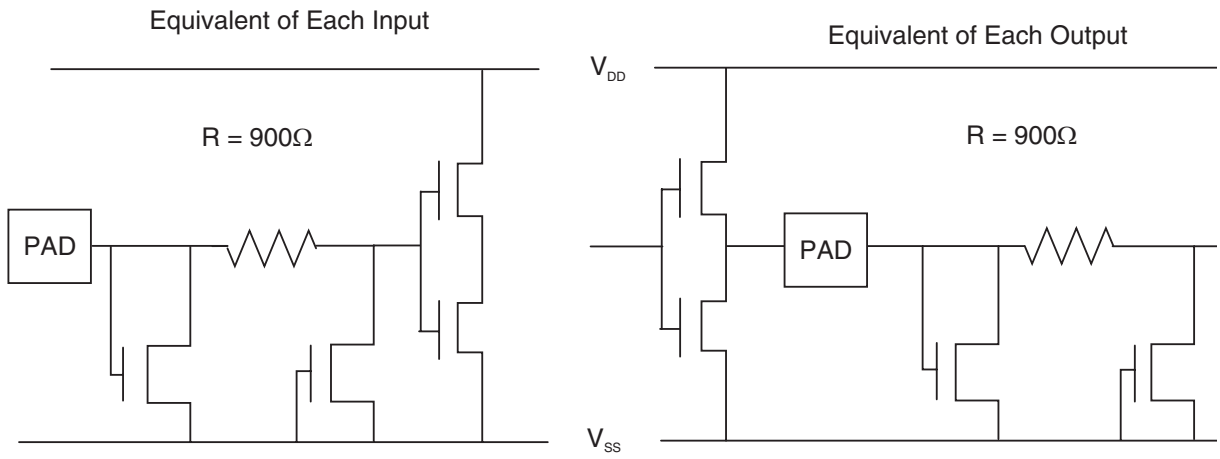


SYSCLK TO CLK2 TIMING



NOTE: Timings specified with respect to SYSCLK can be specified with respect to CLK2 by means of T69 and T70

1.11 PROTECTION NETWORKS



2. REQUIREMENTS

2.1 GENERAL

The complete requirements for procurement of the components specified herein are as stated in this specification and the applicable ESCC Generic Specification. Permitted deviations from the Generic

Specification, applicable to this specification only, are listed below.
Permitted deviations from the Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESCC requirement and do not affect the component's reliability, are listed in the appendices attached to this specification.

2.1.1 Deviations from the Generic Specification

2.1.1.1 Deviations from Screening Tests

(a) High Temperature Reverse Bias Burn-in and the subsequent Final Measurements for HTRB shall be omitted.

2.2 MARKING

The marking shall be in accordance with the requirements of ESCC Basic Specification No. 21700 and as follows.
The information to be marked on the component shall be:
(a) Terminal identification.
(b) The ESCC qualified components symbol (for ESCC qualified components only.)
(c) The ESCC Component Number.
(d) Traceability information.

2.3 ELECTRICAL MEASUREMENTS AT ROOM, HIGH AND LOW TEMPERATURES

Electrical measurements shall be performed at room, high and low temperatures.

2.3.1 Room Temperature Electrical Measurements

The measurements shall be performed at T_{amb} = +22 ±3°C.

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions (Note 1)	Limits		Units
				Min	Max	
Functional Test 1	-	3014	V_{IL}=0.8V,V_{IH1}=2.2V, V_{IH2}=3V V_{DD}=4.5V,V_{SS}=0V Note 2	-	-	-
Functional Test 2	-	3014	V_{IL}=0.8V,V_{IH1}=2.2V, V_{IH2}=3V V_{DD}=5V,V_{SS}=0V Note 2	-	-	-
Functional Test 3	-	3014	V_{IL}=0.8V,V_{IH1}=2.2V, V_{IH2}=3V V_{DD}=5.5V,V_{SS}=0V Note 2	-	-	-
Low Level Input Current 1	I_{IL1}	3009	V_{IN}=0V,V_{DD}=5.5V, V_{SS}=0V Note 3	-	-10	µA

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions (Note 1)	Limits		Units
				Min	Max	
Low Level Input Current 2	I_{IL2}	3009	V_{IN}=0V,V_{DD}=5.5V, V_{SS}=0V Note 3	-	-350	µA
High Level Input Current	I_{IH}	3010	V_{IN} = 5.5V, V_{DD}= 5.5V V_{SS}=0V	-	10	µA
Low Level Output Voltage 1	V_{OL1}	3007	V_{DD}=4.5V, V_{SS}=0V I_{OL}=4mA Note 4	-	400	mV
Low Level Output Voltage 2	V_{OL2}	3007	V_{DD}=4.5V, V_{SS}=0V I_{OL}=12mA Note 4	-	400	mV
High Level Output Voltage 1	V_{OH1}	3006	V_{DD}=4.5V, V_{SS}=0V I_{OH}=-6mA Note 4	2.4	-	V
High Level Output Voltage 2	V_{OH2}	3006	V_{DD}=4.5V, V_{SS}=0V I_{OH}=-16mA Note 4	2.4	-	V
Output Leakage Current Third State, Low Level Applied	I_{OZL}	3020	Outputs disabled V_{OUT}=0V, V_{DD}=5.5V V_{SS}=0V	-	-10	µA
Output Leakage Current Third State, High Level Applied	I_{OZH}	3021	Outputs disabled V_{OUT}=V_{DD}=5.5V V_{SS}=0V	-	10	µA
Supply Current, Power Down	I_{DDPD}	3005	V_{DD}=5.5V, V_{SS}=0V, f=25MHz V_{DDI} Pins Power Down mode	-	41	mA
Supply Current, Operating	I_{DDOP}	3005	V_{DD}=5.5V, V_{SS}=0V, f=25MHz V_{DDI} Pins	-	230	mA
Input Capacitance	C_{IN}	3012	V_{DD}=0V, V_{SS}=0V Note 5	-	7	pF
CLK2 period	T_1	3003	V_{DD}=4.5V and 5.5V, V_{SS}=0V Note 6	20	-	ns
SYSCLK Period	T_2	3003	V_{DD}=4.5V and 5.5V, V_{SS}=0V Note 6	40	-	ns
CLK2 High and Low Pulse Width	T_3	3003	V_{DD}=4.5V and 5.5V, V_{SS}=0V Note 6	9.75	-	ns

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions (Note 1)	Limits		Units
				Min	Max	
RA[31-0], RAPAR, RSIZE, RLDSTO and LOCK Output Delay from SYSCLK + Edge	T_4	3003	V_{DD}=4.5V and 5.5V, V_{SS}=0V Note 7	-	6.5	ns
$\overline{\text{MEMCS}}$[9-0], $\overline{\text{ROMCS}}$, $\overline{\text{EXMCS}}$ Output Delay from SYSCLK + Edge	T_5	3003	V_{DD}=4.5V and 5.5V, V_{SS}=0V Note 6	-	12.5	ns
DDIR, $\overline{\text{DDIR}}$ Output Delay from SYSCLK + Edge	T_6	3003	V_{DD}=4.5V and 5.5V, V_{SS}=0V Note 6	-	15	ns
$\overline{\text{MEMWR}}$ and $\overline{\text{IOWR}}$ Output Delay from SYSCLK + and SYSCLK - Edge	T_7	3003	V_{DD}=4.5V and 5.5V, V_{SS}=0V Note 7	-	23.5	ns
$\overline{\text{OE}}$ High to Low Output Delay from SYSCLK + Edge	T_8	3003	V_{DD}=4.5V and 5.5V, V_{SS}=0V Note 7	-	20.5	ns
Data Setup Time during Load from SYSCLK + Edge	T_{9-1}	3003	V_{DD}=4.5V and 5.5V, V_{SS}=0V Note 6	11.5	-	ns
Data Setup Time during Load from SYSCLK + Edge	T_{9-2}	3003	V_{DD}=4.5V and 5.5V, V_{SS}=0V Note 7, 8	9	-	ns
Data Hold Time during Load from SYSCLK + Edge	T_{10}	3003	V_{DD}=4.5V and 5.5V, V_{SS}=0V Note 6	5	-	ns
Data Output Delay from SYSCLK- Edge	T_{11}	3003	V_{DD}=4.5V and 5.5V, V_{SS}=0V Note 7	-	28	ns
Data Output Valid from SYSCLK + Edge	T_{12}	3003	V_{DD}=4.5V and 5.5V, V_{SS}=0V Note 6	8	-	ns
CB Output Delay from SYSCLK + Edge	T_{13}	3003	V_{DD}=4.5V and 5.5V, V_{SS}=0V Note 6	-	19	ns
$\overline{\text{ALE}}$ Output Delay From SYSCLK- Edge	T_{14}	3003	V_{DD}=4.5V and 5.5V, V_{SS}=0V Note 6	-	13	ns
$\overline{\text{BUFFEN}}$ High to Low Output Delay from SYSCLK + Edge	T_{15}	3003	V_{DD}=4.5V and 5.5V, V_{SS}=0V Note 7	-	21	ns

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions (Note 1)	Limits		Units
				Min	Max	
$\overline{\text{MHOLD}}$ Output Delay from SYSCLK + Edge	T_{16}	3003	V_{DD}=4.5V and 5.5V, V_{SS}=0V Note 6	-	12	ns
$\overline{\text{MDS}}$, $\overline{\text{DRDY}}$ Output Delay from SYSCLK + Edge	T_{17}	3003	V_{DD}=4.5V and 5.5V, V_{SS}=0V Note 6	-	15	ns
$\overline{\text{MEXC}}$ Output Delay from SYSCLK-Edge	T_{20}	3003	V_{DD}=4.5V and 5.5V, V_{SS}=0V Note 6	-	15	ns
RASI[3-0], RSIZE[1-0], RASPAR Setup Time from SYSCLK + Edge	T_{21}	3003	V_{DD}=4.5V and 5.5V, V_{SS}=0V Note 6	10	-	ns
RASI[3-0], RSIZE[1-0], RASPAR Hold Time from SYSCLK + Edge	T_{22}	3003	V_{DD}=4.5V and 5.5V, V_{SS}=0V Note 6	3	-	ns
BOOT PROM Address Output Delay from SYSCLK + Edge	T_{23}	3003	V_{DD}=4.5V and 5.5V, V_{SS}=0V Note 6	-	13	ns
$\overline{\text{BUSRDY}}$ Setup Time from SYSCLK + Edge	T_{24}	3003	V_{DD}=4.5V and 5.5V, V_{SS}=0V Note 6	12	-	ns
$\overline{\text{BUSRDY}}$ Hold Time SYSCLK + Edge	T_{25}	3003	V_{DD}=4.5V and 5.5V, V_{SS}=0V Note 6	0	-	ns
$\overline{\text{IOSEL}}$[3-0] Output Delay from SYSCLK + Edge	T_{27}	3003	V_{DD}=4.5V and 5.5V, V_{SS}=0V Note 6	-	15	ns
DMAAS Setup Time from SYSCLK + Edge	T_{28}	3003	V_{DD}=4.5V and 5.5V, V_{SS}=0V Note 6	12	20	ns
DMAAS Hold Time from SYSCLK-Edge	T_{29}	3003	V_{DD}=4.5V and 5.5V, V_{SS}=0V Note 6	0	20	ns
$\overline{\text{DMAREQ}}$ Setup Time from SYSCLK + Edge	T_{30}	3003	V_{DD}=4.5V and 5.5V, V_{SS}=0V Note 6	12	-	ns
$\overline{\text{DMAGNT}}$ Output Delay from SYSCLK + Edge	T_{31}	3003	V_{DD}=4.5V and 5.5V, V_{SS}=0V Note 6	-	15	ns

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions (Note 1)	Limits		Units
				Min	Max	
RA[31-0], RAPAR, CPAR Setup Time from SYSCLK + Edge	T_{32}	3003	V_{DD}=4.5V and 5.5V, V_{SS}=0V Note 6	10	-	ns
RA[31-0], RAPAR, CPAR Hold TIme from SYSCLK + Edge	T_{33}	3003	V_{DD}=4.5V and 5.5V, V_{SS}=0V Note 6	3	-	ns
TCK Period	T_{36}	3003	V_{DD}=4.5V and 5.5V, V_{SS}=0V Note 6	100	-	ns
TMS Setup Time from TCK + Edge	T_{37}	3003	V_{DD}=4.5V and 5.5V, V_{SS}=0V Note 6	10	-	ns
TMS Hold Time from TCK + Edge	T_{38}	3003	V_{DD}=4.5V and 5.5V, V_{SS}=0V Note 6	4	-	ns
TDI Setup Time from TCK + Edge	T_{39}	3003	V_{DD}=4.5V and 5.5V, V_{SS}=0V Note 6	10	-	ns
TDI Hold Time from TCK + Edge	T_{40}	3003	V_{DD}=4.5V and 5.5V, V_{SS}=0V Note 6	10	-	ns
TDO Output Delay from TCK-Edge	T_{41}	3003	V_{DD}=4.5V and 5.5V, V_{SS}=0V Note 6	-	20	ns
INULL Output Delay from SYSCLK + Edge	T_{46}	3003	V_{DD}=4.5V and 5.5V, V_{SS}=0V Note 6	-	22	ns
$\overline{\text{RESET}}$, $\overline{\text{CPUHALT}}$ Output Delay from SYSCLK + Edge	T_{48}	3003	V_{DD}=4.5V and 5.5V, V_{SS}=0V Note 6	-	22	ns
SYSERR, SYSAV Output Delay from SYSCLK + Edge	T_{49}	3003	V_{DD}=4.5V and 5.5V, V_{SS}=0V Note 6	-	20	ns
$\overline{\text{IUERR}}$ Output Delay from SYSCLK + Edge	T_{50}	3003	V_{DD}=4.5V and 5.5V, V_{SS}=0V Note 6	-	20	ns
EXTINT[4-0] Setup Time from SYSCKL-Edge	T_{52}	3003	V_{DD}=4.5V and 5.5V, V_{SS}=0V Note 6	12	-	ns
EXTINT[4-0] Hold Time from SYSCKL-Edge	T_{53}	3003	V_{DD}=4.5V and 5.5V, V_{SS}=0V Note 6	0	-	ns

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions (Note 1)	Limits		Units
				Min	Max	
EXTINTACK Output Delay from SYSCLK + Edge	T_{54}	3003	V_{DD}=4.5V and 5.5V, V_{SS}=0V Note 6	-	15	ns
$\overline{OE}$ Low to High Output Delay from SYSCLK + Edge (no DMA Mode)	T_{56}	3003	V_{DD}=4.5V and 5.5V, V_{SS}=0V Note 6	-	8.5	ns
$\overline{BUFFEN}$ Low to High Output Delay from SYSCLK + Edge	T_{57}	3003	V_{DD}=4.5V and 5.5V, V_{SS}=0V Note 6	-	9	ns
INST Output Delay from SYSCLK + Edge	T_{60}	3003	V_{DD}=4.5V and 5.5V, V_{SS}=0V Note 6	-	22	ns
Data Output Delay to Low-Z from SYSCLK + Edge	T_{61}	3003	V_{DD}=4.5V and 5.5V, V_{SS}=0V Note 6	20	-	ns

NOTES:

1. Unless otherwise specified all inputs and outputs shall be tested for each characteristic.
2. Functional tests shall be performed at each supply voltage with f_{SYSCLK} = 25MHz, $t_r = t_f \leq 5$ns, V_{IL} = 0.8V, V_{IH1} = 2.2V, V_{IH2} = 3V, $V_{OL} \leq 1.45$V, $V_{OH} \geq 1.55$V.
   V_{IH2} applies to inputs RxA/RxB, GPI[7-0], EXTINT[4-0], EWDINT, $\overline{SYSRESET}$. V_{IH1} applies to all other inputs.
   Functionality per the timing diagrams specified herein shall be verified.
3. I_{L2} applies to inputs $\overline{TRST}$, TMS, TDI, I_{L1} applies to all other inputs.
4. V_{OL2} and V_{OH2} apply to outputs RA[31-0], $\overline{MEMCS}$[9-0], $\overline{MEMWR}$, $\overline{OE}$. V_{OL1} and V_{OH1} apply to all other outputs.
5. Guaranteed but not tested.
6. Parameter tested go-no-go at each supply voltage during AC testing with f_{SYSCLK} = 25MHz, C_L = 50pF, V_{ref} = 2.5V.
7. Parameter recorded at each supply voltage during AC testing with f_{SYSCLK} =25MHz, C_L = 50pF, V_{ref} = 2.5V.
8. Parameter tested with following conditions: NOPAR = 0, rpa = rec = 0 or 1
   (NOPAR: No Parity Input Signal; rpa, rec: bit 13 and 14 of Memory Configuration Register)

2.3.2 High and Low Temperatures Electrical Measurements

The measurements shall be performed at T_{amb} = +125(+0 -5)°C and T_{amb} = -55(+5 -0)°C.
The characteristics, test methods, conditions and limits shall be the same as specified for Room Temperature Electrical Measurements.

2.4 PARAMETER DRIFT VALUES

Unless otherwise specified, the measurements shall be performed at T_{amb} = +22 ±3°C.
The test methods and test conditions shall be as per the corresponding test defined in Room Temperature Electrical Measurements.
The drift values (Δ) shall not be exceeded for each characteristic specified. The corresponding absolute limit values for each characteristic shall not be exceeded.

Characteristics	Symbols	Limits			Units
		Drift Value Δ	Absolute		
			Min	Max	
Low Level Input Current 1	I_{IL1}	±0.1	-	-10	µA
High Level Input Current	I_{IH}	±0.1	-	10	µA
Low Level Output Voltage 1	V_{OL1}	±100	-	400	mV
Low Level Output Voltage 2	V_{OH2}	±100	-	400	mV
High Level Output Voltage 1	V_{OH1}	±0.1	2.4	-	V
High Level Output Voltage 2	V_{OH2}	±0.1	2.4	-	V
Output Leakage Current Third State, Low Level Applied	I_{OZL}	±0.1	-	-10	µA
Output Leakage Current Third State, High Level Applied	I_{OZH}	±0.1	-	10	µA

NOTES:
Unless otherwise specified all inputs and outputs shall be tested for each characteristic.

2.5 INTERMEDIATE AND END-POINT ELECTRICAL MEASUREMENTS

Unless otherwise specified, the measurements shall be performed at T_{amb} = +22 ±3°C.
The characteristics, test methods, conditions and limits shall be the same as specified for Room Temperature Electrical Measurements.

2.6 POWER BURN-IN CONDITIONS

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	T_{amb}	+125(+0, -3)	°C
Input CLK2	V_{IN}	V_{GEN1} (Note 1)	V
Input $\overline{\text{SYSRESET}}$	V_{IN}	V_{GEN2} (Note 1)	V
All other Inputs and Outputs	V_{IN}, V_{OUT}	V_{DD}, V_{SS} (Note 1)	V
Pulse Voltage	V_{GEN1} V_{GEN2}	0V to V_{DD}	V
Pulse Frequency Square Wave	f_{GEN1} f_{GEN2}	1.65M 50.3 (Note 2) 50± 15% Duty Cycle $t_r = t_f \leq 5$ns	Hz
Positive Supply Voltage V_{DDO}, V_{DDI}	V_{DD}	5(+0.5, -0)	V
Negative Supply Voltage V_{SSO}, V_{SSI}	V_{SS}	0	V

NOTES:

1. All Inputs and Outputs shall be connected through a serial protection resistor/load as follows:

Pin	Signal	Wired to:	Serial Resistor
1	GPINNT	V_{DD}	5.6kΩ
2	GPI[7]	V_{DD}	1kΩ
3	V_{DDO}	V_{DD}	N/A
4	V_{SSO}	V_{SS}	N/A
5	GPI[6]	V_{DD}	1kΩ
6	GPI[5]	V_{DD}	1kΩ
7	GPI[4]	V_{DD}	1kΩ
8	GPI[3]	V_{DD}	1kΩ
9	V_{DDO}	V_{DD}	N/A
10	V_{SSO}	V_{SS}	N/A
11	GPI[2]	V_{DD}	1kΩ
12	GPI[1]	V_{DD}	1kΩ
13	GPI[0]	V_{DD}	1kΩ
14	D[31]	V_{DD}	1kΩ
15	D[[30]	V_{DD}	1kΩ
16	V_{DDO}	V_{DD}	N/A
17	V_{SSO}	V_{SS}	N/A
18	D[29]	V_{SS}	1kΩ
19	D[28]	V_{SS}	1kΩ
20	V_{DDI}	V_{DD}	N/A
21	V_{SSI}	V_{SS}	N/A
22	D[27]	V_{SS}	1kΩ
23	D[26]	V_{DD}	1kΩ
24	V_{DDO}	V_{DD}	N/A
25	V_{SSO}	V_{SS}	N/A
26	D[25]	V_{SS}	1kΩ
27	D[24]	V_{SS}	1kΩ
28	D[23]	V_{DD}	1kΩ
29	D[22]	V_{SS}	1kΩ
30	V_{DDO}	V_{DD}	N/A
31	V_{SSO}	V_{SS}	N/A
32	D[21]	V_{SS}	1kΩ
33	D[20]	V_{DD}	1kΩ
34	D[19]	V_{DD}	1kΩ

Pin	Signal	Wired to:	Serial Resistor
35	D[18]	V_{SS}	1kΩ
36	V_{DDO}	V_{DD}	N/A
37	V_{SSO}	V_{SS}	N/A
38	D[17]	V_{SS}	1kΩ
39	D[16]	V_{SS}	1kΩ
40	V_{DDI}	V_{DD}	N/A
41	V_{SSI}	V_{SS}	N/A
42	D[15]	V_{SS}	1kΩ
43	D[14]	V_{SS}	1kΩ
44	V_{DDO}	V_{DD}	N/A
45	V_{SSO}	V_{SS}	N/A
46	D[13]	V_{SS}	1kΩ
47	D[12]	V_{SS}	1kΩ
48	D[11]	V_{SS}	1kΩ
49	D[10]	V_{SS}	1kΩ
50	V_{DDO}	V_{DD}	N/A
51	V_{SSO}	V_{SS}	N/A
52	D[9]	V_{SS}	1kΩ
53	D[8]	V_{DD}	1kΩ
54	D[7]	V_{SS}	1kΩ
55	D[6]	V_{SS}	1kΩ
56	V_{DDO}	V_{DD}	N/A
57	V_{SSO}	V_{SS}	N/A
58	D[5]	V_{DD}	1kΩ
59	D[4]	V_{SS}	1kΩ
60	D[3]	V_{SS}	1kΩ
61	D[2]	V_{SS}	1kΩ
62	V_{DDO}	V_{DD}	N/A
63	V_{SSO}	V_{SS}	N/A
64	D[1]	V_{SS}	1kΩ
65	D[0]	V_{SS}	1kΩ
66	RSIZE[1]	V_{DD}	5.6kΩ
67	RSIZE[0]	V_{DD}	5.6kΩ
68	RASI[3]	V_{DD}	5.6kΩ
69	V_{DDO}	V_{DD}	N/A
70	V_{SSO}	V_{SS}	N/A

Pin	Signal	Wired to:	Serial Resistor
71	RASI[2]	V_{DD}	5.6kΩ
72	RASI[1]	V_{DD}	5.6kΩ
73	RASI[0]	V_{DD}	5.6kΩ
74	RA[31]	V_{DD}	5.6kΩ
75	RA[30]	V_{DD}	5.6kΩ
76	V_{DDO}	V_{DD}	N/A
77	V_{SSO}	V_{SS}	N/A
78	RA[29]	V_{DD}	5.6kΩ
79	RA[28]	V_{DD}	5.6kΩ
80	RA[27]	V_{DD}	5.6kΩ
81	V_{DDO}	V_{DD}	N/A
82	V_{SSO}	V_{SS}	N/A
83	RA[26]	V_{DD}	5.6kΩ
84	RA[25]	V_{DD}	5.6kΩ
85	RA[24]	V_{DD}	5.6kΩ
86	V_{DDI}	V_{DD}	N/A
87	V_{SSI}	V_{SS}	N/A
88	V_{DDO}	V_{DD}	N/A
89	V_{SSO}	V_{SS}	N/A
90	RA[23]	V_{DD}	5.6kΩ
91	RA[22]	V_{DD}	5.6kΩ
92	RA[21]	V_{DD}	5.6kΩ
93	V_{DDO}	V_{DD}	N/A
94	V_{SSO}	V_{SS}	N/A
95	RA[20]	V_{DD}	5.6kΩ
96	RA[19]	V_{DD}	5.6kΩ
97	RA[18]	V_{DD}	5.6kΩ
98	V_{DDO}	V_{DD}	N/A
99	V_{SSO}	V_{SS}	N/A
100	RA[17]	V_{DD}	5.6kΩ
101	RA[16]	V_{DD}	5.6kΩ
102	RA[15]	V_{DD}	5.6kΩ
103	V_{DDO}	V_{DD}	N/A
104	V_{SSO}	V_{SS}	N/A
105	RA[14]	V_{DD}	5.6kΩ
106	V_{DDI}	V_{DD}	N/A

Pin	Signal	Wired to:	Serial Resistor
107	V_{SSI}	V_{SS}	N/A
108	RA[13]	V_{DD}	5.6kΩ
109	RA[12]	V_{DD}	5.6kΩ
110	V_{DDO}	V_{DD}	N/A
111	V_{SSO}	V_{SS}	N/A
112	RA[11]	V_{DD}	5.6kΩ
113	RA[10]	V_{DD}	5.6kΩ
114	RA[9]	V_{DD}	5.6kΩ
115	V_{DDO}	V_{DD}	N/A
116	V_{SSO}	V_{SS}	N/A
117	RA[8]	V_{DD}	5.6kΩ
118	RA[7]	V_{DD}	5.6kΩ
119	RA[6]	V_{DD}	5.6kΩ
120	V_{DDO}	V_{DD}	N/A
121	V_{SSO}	V_{SS}	N/A
122	RA[5]	V_{DD}	5.6kΩ
123	RA[4]	V_{DD}	5.6kΩ
124	RA[3]	V_{DD}	5.6kΩ
125	V_{DDO}	V_{DD}	N/A
126	V_{SSO}	V_{SS}	N/A
127	RA[2]	V_{DD}	5.6kΩ
128	RA[1]	V_{DD}	5.6kΩ
129	RA[0]	V_{DD}	5.6kΩ
130	V_{DDO}	V_{DD}	N/A
131	V_{SSO}	V_{SS}	N/A
132	RAPAR	V_{DD}	5.6kΩ
133	RASPAR	V_{DD}	5.6kΩ
134	DPAR	V_{DD}	1kΩ
135	V_{DDO}	V_{DD}	N/A
136	V_{SSO}	V_{SS}	N/A
137	SYSCLK	V_{DD}	5.6kΩ
138	TDO	V_{DD}	5.6kΩ
139	$\overline{\text{TRST}}$	V_{SS}	1kΩ
140	TMS	V_{DD}	1kΩ
141	TDI	V_{DD}	1kΩ
142	TCK	V_{DD}	1kΩ

Pin	Signal	Wired to:	Serial Resistor
143	CLK2	V_{GEN1}	1kΩ
144	$\overline{DRDY}$	V_{DD}	5.6kΩ
145	DMAAS	V_{SS}	1kΩ
146	V_{DDO}	V_{DD}	N/A
147	V_{SSO}	V_{SS}	N/A
148	$\overline{DMAGNT}$	V_{DD}	5.6kΩ
149	$\overline{EXMCS}$	V_{DD}	5.6kΩ
150	V_{DDI}	V_{DD}	N/A
151	V_{SSI}	V_{SS}	N/A
152	$\overline{DMAREQ}$	V_{DD}	1kΩ
153	$\overline{BUSERR}$	V_{DD}	1kΩ
154	$\overline{BUSRDY}$	V_{DD}	1kΩ
155	$\overline{ROMWRT}$	V_{DD}	1kΩ
156	$\overline{NOPAR}$	V_{SS}	1kΩ
157	$\overline{SYSHALT}$	V_{DD}	1kΩ
158	$\overline{CPUHALT}$	V_{DD}	5.6kΩ
159	V_{DDO}	V_{DD}	N/A
160	V_{SSO}	V_{SS}	N/A
161	SYSERR	V_{DD}	5.6kΩ
162	SYSAV	V_{DD}	5.6kΩ
163	EXTINT[4]	V_{DD}	1kΩ
164	EXTINT[3]	V_{DD}	1kΩ
165	EXTINT[2]	V_{DD}	1kΩ
166	EXTINT[1]	V_{DD}	1kΩ
167	EXTINT[0]	V_{DD}	1kΩ
168	V_{DDI}	V_{DD}	N/A
169	V_{SSI}	V_{SS}	N/A
170	EXTINTACK	V_{DD}	5.6kΩ
171	$\overline{IUERR}$	V_{DD}	5.6kΩ
172	V_{DDO}	V_{DD}	N/A
173	V_{SSO}	V_{SS}	N/A
174	CPAR	V_{DD}	5.6kΩ
175	TXA	V_{DD}	5.6kΩ
176	RXA	V_{DD}	1kΩ
177	RXB	V_{DD}	1kΩ
178	TXB	V_{DD}	5.6kΩ

Pin	Signal	Wired to:	Serial Resistor
179	$\overline{\text{IOWR}}$	V_{DD}	5.6kΩ
180	$\overline{\text{IOSEL}}$[3]	V_{DD}	5.6kΩ
181	V_{DDO}	V_{DD}	N/A
182	V_{SSO}	V_{SS}	N/A
183	$\overline{\text{IOSEL}}$[2]	V_{DD}	5.6kΩ
184	$\overline{\text{IOSEL}}$[1]	V_{DD}	5.6kΩ
185	$\overline{\text{IOSEL}}$[0]	V_{DD}	5.6kΩ
186	WRT	V_{DD}	5.6kΩ
187	$\overline{\text{WE}}$	V_{DD}	5.6kΩ
188	V_{DDO}	V_{DD}	N/A
189	V_{SSO}	V_{SS}	N/A
190	RD	V_{DD}	5.6kΩ
191	RLDSTO	V_{DD}	5.6kΩ
192	LOCK	V_{DD}	5.6kΩ
193	DXFER	V_{DD}	5.6kΩ
194	$\overline{\text{MEXC}}$	V_{DD}	5.6kΩ
195	V_{DDO}	V_{DD}	N/A
196	V_{SSO}	V_{SS}	N/A
197	$\overline{\text{RESET}}$	V_{DD}	5.6kΩ
198	$\overline{\text{SYSRESET}}$	V_{GEN2}	1kΩ
199	BA[1]	V_{DD}	5.6kΩ
200	BA[0]	V_{DD}	5.6kΩ
201	CB[6]	V_{SS}	1kΩ
202	CB[5]	V_{SS}	1kΩ
203	V_{DDO}	V_{DD}	N/A
204	V_{SSO}	V_{SS}	N/A
205	CB[4]	V_{SS}	1kΩ
206	CB[3]	V_{DD}	1kΩ
207	CB[2]	V_{SS}	1kΩ
208	CB[1]	V_{DD}	1kΩ
209	V_{DDO}	V_{DD}	N/A
210	V_{SSO}	V_{SS}	N/A
211	CB[0]	V_{SS}	1kΩ
212	$\overline{\text{ALE}}$	V_{DD}	5.6kΩ
213	V_{DDI}	V_{DD}	N/A
214	V_{SSI}	V_{SS}	N/A

Pin	Signal	Wired to:	Serial Resistor
215	$\overline{\text{PROM8}}$	V_{DD}	1kΩ
216	$\overline{\text{ROMCS}}$	V_{DD}	5.6kΩ
217	$\overline{\text{MEMCS}}$[9]	V_{DD}	5.6kΩ
218	V_{DDO}	V_{DD}	N/A
219	V_{SSO}	V_{SS}	N/A
220	$\overline{\text{MEMCS}}$[8]	V_{DD}	5.6kΩ
221	$\overline{\text{MEMCS}}$[7]	V_{DD}	5.6kΩ
222	$\overline{\text{MEMCS}}$[6]	V_{DD}	5.6kΩ
223	$\overline{\text{MEMCS}}$[5]	V_{DD}	5.6kΩ
224	$\overline{\text{MEMCS}}$[4]	V_{DD}	5.6kΩ
225	$\overline{\text{MEMCS}}$[3]	V_{DD}	5.6kΩ
226	V_{DDO}	V_{DD}	N/A
227	V_{SSO}	V_{SS}	N/A
228	$\overline{\text{MEMCS}}$[2]	V_{DD}	5.6kΩ
229	$\overline{\text{MEMCS}}$[1]	V_{DD}	5.6kΩ
230	$\overline{\text{MEMCS}}$[0]	V_{DD}	5.6kΩ
231	V_{DDI}	V_{DD}	N/A
232	V_{SSI}	V_{SS}	N/A
233	$\overline{\text{OE}}$	V_{DD}	5.6kΩ
234	V_{DDO}	V_{DD}	N/A
235	V_{SSO}	V_{SS}	N/A
236	$\overline{\text{MEMWR}}$	V_{DD}	5.6kΩ
237	$\overline{\text{BUFFEN}}$	V_{DD}	5.6kΩ
238	DDIR	V_{DD}	5.6kΩ
239	V_{DDO}	V_{DD}	N/A
240	V_{SSO}	V_{SS}	N/A
241	$\overline{\text{DDIR}}$	V_{DD}	5.6kΩ
242	$\overline{\text{MHOLD}}$	V_{DD}	5.6kΩ
243	$\overline{\text{MDS}}$	V_{DD}	5.6kΩ
244	WDCLK	V_{SS}	1kΩ
245	IWDE	V_{SS}	1kΩ
246	EWDINT	V_{SS}	1kΩ
247	TMODE[1]	V_{SS}	1kΩ
248	TMODE[0]	V_{SS}	1kΩ
249	DEBUG	V_{SS}	1kΩ
250	INULL	V_{DD}	5.6kΩ

Pin	Signal	Wired to:	Serial Resistor
251	DIA	V_{DD}	5.6kΩ
252	V_{DDO}	V_{DD}	N/A
253	V_{SSO}	V_{SS}	N/A
254	FLUSH	V_{DD}	5.6kΩ
255	INST	V_{DD}	5.6kΩ
256	RTC	V_{DD}	5.6kΩ

2. $f_{GEN2} = f_{GEN1} / 2^{15}$.

2.7 OPERATING LIFE CONDITIONS

The conditions shall be as specified for Power Burn-in.

2.8 TOTAL DOSE IRRADIATION TESTING

2.8.1 Bias Conditions and Total Dose Level for Total Dose Radiation Testing

Continuous bias shall be applied during irradiation testing as specified below.
The total dose level applied shall be as specified in the component type variant information herein or in the Purchase Order.

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	T_{amb}	+22 ± 3	°C
Input CLK2	V_{IN}	V_{GEN1} (Note 1)	V
All other Inputs and Outputs	V_{IN}, V_{OUT}	V_{DD}, V_{SS} (Note 1)	V
Pulse Voltage	V_{GEN1}	0V to V_{DD}	V
Pulse Frequency Square Wave	f_{GEN1}	≤ 100 50± 15% Duty Cycle $t_r = t_f \leq 500ns$	Hz
Positive Supply Voltage V_{DDO}, V_{DDI}	V_{DD}	5(+0.5, -0)	V
Negative Supply Voltage V_{SSO}, V_{SSI}	V_{SS}	0	V

NOTES:

1. All Inputs and Outputs shall be connected through a serial protection resistor/load as defined for burn-in with the exception that Pin 198 $\overline{\text{SYSRESET}}$ shall be connected to V_{SS} through 1kΩ serial resistor.

2.8.2 Electrical Measurements for Total Dose Radiation Testing

Prior to, during and on completion of irradiation testing the devices shall successfully meet Room Temperature Electrical Measurements specified herein.
Unless otherwise stated the measurements shall be performed at T_{amb} = +22 ± 3°C.

The characteristics, test methods, conditions and limits shall be the same as specified for Room Temperature Electrical Measurements.