



Pages 1 to 34

**INTEGRATED CIRCUITS, SILICON MONOLITHIC, CMOS,
GATE ARRAY/EMBEDDED ARRAY**

BASED ON TYPE MH1RT

ESCC Detail Specification No. 9202/076

Issue 4	November 2010
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Document Custodian: European Space Agency - see <https://escies.org>

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DCR No.	CHANGE DESCRIPTION
615, 633	Specification upissued to incorporate technical and editorial changes per DCRs.

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1. GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics and test and inspection data for the component type variants and/or the range of components specified below. It supplements the requirements of, and shall be read in conjunction with, the ESCC Generic Specification listed under Applicable Documents.

1.2 APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:

- (a) ESCC Generic Specification No. 9000.
- (b) MIL-STD-883, Test Methods and Procedures for Microelectronics.

1.3 TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESCC Basic Specification No. 21300 shall apply.

1.4 THE ESCC COMPONENT NUMBER AND COMPONENT TYPE VARIANTS

1.4.1 The ESCC Component Number

The ESCC Component number shall be constituted as follows:

Example: 920207601RXYZ

- Detail Specification Reference: 9202076
- Component Type Variant Number: 01 (as required)
- Total Dose Radiation Level Letter: R (as required)
- Manufacturer Specific ASIC Identification: XYZ (as applicable) where:
 XYZ : Individual 3 character code allocated by the Manufacturer to a specific ASIC design.

1.4.2 Component Type Variants

The component type variants applicable to this specification are as follows:

Variant Number	Based on Type	Circuit Function	Supply Voltage	Case	Terminal Material and Finish (Note 5)	Weight max g	Total Dose Radiation Level Letter (Note 6)	Notes
01	TH1099ER	988000 sites	Single Supply (3V)	MQFP-T352	D2	27	R [100kRAD(Si)]	1, 3
02	TH1099ER	988000 sites	Single Supply (3V)	MQFP-F256	D2	14	R [100kRAD(Si)]	1, 3

Variant Number	Based on Type	Circuit Function	Supply Voltage	Case	Terminal Material and Finish (Note 5)	Weight max g	Total Dose Radiation Level Letter (Note 6)	Notes
03	TH1099ER	988000 sites	Single Supply (3V)	MQFP-F196	D2	10	R [100kRAD(Si)]	1, 3
04	TH1099ER	988000 sites	Single Supply (3V)	MCGA-349	R	9	R [100kRAD(Si)]	1, 3
05	TH1156ER	1558000 sites	Single Supply (3V)	MQFP-T352	D2	27	R [100kRAD(Si)]	1, 3
06	TH1156ER	1558000 sites	Single Supply (3V)	MQFP-F256	D2	14	R [100kRAD(Si)]	1, 3
07	TH1156ER	1558000 sites	Single Supply (3V)	MCGA-472	R	12	R [100kRAD(Si)]	1, 3
08	TH1156ER	1558000 sites	Single Supply (3V)	MCGA-349	R	9	R [100kRAD(Si)]	1, 3
09	TH1242ER	2422000 sites	Single Supply (3V)	MQFP-T352	D2	27	R [100kRAD(Si)]	1, 3
10	TH1242ER	2422000 sites	Single Supply (3V)	MQFP-F256	D2	14	R [100kRAD(Si)]	1, 3
11	TH1242ER	2422000 sites	Single Supply (3V)	MCGA-472	R	12	R [100kRAD(Si)]	1, 3
12	TH1242ER	2422000 sites	Single Supply (3V)	MCGA-349	R	9	R [100kRAD(Si)]	1, 3
13	TH1332ER	3319000 sites	Single Supply (3V)	MCGA-472	R	12	R [100kRAD(Si)]	1, 3
14	TH1099ES	988000 sites	Bi-voltage Supply (3V/5V)	MQFP-T352	D2	27	R [100kRAD(Si)]	2, 3
15	TH1099ES	988000 sites	Bi-voltage Supply (3V/5V)	MQFP-F256	D2	14	R [100kRAD(Si)]	2, 3
16	TH1099ES	988000 sites	Bi-voltage Supply (3V/5V)	MQFP-F196	D2	10	R [100kRAD(Si)]	2, 3

Variant Number	Based on Type	Circuit Function	Supply Voltage	Case	Terminal Material and Finish (Note 5)	Weight max g	Total Dose Radiation Level Letter (Note 6)	Notes
17	TH1099ES	988000 sites	Bi-voltage Supply (3V/5V)	MCGA-349	R	9	R [100kRAD(Si)]	2, 3
18	TH1156ES	1558000 sites	Bi-voltage Supply (3V/5V)	MQFP-T352	D2	27	R [100kRAD(Si)]	2, 3
19	TH1156ES	1558000 sites	Bi-voltage Supply (3V/5V)	MQFP-F256	D2	14	R [100kRAD(Si)]	2, 3
20	TH1156ES	1558000 sites	Bi-voltage Supply (3V/5V)	MCGA-472	R	12	R [100kRAD(Si)]	2, 3
21	TH1156ES	1558000 sites	Bi-voltage Supply (3V/5V)	MCGA-349	R	9	R [100kRAD(Si)]	2, 3
22	TH1242ES	2422000 sites	Bi-voltage Supply (3V/5V)	MQFP-T352	D2	27	R [100kRAD(Si)]	2, 3
23	TH1242ES	2422000 sites	Bi-voltage Supply (3V/5V)	MQFP-F256	D2	14	R [100kRAD(Si)]	2, 3
24	TH1242ES	2422000 sites	Bi-voltage Supply (3V/5V)	MCGA-472	R	12	R [100kRAD(Si)]	2, 3
25	TH1242ES	2422000 sites	Bi-voltage Supply (3V/5V)	MCGA-349	R	9	R [100kRAD(Si)]	2, 3
26	TH1332ES	3319000 sites	Bi-voltage Supply (3V/5V)	MCGA-472	R	12	R [100kRAD(Si)]	2, 3
27	TH1M099ER	988000 sites composite	Single Supply (3V)	MQFP-T352	D2	27	R [100kRAD(Si)]	1, 4
28	TH1M099ER	988000 sites composite	Single Supply (3V)	MQFP-F256	D2	14	R [100kRAD(Si)]	1, 4
29	TH1M099ER	988000 sites composite	Single Supply (3V)	MQFP-F196	D2	10	R [100kRAD(Si)]	1, 4
30	TH1M099ER	988000 sites composite	Single Supply (3V)	MCGA-349	R	9	R [100kRAD(Si)]	1, 4

Variant Number	Based on Type	Circuit Function	Supply Voltage	Case	Terminal Material and Finish (Note 5)	Weight max g	Total Dose Radiation Level Letter (Note 6)	Notes
31	TH1M156ER	1558000 sites composite	Single Supply (3V)	MQFP-T352	D2	27	R [100kRAD(Si)]	1, 4
32	TH1M156ER	1558000 sites composite	Single Supply (3V)	MQFP-F256	D2	14	R [100kRAD(Si)]	1, 4
33	TH1M156ER	1558000 sites composite	Single Supply (3V)	MCGA-472	R	12	R [100kRAD(Si)]	1, 4
34	TH1M156ER	1558000 sites composite	Single Supply (3V)	MCGA-349	R	9	R [100kRAD(Si)]	1, 4
35	TH1M242ER	2422000 sites composite	Single Supply (3V)	MQFP-T352	D2	27	R [100kRAD(Si)]	1, 4
36	TH1M242ER	2422000 sites composite	Single Supply (3V)	MQFP-F256	D2	14	R [100kRAD(Si)]	1, 4
37	TH1M242ER	2422000 sites composite	Single Supply (3V)	MCGA-472	R	12	R [100kRAD(Si)]	1, 4
38	TH1M242ER	2422000 sites composite	Single Supply (3V)	MCGA-349	R	9	R [100kRAD(Si)]	1, 4
39	TH1M332ER	3319000 sites composite	Single Supply (3V)	MCGA-472	R	12	R [100kRAD(Si)]	1, 4
40	TH1M099ES	988000 sites composite	Bi-voltage Supply (3V/5V)	MQFP-T352	D2	27	R [100kRAD(Si)]	2, 4
41	TH1M099ES	988000 sites composite	Bi-voltage Supply (3V/5V)	MQFP-F256	D2	14	R [100kRAD(Si)]	2, 4
42	TH1M099ES	988000 sites composite	Bi-voltage Supply (3V/5V)	MQFP-F196	D2	10	R [100kRAD(Si)]	2, 4
43	TH1M099ES	988000 sites composite	Bi-voltage Supply (3V/5V)	MCGA-349	R	9	R [100kRAD(Si)]	2, 4
44	TH1M156ES	1558000 sites composite	Bi-voltage Supply (3V/5V)	MQFP-T352	D2	27	R [100kRAD(Si)]	2, 4

Variant Number	Based on Type	Circuit Function	Supply Voltage	Case	Terminal Material and Finish (Note 5)	Weight max g	Total Dose Radiation Level Letter (Note 6)	Notes
45	TH1M156ES	1558000 sites composite	Bi-voltage Supply (3V/5V)	MQFP-F256	D2	14	R [100kRAD(Si)]	2, 4
46	TH1M156ES	1558000 sites composite	Bi-voltage Supply (3V/5V)	MCGA-472	R	12	R [100kRAD(Si)]	2, 4
47	TH1M156ES	1558000 sites composite	Bi-voltage Supply (3V/5V)	MCGA-349	R	9	R [100kRAD(Si)]	2, 4
48	TH1M242ES	2422000 sites composite	Bi-voltage Supply (3V/5V)	MQFP-T352	D2	27	R [100kRAD(Si)]	2, 4
49	TH1M242ES	2422000 sites composite	Bi-voltage Supply (3V/5V)	MQFP-F256	D2	14	R [100kRAD(Si)]	2, 4
50	TH1M242ES	2422000 sites composite	Bi-voltage Supply (3V/5V)	MCGA-472	R	12	R [100kRAD(Si)]	2, 4
51	TH1M242ES	2422000 sites composite	Bi-voltage Supply (3V/5V)	MCGA-349	R	9	R [100kRAD(Si)]	2, 4
52	TH1M332ES	3319000 sites composite	Bi-voltage Supply (3V/5V)	MCGA-472	R	12	R [100kRAD(Si)]	2, 4
53	TH1099ER	988000 sites	Single Supply (3V)	LGA-349	E2	7	R [100kRAD(Si)]	1, 3
54	TH1156ER	1558000 sites	Single Supply (3V)	LGA-472	E2	10	R [100kRAD(Si)]	1, 3
55	TH1156ER	1558000 sites	Single Supply (3V)	LGA-349	E2	7	R [100kRAD(Si)]	1, 3
56	TH1242ER	2422000 sites	Single Supply (3V)	LGA-472	E2	10	R [100kRAD(Si)]	1, 3
57	TH1242ER	2422000 sites	Single Supply (3V)	LGA-349	E2	7	R [100kRAD(Si)]	1, 3
58	TH1332ER	3319000 sites	Single Supply (3V)	LGA-472	E2	10	R [100kRAD(Si)]	1, 3

Variant Number	Based on Type	Circuit Function	Supply Voltage	Case	Terminal Material and Finish (Note 5)	Weight max g	Total Dose Radiation Level Letter (Note 6)	Notes
59	TH1099ES	988000 sites	Bi-voltage Supply (3V/5V)	LGA-349	E2	7	R [100kRAD(Si)]	2, 3
60	TH1156ES	1558000 sites	Bi-voltage Supply (3V/5V)	LGA-472	E2	10	R [100kRAD(Si)]	2, 3
61	TH1156ES	1558000 sites	Bi-voltage Supply (3V/5V)	LGA-349	E2	7	R [100kRAD(Si)]	2, 3
62	TH1242ES	2422000 sites	Bi-voltage Supply (3V/5V)	LGA-472	E2	10	R [100kRAD(Si)]	2, 3
63	TH1242ES	2422000 sites	Bi-voltage Supply (3V/5V)	LGA-349	E2	7	R [100kRAD(Si)]	2, 3
64	TH1332ES	3319000 sites	Bi-voltage Supply (3V/5V)	LGA-472	E2	10	R [100kRAD(Si)]	2, 3
65	TH1M099ER	988000 sites composite	Single Supply (3V)	LGA-349	E2	7	R [100kRAD(Si)]	1, 4
66	TH1M156ER	1558000 sites composite	Single Supply (3V)	LGA-472	E2	10	R [100kRAD(Si)]	1, 4
67	TH1M156ER	1558000 sites composite	Single Supply (3V)	LGA-349	E2	7	R [100kRAD(Si)]	1, 4
68	TH1M242ER	2422000 sites composite	Single Supply (3V)	LGA-472	E2	10	R [100kRAD(Si)]	1, 4
69	TH1M242ER	2422000 sites composite	Single Supply (3V)	LGA-349	E2	7	R [100kRAD(Si)]	1, 4
70	TH1M332ER	3319000 sites composite	Single Supply (3V)	LGA-472	E2	10	R [100kRAD(Si)]	1, 4
71	TH1M099ES	988000 sites composite	Bi-voltage Supply (3V/5V)	LGA-349	E2	7	R [100kRAD(Si)]	2, 4
72	TH1M156ES	1558000 sites composite	Bi-voltage Supply (3V/5V)	LGA-472	E2	10	R [100kRAD(Si)]	2, 4

Variant Number	Based on Type	Circuit Function	Supply Voltage	Case	Terminal Material and Finish (Note 5)	Weight max g	Total Dose Radiation Level Letter (Note 6)	Notes
73	TH1M156ES	1558000 sites composite	Bi-voltage Supply (3V/5V)	LGA-349	E2	7	R [100kRAD(Si)]	2, 4
74	TH1M242ES	2422000 sites composite	Bi-voltage Supply (3V/5V)	LGA-472	E2	10	R [100kRAD(Si)]	2, 4
75	TH1M242ES	2422000 sites composite	Bi-voltage Supply (3V/5V)	LGA-349	E2	7	R [100kRAD(Si)]	2, 4
76	TH1M332ES	3319000 sites composite	Bi-voltage Supply (3V/5V)	LGA-472	E2	10	R [100kRAD(Si)]	2, 4

NOTES:

1. The component is specified for operation at a nominal single supply voltage $V_{DD} = 2.5V, 3V$ or $3.3V$.
2. The component is specified for bi-voltage operation at $V_{DD} = 2.5V, 3V$ or $3.3V$ and inputs and/or outputs tolerant or compliant to $V_{CC} = 5V$.
3. The ASIC design will be customised at metal levels.
4. The ASIC design will be customised at base wafer and metal levels.
5. The terminal material and finish shall be in accordance with the requirements of ESCC Basic Specification No. 23500.
6. The total dose radiation level letter shall be as defined in ESCC Basic Specification No. 22900. If an alternative radiation test level is specified in the Purchase Order the letter shall be changed accordingly.

1.4.3 Manufacturer Specific ASIC Identification

An ASIC Sheet shall be produced by the Manufacturer, after negotiation with the Orderer, that, as a minimum, specifies all the requirements unique to the specific ASIC design that are identified herein as being specified in the ASIC Sheet. The ASIC Sheet shall be held under configuration control by the Manufacturer. For identification and traceability purposes the Manufacturer shall allocate a unique Manufacturer Specific ASIC Identification to the ASIC Sheet and the specific ASIC design as specified in The ESCC Component Number herein.

1.5 MAXIMUM RATINGS

The maximum ratings shall not be exceeded at any time during use or storage. Maximum ratings shall only be exceeded during testing to the extent specified in this specification and when stipulated in Test Methods and Procedures of the ESCC Generic Specification.

Characteristics	Symbols	Maximum Ratings	Units	Remarks
Supply Voltage	V_{DD} V_{CC}	-0.5 to 4 -0.5 to 6	V	Note 1
Input Voltage 2.5V, 3V, 3.3V Range 5V Compliant 5V Tolerant	V_{IN}	-0.5 to $V_{DD} + 0.5$ -0.5 to $V_{CC} + 0.5$ $-0.5V \leq V_{CC} \leq 6$	V	Note 1, 2
Input Current	I_{IN}	± 60	mA	Each Input pin

Characteristics	Symbols	Maximum Ratings	Units	Remarks
Device Power Dissipation (Continuous)	P_D	See ASIC Sheet	W	
Supply Current	I_{DDop}	See ASIC Sheet	mA	
Minimum Guaranteed Operating Temperature Range	T_{op}	-55 to +125	°C	T_{amb} , Note 4
Storage Temperature Range	T_{stg}	-65 to +150	°C	
Junction Temperature	T_j	+175	°C	
Thermal Resistance Junction to case	$R_{th(j-c)}$	See ASIC Sheet	°C/W	
Soldering Temperature	T_{sol}	+300	°C	Note 3

NOTES:

1. With reference to $V_{SS} = 0V$.
2. Applicable to all inputs. Input current limited to $I_{IC} = \pm 10mA$.
3. Duration 10 seconds maximum at a distance of not less than 1.6mm from the device body and the same terminal shall not be resoldered until 3 minutes have elapsed.
4. For an individual ASIC design see ASIC Sheet for the actual maximum operating temperature range.

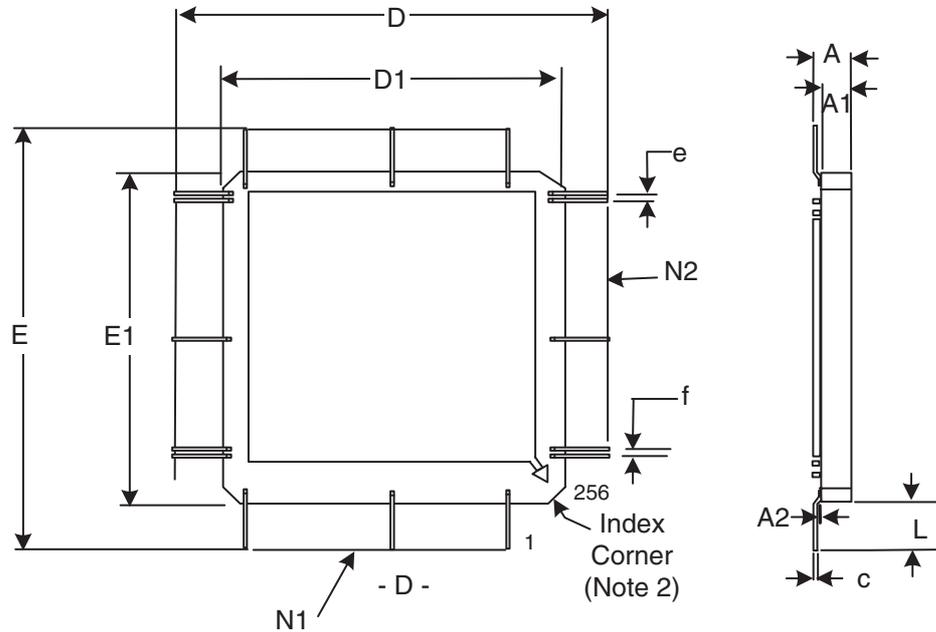
1.6

HANDLING PRECAUTIONS

These devices are susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacture, testing, packaging, shipment and any handling.

These components are categorised as Class 3 per ESCC Basic Specification No. 23800 with a Minimum Critical Path Failure Voltage of 4000 Volts.

1.7.2 Multilayer Quad Flat Package (MQFP-F256) - 256 Flat Leads

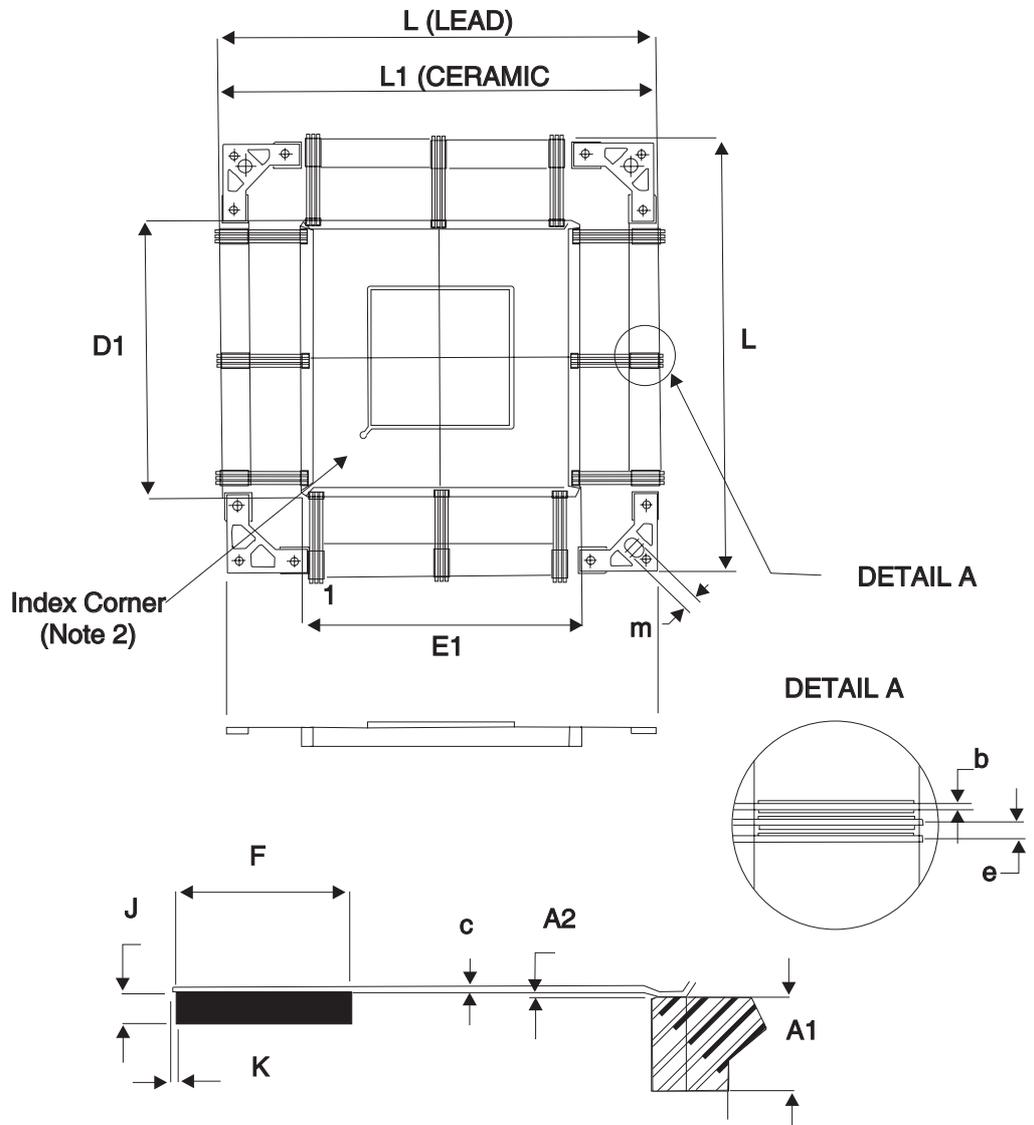


Symbols	Dimensions mm		Notes
	Min	Max	
A	2.41	3.18	
A1	2.06	2.56	
A2	0.05	0.36	
c	0.1	0.2	1
D/E	53.23	55.74	
D1/E1	36.83	37.34	
e	0.508 BSC		1
f	0.15	0.25	1
L	8.2	9.2	1
N1/N2	64		Each side

NOTES:

1. Applies to all leads.
2. Terminal identification is specified by reference to the index corner as shown.

1.7.3 Multilayer Quad Flat Package (MQFP-T352) - 352 Tied Leads



Symbols	Dimensions mm		Notes
	Min	Max	
A1	2.35	3.15	
A2	0.05	0.35	
b	0.19	0.25	1
c	0.11	0.2	1
D1/E1	47.52	48.48	
e	0.50 BSC		1
F	4.5	5.5	
G	2.5	2.6	
J	0.75	1.05	

Symbols	Dimensions mm		Notes
	Min	Max	
K	-	0.5	1
L	74.85	76.4	
L1	74.6	75.4	
m	2.5	2.65	
N1/N2	88		Each side

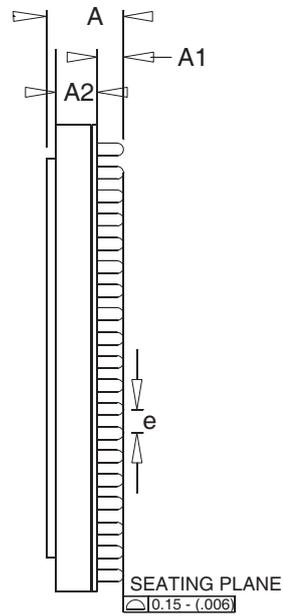
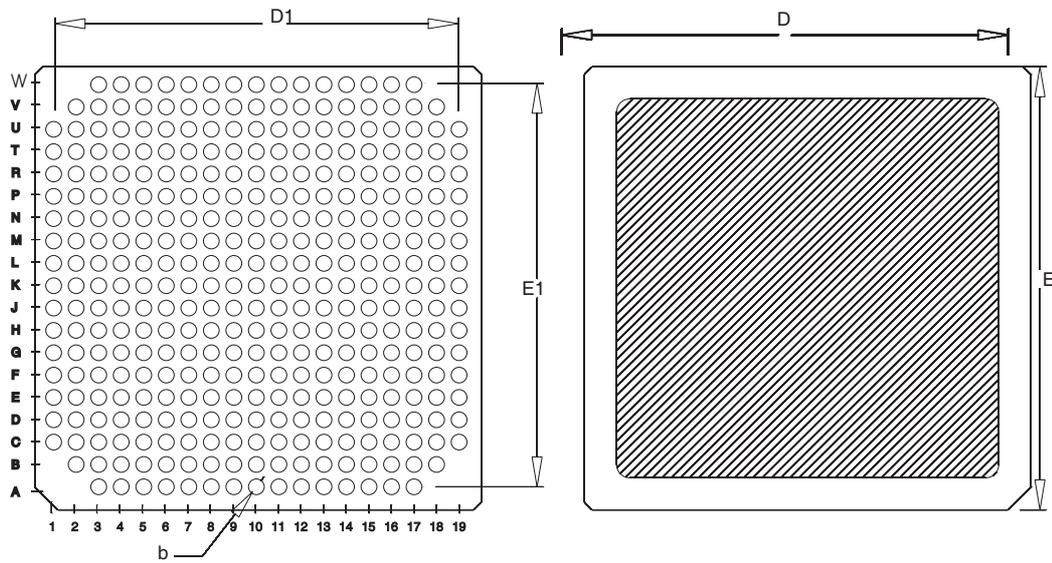
NOTES:

1. Applies to all leads.
2. Terminal identification is specified by reference to the index corner as shown.

1.7.4 Multilayer Column Grid Array (MCGA-349) - 349 Columns

BOTTOM VIEW

TOP VIEW



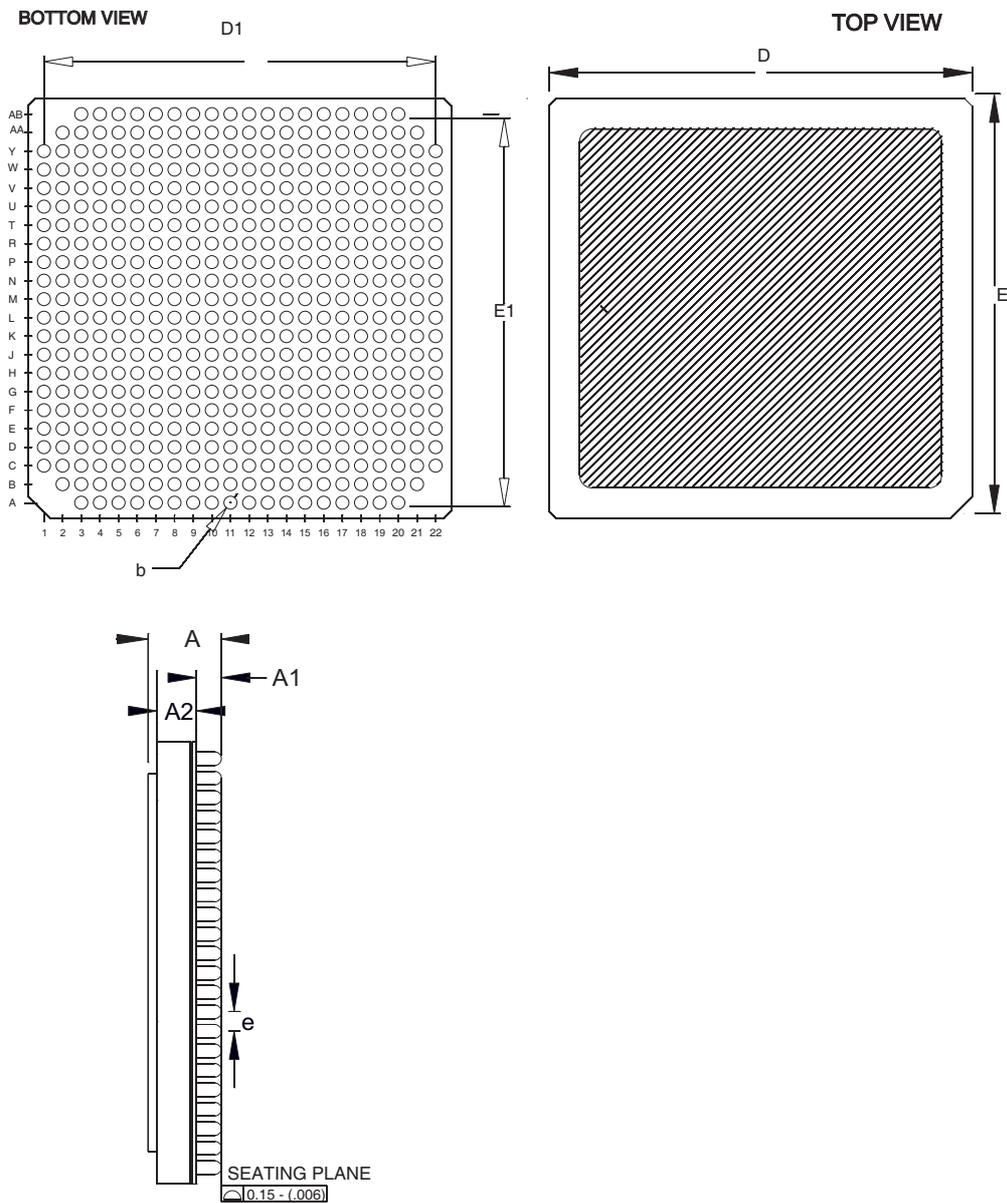
Symbols	Dimensions mm		Notes
	Min	Max	
A	4.3	5.9	
A1	1.4	1.85	
A2	2.4	3.45	
b	0.79	0.99	1

Symbols	Dimensions mm		Notes
	Min	Max	
D/E	24.8	25.2	
D1/E1	22.86		
e	1.27 BSC		1

NOTES:

1. Applies to all columns.
2. Terminal identification is specified by reference to the index corner as shown.

1.7.5 Multilayer Column Grid Array (MCGA-472) - 472 Columns



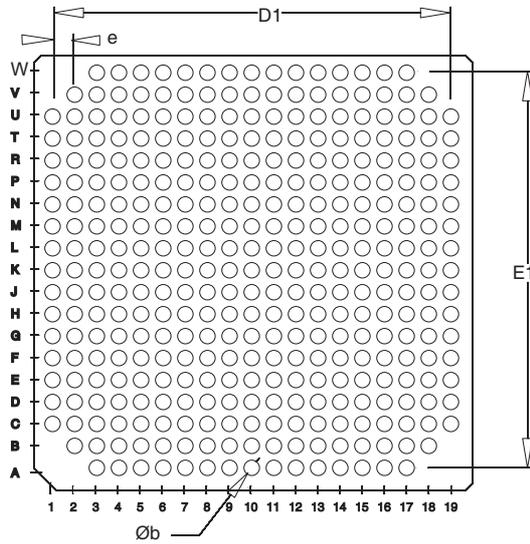
Symbols	Dimensions mm		Notes
	Min	Max	
A	4.3	5.9	
A1	1.4	1.85	
A2	2.6	3.45	
b	0.79	0.99	1
D/E	28.77	29.23	
D1/E1	26.67		
e	1.27 BSC		1

NOTES:

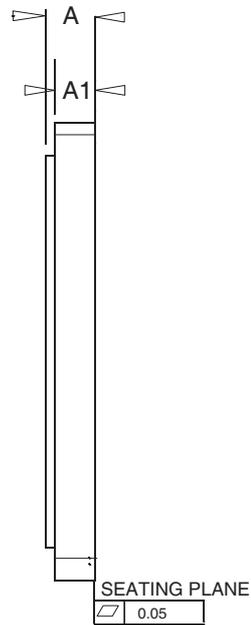
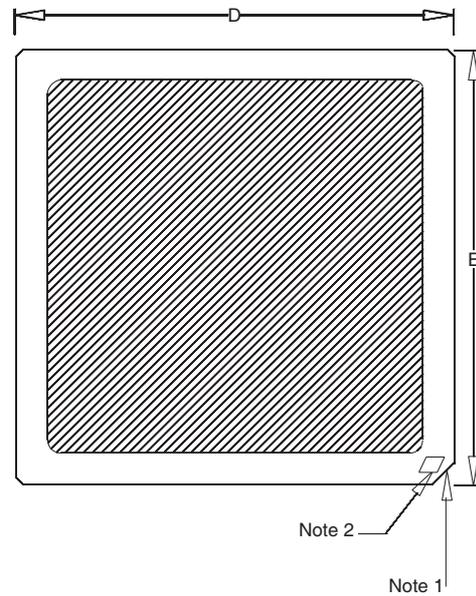
1. Applies to all columns.
2. Terminal identification is specified by reference to the index corner as shown.

1.7.6 Land Grid Array (LGA-349) - 349 Pads

BOTTOM VIEW



TOP VIEW



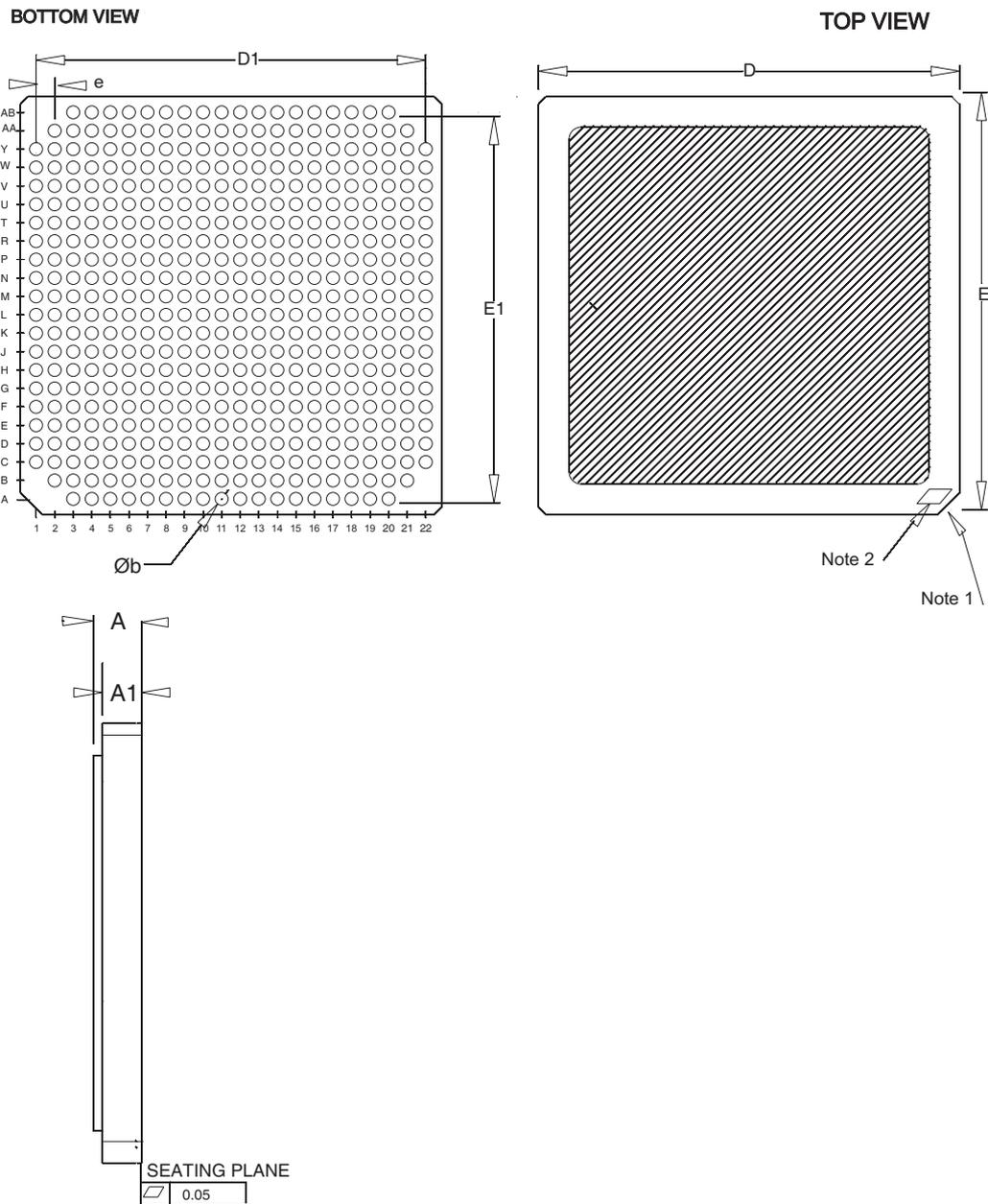
Symbols	Dimensions mm		Notes
	Min	Max	
A	-	3.24	
A1	2.27	2.77	
Øb	0.81	0.91	3
D/E	24.85	25.15	
D1/E1	22.86 BSC		

Symbols	Dimensions mm		Notes
	Min	Max	
e	1.27 BSC		3

NOTES:

1. Index corner. Terminal identification is specified by reference to the index corner as shown.
2. A terminal identification mark shall be located at the index corner as shown.
3. Applies to all pads.

1.7.7 Land Grid Array (LGA-472) - 472 Pads



Symbols	Dimensions mm		Notes
	Min	Max	
A	-	3.24	
A1	2.27	2.77	
Øb	0.81	0.91	3
D/E	28.85	29.15	
D1/E1	26.67 BSC		
e	1.27 BSC		3

NOTES:

1. Index corner. Terminal identification is specified by reference to the index corner as shown.
2. A terminal identification mark shall be located at the index corner as shown.
3. Applies to all pads.

1.8 FUNCTIONAL DIAGRAM

See ASIC Sheet.

NOTES:

1. For all packages the lid is internally connected to the ground terminal as specified in the ASIC Sheet.

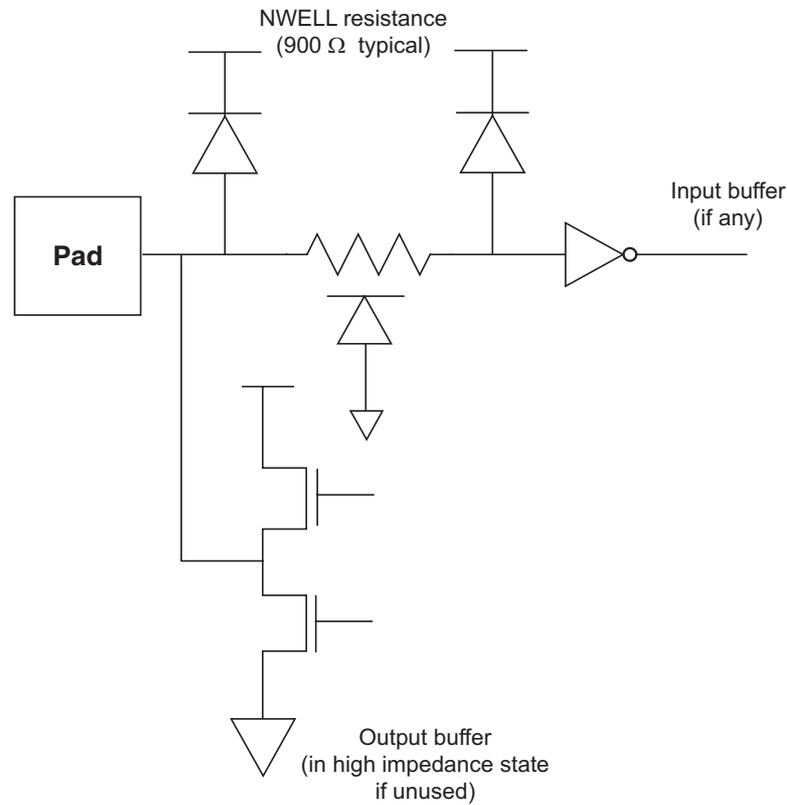
1.9 PIN ASSIGNMENT

See ASIC Sheet.

1.10 INSTRUCTION SET AND TIMING DIAGRAMS

See ASIC Sheet.

1.11 PROTECTION NETWORK



2. REQUIREMENTS

2.1 GENERAL

The complete requirements for procurement of the components specified herein are as stated in this specification and the ESCC Generic Specification. Permitted deviations from the Generic Specification, applicable to this specification only, are listed below.

Permitted deviations from the Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESCC requirement and do not affect the component's reliability, are listed in the appendices attached to this specification.

2.1.1 Deviations from the Generic Specification

2.1.1.1 *Deviations from Screening Tests*

High Temperature Reverse Bias Burn-in shall not be performed.

2.2 MARKING

The marking shall be in accordance with the requirements of ESCC Basic Specification No. 21700 and

as follows.

As a minimum the information to be marked on the component shall be:

- (a) The ESCC qualified components symbol (for ESCC qualified components only).
- (b) The ESCC Component Number.
- (c) Traceability information.

The complete marking shall be as specified in the ASIC Sheet.

2.3 ELECTRICAL MEASUREMENTS AT ROOM, HIGH AND LOW TEMPERATURES

Electrical measurements shall be performed at room, high and low temperatures. Consolidated notes are given after the tables.

2.3.1 Room Temperature Electrical Measurements

The measurements shall be performed at $T_{amb} = +22 \pm 3^{\circ}\text{C}$.

2.3.1.1 Room Temperature Electrical Measurements for Components Specified at Single Supply Voltage $V_{DD} = 2.5\text{V}$

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1 ($V_{DD} = 2.5 \pm 0.2\text{V}$)	Limits		Units
				Min	Max	
Functional Test 1	-	3014	See ASIC Sheet $V_{DD}=2.3\text{V}$	-	-	-
Functional Test 2	-	3014	See ASIC Sheet $V_{DD}=2.5\text{V}$	-	-	-
Functional Test 3	-	3014	See ASIC Sheet $V_{DD}=2.7\text{V}$	-	-	-
Supply Current, Stand-by	I_{DDSB}	3005	See ASIC Sheet			mA
Supply Current, Operating	I_{DDOP}	3005	See ASIC Sheet			mA
Low Level Input Current	I_{IL}	3009	$V_{IN}=V_{SS}$, CMOS Buffers	-	-1	μA
Low Level Input Current, Pull-up Resistor PRU1	I_{ILPU}	3009	$V_{IN}=V_{SS}$, CMOS Buffers Note 2	70	230	μA
Low Level Input Current, Pull-down Resistor PRD1	I_{ILPD}	3009	$V_{IN}=V_{SS}$, CMOS Buffers Note 2	-	± 5	μA
High Level Input Current	I_{IH}	3010	$V_{IN}=V_{DD}$, CMOS Buffers	-	1	μA
High Level Input Current, Pull-up Resistor PRU1	I_{IHPU}	3010	$V_{IN}=V_{DD}$, CMOS Buffers Note 2	-	± 5	μA

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1 ($V_{DD} = 2.5 \pm 0.2V$)	Limits		Units
				Min	Max	
High Level Input Current, Pull-down Resistor PRD1	I_{IHPD}	3010	$V_{IN}=V_{DD}$, CMOS Buffers Note 2	70	540	μA
Low Level Input Voltage	V_{IL}	-	CMOS Buffers $V_{DD}=2.3V$,	-	690	mV
High Level Input Voltage	V_{IH}	-	CMOS Buffers $V_{DD}=2.7V$	1.89	-	V
Positive Trigger Threshold Voltage	V_{TP}	-	Note 5	1.06	1.61	V
Negative Trigger Threshold Voltage	V_{TN}	-	Note 5	0.78	1.25	V
Hysteresis Voltage	V_H	-	Note 5	250	-	mV
Output Leakage Current Third State, Low Level Applied	I_{OZL}	3020	$V_{OUT}=0V$, All Buffers $V_{DD}=2.7V$	-	-1	μA
Output Leakage Current Third State, High Level Applied	I_{OZH}	3021	$V_{OUT}=0V$, All Buffers $V_{DD}=2.7V$	-	1	μA
Input Current, Cold Sparing	I_{ICS}	-	$V_{IN}=0V$ to 2.7V, PICZ Buffers $V_{DD}=V_{SS}=0V$	-	± 2	μA
Output Current, Cold Sparing	I_{OCS}	-	$V_{OUT}=0V$ to 2.7V, PO11Z Buffers $V_{DD}=V_{SS}=0V$	-	± 2	μA
Low Level Output Voltage	V_{OL}	3007	$V_{DD}=2.3V$, $I_{OL}=800\mu A$ PO11 Buffers Note 3	-	400	mV
High Level Output Voltage	V_{OH}	3006	$V_{DD}=2.3V$, $I_{OH}=-600\mu A$ PO11 Buffers Note 4	2	-	V
Output Short Circuit Current, to V_{DD}	I_{OSN}	-	PO11 output at High Level shorted to V_{DD} Note 5	-	15	mA
Output Short Circuit Current, to V_{SS}	I_{OSP}	-	PO11 output at High Level shorted to V_{SS} Note 5	-	8	mA
Input Capacitance	C_{IN}	3012	Note 5	-	2.4	pF
Output Capacitance	C_{OUT}	3012	Note 5	-	5.6	pF

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1 ($V_{DD} = 2.5 \pm 0.2V$)	Limits		Units
				Min	Max	
Input/Output Capacitance	$C_{I/O}$	3012	Note 5	-	6.6	pF
Timings	-	3003	See ASIC Sheet			ns

2.3.1.2 *Room Temperature Electrical Measurements for Components Specified at Single Supply Voltage $V_{DD} = 3V$*

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1 ($V_{DD} = 3 \pm 0.3V$)	Limits		Units
				Min	Max	
Functional Test 1	-	3014	See ASIC Sheet $V_{DD}=2.7V$	-	-	-
Functional Test 2	-	3014	See ASIC Sheet $V_{DD}=3V$	-	-	-
Functional Test 3	-	3014	See ASIC Sheet $V_{DD}=3.3V$	-	-	-
Supply Current, Stand-by	I_{DDBS}	3005	See ASIC Sheet			mA
Supply Current, Operating	I_{DDOP}	3005	See ASIC Sheet			mA
Low Level Input Current	I_{IL}	3009	$V_{IN}=V_{SS}$, CMOS Buffers	-	-1	μA
Low Level Input Current, Pull-up Resistor PRU1	I_{ILPU}	3009	$V_{IN}=V_{SS}$, CMOS Buffers Note 2	108	330	μA
Low Level Input Current, Pull-down Resistor PRD1	I_{ILPD}	3009	$V_{IN}=V_{SS}$, CMOS Buffers Note 2	-	± 5	μA
High Level Input Current	I_{IH}	3010	$V_{IN}=V_{DD}$, CMOS Buffers	-	1	μA
High Level Input Current, Pull-up Resistor PRU1	I_{IHPU}	3010	$V_{IN}=V_{DD}$, CMOS Buffers Note 2	-	± 5	μA
High Level Input Current, Pull-down Resistor PRD1	I_{IHPD}	3010	$V_{IN}=V_{DD}$, CMOS Buffers Note 2	108	825	μA
Low Level Input Voltage	V_{IL}	-	CMOS Buffers $V_{DD}=2.7V$,	-	800	mV
High Level Input Voltage	V_{IH}	-	CMOS Buffers $V_{DD}=3.3V$	2	-	V
Positive Trigger Threshold Voltage	V_{TP}	-	Note 5	1.25	1.93	V

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1 ($V_{DD} = 3 \pm 0.3V$)	Limits		Units
				Min	Max	
Negative Trigger Threshold Voltage	V_{TN}	-	Note 5	0.9	1.42	V
Hysteresis Voltage	V_H	-	Note 5	310	-	mV
Output Leakage Current Third State, Low Level Applied	I_{OZL}	3020	$V_{OUT}=0V$, All Buffers $V_{DD}=3.3V$	-	-1	μA
Output Leakage Current Third State, High Level Applied	I_{OZH}	3021	$V_{OUT}=0V$, All Buffers $V_{DD}=3.3V$	-	1	μA
Input Current, Cold Sparing	I_{ICS}	-	$V_{IN}=0V$ to 3.3V, PICZ Buffers $V_{DD}=V_{SS}=0V$	-	± 2	μA
Output Current, Cold Sparing	I_{OCS}	-	$V_{OUT}=0V$ to 3.3V, PO11X Buffers $V_{DD}=V_{SS}=0V$	-	± 2	μA
Low Level Output Voltage	V_{OL}	3007	$V_{DD}=2.7V$, $I_{OL}=1mA$ PO11 Buffers Note 3	-	400	mV
High Level Output Voltage	V_{OH}	3006	$V_{DD}=2.7V$, $I_{OH}=-800\mu A$ PO11 Buffers Note 4	2.4	-	V
Output Short Circuit Current, to V_{DD}	I_{OSN}	-	PO11 output at High Level shorted to V_{DD} Note 5	-	21	mA
Output Short Circuit Current, to V_{SS}	I_{OSP}	-	PO11 output at High Level shorted to V_{SS} Note 5	-	12	mA
Input Capacitance	C_{IN}	3012	Note 5	-	2.4	pF
Output Capacitance	C_{OUT}	3012	Note 5	-	5.6	pF
Input/Output Capacitance	$C_{I/O}$	3012	Note 5	-	6.6	pF
Timings	-	3003	See ASIC Sheet			ns

2.3.1.3 Room Temperature Electrical Measurements for Components Specified at Single Supply Voltage $V_{DD} = 3.3V$

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1 ($V_{DD} = 3.3 \pm 0.3V$)	Limits		Units
				Min	Max	
Functional Test 1	-	3014	See ASIC Sheet $V_{DD}=3V$	-	-	-
Functional Test 2	-	3014	See ASIC Sheet $V_{DD}=3.3V$	-	-	-
Functional Test 3	-	3014	See ASIC Sheet $V_{DD}=3.6V$	-	-	-
Supply Current, Stand-by	I_{DDBS}	3005	See ASIC Sheet			mA
Supply Current, Operating	I_{DDOP}	3005	See ASIC Sheet			mA
Low Level Input Current	I_{IL}	3009	$V_{IN}=V_{SS}$, CMOS Buffers	-	-1	μA
Low Level Input Current, Pull-up Resistor PRU1	I_{ILPU}	3009	$V_{IN}=V_{SS}$, CMOS Buffers Note 2	120	400	μA
Low Level Input Current, Pull-down Resistor PRD1	I_{ILPD}	3009	$V_{IN}=V_{SS}$, CMOS Buffers Note 2	-	± 5	μA
High Level Input Current	I_{IH}	3010	$V_{IN}=V_{DD}$, CMOS Buffers	-	1	μA
High Level Input Current, Pull-up Resistor PRU1	I_{IHPU}	3010	$V_{IN}=V_{DD}$, CMOS Buffers Note 2	-	± 5	μA
High Level Input Current, Pull-down Resistor PRD1	I_{IHPD}	3010	$V_{IN}=V_{DD}$, CMOS Buffers Note 2	150	900	μA
Low Level Input Voltage	V_{IL}	-	CMOS Buffers $V_{DD}=3V$	-	800	mV
High Level Input Voltage	V_{IH}	-	CMOS Buffers $V_{DD}=3.6V$	2	-	V
Positive Trigger Threshold Voltage	V_{TP}	-	Note 5	1.4	2.08	V
Negative Trigger Threshold Voltage	V_{TN}	-	Note 5	0.99	1.51	V
Hysteresis Voltage	V_H	-	Note 5	370	-	mV
Output Leakage Current Third State, Low Level Applied	I_{OZL}	3020	$V_{OUT}=0V$, All Buffers $V_{DD}=3.6V$	-	-1	μA

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1 ($V_{DD} = 3.3 \pm 0.3V$)	Limits		Units
				Min	Max	
Output Leakage Current Third State, High Level Applied	I_{OZH}	3021	$V_{OUT}=0V$, All Buffers $V_{DD}=3.6V$	-	1	μA
Input Current, Cold Sparing	I_{ICS}	-	$V_{IN}=0V$ to 3.6V, PICZ Buffers $V_{DD}=V_{SS}=0V$	-	± 2	μA
Output Current, Cold Sparing	I_{OCS}	-	$V_{OUT}=0V$ to 3.6V, PO11Z Buffers $V_{DD}=V_{SS}=0V$	-	± 2	μA
Low Level Output Voltage	V_{OL}	3007	$V_{DD}=3V$ $I_{OL}=2mA$ PO11 Buffers Note 3	-	400	mV
High Level Output Voltage	V_{OH}	3006	$V_{DD}=3V$ $I_{OL}=-1.8mA$ PO11 Buffers Note 4	2.4	-	V
Output Short Circuit Current, to V_{DD}	I_{OSN}	-	PO11 output at High Level shorted to V_{DD} Note 5	-	23	mA
Output Short Circuit Current, to V_{SS}	I_{OSP}	-	PO11 output at High Level shorted to V_{SS} Note 5	-	13	mA
Input Capacitance	C_{IN}	3012	Note 5	-	2.4	pF
Output Capacitance	C_{OUT}	3012	Note 5	-	5.6	pF
Input/Output Capacitance	$C_{I/O}$	3012	Note 5	-	6.6	pF
Timings	-	3003	See ASIC Sheet			ns

2.3.1.4 Room Temperature Electrical Measurements for Components Specified for Bi-voltage Operation at $V_{DD} = 2.5V, 3V$ or $3.3V$ and $V_{CC} = 5V$.

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1 [$V_{DD} = 2.5 \pm 0.2V, 3 \pm 0.3V, 3.3 \pm 0.3V$ (Note 6) $V_{CC}=5 \pm 0.5V$ (Note 7)]	Limits		Units
				Min	Max	
Functional Test 1	-	3014	See ASIC Sheet $V_{CC}=4.5V, V_{DD}=3V$	-	-	-
Functional Test 2	-	3014	See ASIC Sheet $V_{CC}=5V, V_{DD}=3.3V$	-	-	-

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1 [$V_{DD} = 2.5 \pm 0.2V, 3 \pm 0.3V, 3.3 \pm 0.3V$ (Note 6) $V_{CC}=5 \pm 0.5V$ (Note 7)]	Limits		Units
				Min	Max	
Functional Test 3	-	3014	See ASIC Sheet $V_{CC}=5.5V, V_{DD}=3.6V$	-	-	-
Supply Current, Stand-by	I_{DDBS}	3005	See ASIC Sheet			mA
Supply Current, Operating	I_{DDOP}	3005	See ASIC Sheet			mA
Low Level Input Current	I_{IL}	3009	$V_{IN}=V_{SS}$, CMOS Buffers	-	-1	μA
Low Level Input Current, Pull-up Resistor PRU1	I_{ILPU}	3009	$V_{IN}=V_{SS}$, CMOS Buffers Note 2	180	690	μA
Low Level Input Current, Pull-down Resistor PRD1	I_{ILPD}	3009	$V_{IN}=V_{SS}$, CMOS Buffers Note 2	-	± 5	μA
High Level Input Current	I_{IH}	3010	$V_{IN}=V_{DD}$, CMOS Buffers	-	1	μA
High Level Input Current, Pull-up Resistor PRU1	I_{IHPU}	3010	$V_{IN}=V_{DD}$, CMOS Buffers Note 2	-	± 5	μA
High Level Input Current, Pull-down Resistor PRD1	I_{IHPD}	3010	$V_{IN}=V_{DD}$, CMOS Buffers Note 2	30	400	μA
Low Level Input Voltage	V_{IL}	-	PICV, PICV5 Buffers $V_{DD}=V_{DDmin}$	-	800	mV
High Level Input Voltage	V_{IH}	-	PICV, PICV5 Buffers $V_{DD}=V_{DDmax}$	2	-	V
Positive Trigger Threshold Voltage	V_{TP}	-	Note 5	1.4	2.08	V
Negative Trigger Threshold Voltage	V_{TN}	-	Note 5	0.99	1.51	V
Hysteresis Voltage	V_H	-	Note 5	370	-	mV
Output Leakage Current Third State, Low Level Applied	I_{OZL}	3020	$V_{OUT}=0V$, All Buffers $V_{DD}=3.6V$	-	-1	μA
Output Leakage Current Third State, High Level Applied	I_{OZH}	3021	$V_{OUT}=0V$, All Buffers $V_{DD}=3.6V$	-	1	μA

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1 [$V_{DD} = 2.5 \pm 0.2V, 3 \pm 0.3V, 3.3 \pm 0.3V$ (Note 6) $V_{CC} = 5 \pm 0.5V$ (Note 7)]	Limits		Units
				Min	Max	
Input Current, Cold Sparing	I_{ICS}	-	$V_{IN} = 0V$ to 3.6V, PICZ Buffers $V_{DD} = V_{SS} = 0V$	-	± 2	μA
Output Current, Cold Sparing	I_{OCS}	-	$V_{OUT} = 0V$ to 3.6V, PO11Z Buffers $V_{DD} = V_{SS} = 0V$	-	± 2	μA
Low Level Output Voltage	V_{OL}	3007	$V_{DD} = V_{DDmin}$, $V_{CC} = 4.5V$	-	400	mV
High Level Output Voltage	V_{OH}	3006	$V_{DD} = V_{DDmin}(2.5V)$, $V_{CC} = 4.5V$	2	-	V
			$V_{DD} = V_{DDmin}(3V, 3.3V)$, $V_{CC} = 4.5V$	2.4	-	V
Output Short Circuit Current, to V_{DD}	I_{OSN}	-	PO11 output at High Level shorted to V_{DD} Note 5	-	28	mA
Output Short Circuit Current, to V_{SS}	I_{OSP}	-	PO11 output at High Level shorted to V_{SS} Note 5	-	17	mA
Input Capacitance	C_{IN}	3012	Note 5	-	2.4	pF
Output Capacitance	C_{OUT}	3012	Note 5	-	5.6	pF
Input/Output Capacitance	$C_{I/O}$	3012	Note 5	-	6.6	pF
Timing	-	3003	See ASIC Sheet			ns

- 2.3.2 Notes to Electrical Measurements Tables
- Unless otherwise specified: all inputs and outputs shall be tested for each characteristic; Inputs not under test shall be $V_{IN} = V_{SS}$, V_{CC} or V_{DD} and outputs not under test shall be open; $V_{SS} = 0V$.
 - Standard pull-ups: PRU# where # = [1-31] index for Ron:
 $R_{on} = \# \times R_0 = 19k\Omega$ typical (12 to 30k Ω) in 2.5V range.
 $R_{on} = \# \times R_0 = 15k\Omega$ typical (10 to 25k Ω) in 3V range.
 $R_{on} = \# \times R_0 = 14k\Omega$ typical (9 to 25k Ω) in 3.3V range.
 5V tolerant/compliant pull-ups: PRU# where # = [1-31] index for Ron:
 $R_{on} = \# \times R_0 = 14k\Omega$ typical (8 to 25k Ω) in each range.

 Standard pull-downs: PRD# where # = [1-31] index for Ron:
 $R_{on} = \# \times R_0 = 11k\Omega$ typical (5 to 30k Ω) in 2.5V range.
 $R_{on} = \# \times R_0 = 9k\Omega$ typical (4 to 25k Ω) in 3V range.
 $R_{on} = \# \times R_0 = 8k\Omega$ typical (4 to 20k Ω) in 3.3V range.
 5V tolerant/compliant pull-downs: PRD# where # = [1-31] index for Ron:
 $R_{on} = \# \times R_0 = 36k\Omega$ typical (17 to 80k Ω) in 2.5V range.
 $R_{on} = \# \times R_0 = 23k\Omega$ typical (11 to 55k Ω) in 3V range.
 $R_{on} = \# \times R_0 = 19k\Omega$ typical (9 to 45k Ω) in 3.3V range.

3. Output buffers: PO\$# where
\$ = [1-12] quantity of output driving capability of p-channels.
#=[1-12] quantity of output driving capability of n-channels.
Standard buffers (including cold sparing)
IO = 1.6, 1.8, 2mA measured at $V_{OL} = 400, 400, 400\text{mV}$ in 2.5, 3, 3.3V range respectively.
Tolerance buffers (including cold sparing)
IO = 1, 1.3, 1.4mA measured at $V_{OL} = 400, 400, 400\text{mV}$ in 2.5, 3, 3.3V range respectively.
Compliant buffers ($V_{CC} = 4.5\text{V}$)
IO = 1.1, 1.4, 1.6mA measured at $V_{OL} = 400, 400, 400\text{mV}$ in 2.5, 3, 3.3V range respectively.
4. Output buffers: PO\$# where
\$ = [1-12] quantity of output driving capability of p-channels.
#=[1-12] quantity of output driving capability of n-channels.
Standard buffers (including cold sparing)
IO = -1.6, -1.8, -2mA measured at $V_{OL} = 2, 2.4, 2.4\text{V}$ in 2.5, 3, 3.3V range respectively.
Tolerance buffers (including cold sparing)
IO = -1, -1.3, -1.4mA measured at $V_{OL} = 2, 2.4, 2.4\text{V}$ in 2.5, 3, 3.3V range respectively.
Compliant buffers ($V_{CC} = 4.5\text{V}$)
IO = -1.1, -1.4, -1.6mA measured at $V_{OL} = 2, 2.4, 2.4\text{V}$ in 2.5, 3, 3.3V range respectively.
5. Guaranteed but not tested.
6. 5V tolerant buffers.
7. 5V compliant buffers.

2.3.3 High and Low Temperatures Electrical Measurements

Unless otherwise specified the measurements shall be performed at $T_{amb} = +125 (+0 -5)^{\circ}\text{C}$ and $T_{amb} = -55 (+5 - 0)^{\circ}\text{C}$. Unless otherwise specified the characteristics, test methods, conditions and limits shall be the same as specified for Room Temperature Electrical Measurements.

2.4 PARAMETER DRIFT VALUES

Unless otherwise specified, the measurements shall be performed at $T_{amb} = +22 \pm 3^{\circ}\text{C}$.

The test methods and test conditions shall be as per the corresponding test defined in Room Temperature Electrical Measurements.

The drift values (Δ) shall not be exceeded for each characteristic specified. The corresponding absolute limit values for each characteristic shall not be exceeded.

Characteristics	Symbols	Limits			Units
		Drift Value Δ	Absolute		
			Min	Max	
Supply Current, Stand-by	I_{DDSB}	See ASIC Sheet			mA
Low Level Input Current	I_{IL}	± 0.1	-	-1	μA
High Level Input Current	I_{IH}	± 0.1	-	1	μA
Output Leakage Current Third State, Low Level Applied	I_{OZL}	± 0.1	-	-1	μA
Output Leakage Current Third State, High Level Applied	I_{OZH}	± 0.1	-	1	μA
Low Level Output Voltage	V_{OL}	± 100	-	400	mV
High Level Output Voltage	V_{OH}	± 0.1	2.4 or 2	-	V

NOTES:

1. Unless otherwise specified all inputs and outputs shall be tested for each characteristic.

2.5 INTERMEDIATE AND END-POINT ELECTRICAL MEASUREMENTS

Unless otherwise specified, the measurements shall be performed at $T_{amb} = +22 \pm 3^{\circ}C$. Unless otherwise specified the characteristics, test methods, conditions and limits shall be the same as specified for Room Temperature Electrical Measurements.

2.6 POWER BURN-IN CONDITIONS

See ASIC Sheet.

2.7 OPERATING LIFE CONDITIONS

Unless otherwise specified the conditions shall be as specified for Power Burn-in.

2.8 TOTAL DOSE RADIATION TESTING

2.8.1 Bias Conditions and Total Dose Level for Total Dose Radiation Testing

Continuous bias shall be applied during irradiation testing as specified in the ASIC Sheet.

The total dose level applied shall be as specified in the component type variant information herein, in the ASIC Sheet or in the Purchase Order.

2.8.2 Electrical Measurements for Total Dose Radiation Testing

Prior to irradiation testing the devices shall have successfully met Room Temperature Electrical Measurements specified herein.

Unless otherwise stated the measurements shall be performed at $T_{amb} = +22 \pm 3^{\circ}C$.

The test methods and test conditions shall be as per the corresponding test defined in Room Temperature Electrical Measurements.

The parameters to be measured during and on completion of irradiation testing are specified in the ASIC Sheet.