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INTEGRATED CIRCUITS, SILICON MONOLITHIC, CMOS 8K X 16 DUAL-PORT STATIC RANDOM ACCESS MEMORY WITH THREE STATE OUTPUTS

BASED ON TYPE 67025E

ESCC Detail Specification No. 9301/050

Issue 1	October 2007

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DOCUMENTATION CHANGE NOTICE

(Refer to https://escies.org for ESCC DCR content)

DCR No.	CHANGE DESCRIPTION

TABLE OF CONTENTS

1. GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics and test and inspection data for the component type variants and/or the range of components specified below. It supplements the requirements of, and shall be read in conjunction with, the ESCC Generic Specification listed under Applicable Documents.

1.2 APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:

(a) ESCC Generic Specification No. 9000
(b) MIL-STD-883, Test Methods and Procedures for Microelectronics

1.3 TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESCC Basic Specification No. 21300 shall apply.

1.4 THE ESCC COMPONENT NUMBER AND COMPONENT TYPE VARIANTS

1.4.1 The ESCC Component Number

The ESCC Component Number shall be constituted as follows:

Example: 930105001D

- Detail Specification Reference: 9301050
- Component Type Variant Number: 01 (as required)
- Total Dose Radiation Level Letter: D (as required)

1.4.2 Component Type Variants

The component type variants applicable to this specification are as follows:

Variant Number	Based on Type	Access Time (ns)	Case	Lead/Terminal Material and Finish	Weight max g	Total Dose Radiation Level Letter
01	67025E-30	30	MQFP-F84	G2	5	D [10kRAD(Si)]
02	67025E-45	45	MQFP-F84	G2	5	D [10kRAD(Si)]

The lead/terminal material and finish shall be in accordance with the requirements of ESCC Basic Specification No. 23500.

The total dose radiation level letter shall be as defined in ESCC Basic Specification No. 22900. If an alternative radiation test level is specified in the Purchase Order the letter shall be changed accordingly.

1.5 MAXIMUM RATINGS

The maximum ratings shall not be exceeded at any time during use or storage.

Maximum ratings shall only be exceeded during testing to the extent specified in this specification and when stipulated in Test Methods and Procedures of the ESCC Generic Specification.

Characteristics	Symbols	Maximum Ratings	Units	Remarks
Supply Voltage	V_{DD}	-0.5 to 7	V	Note 1
Input Voltage Range	V_{IN}	-0.5 to V_{DD} +0.3	V	Notes 1, 2
Output Voltage Range	V_{OUT}	-0.5 to V_{DD} +0.3	V	Notes 1, 2
Output Current Connected to V_{DD} V_{SS}	 I_{O+} I_{O-}	 120 -60	mA	Note 3
Device Power Dissipation	P_D	1.8	W	
Operating Temperature Range	T_{op}	-55 to +125	^oC	T_{amb}
Storage Temperature Range	T_{stg}	-65 to +150	^oC	
Soldering Temperature	T_{sol}	+265	^oC	Note 4
Junction Temperature	T_j	+165	^oC	Note 5
Thermal Resistance, Junction to Case	$R_{th(j-c)}$	6	$^oC/W$	

NOTES:

1. All voltages are with respect to V_{SS}. Device is functional for $4.5 \leq V_{DD} \leq 5.5V$.
2. V_{DD} +0.3V shall not exceed 7V.
3. The maximum output current of any single output.
4. Duration 10 seconds maximum at a distance of not less than 1.6mm from the device body and the same terminal shall not be resoldered until 3 minutes have elapsed.
5. Maximum junction temperature may be increased to $+175^oC$ during Power Burn-in and Operating Life.

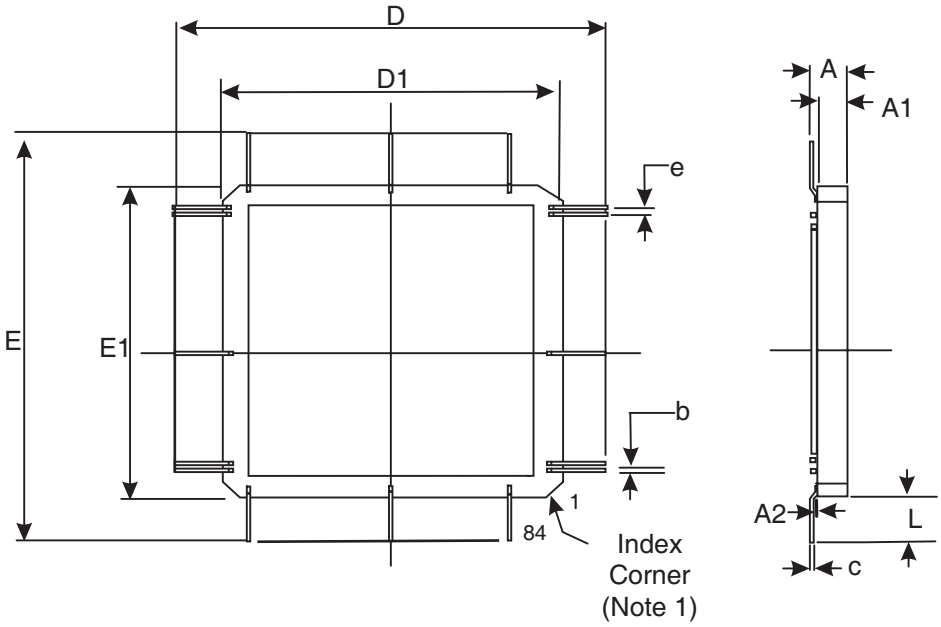
1.6 HANDLING PRECAUTIONS

These devices are susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacture, testing, packaging, shipment and any handling.

These components are categorised as Class 1 per ESCC Basic Specification 23800 with a Minimum Critical Path Failure Voltage of 1000 Volts.

1.7 PHYSICAL DIMENSIONS AND TERMINAL IDENTIFICATION

1.7.1 Multilayer Quad Flat Package (MQFP-F84) - 84 Lead

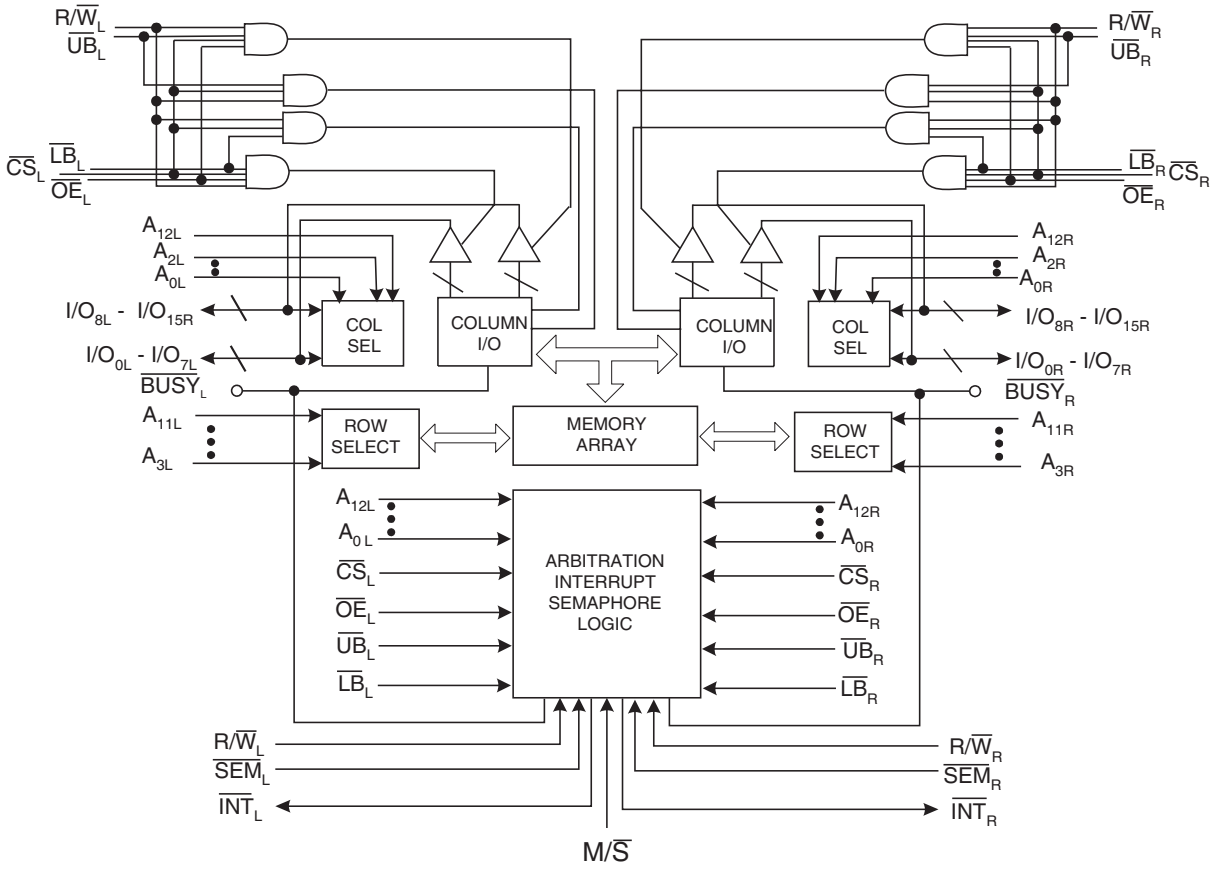


Symbols	Dimensions (mm)		Notes
	Min	Max	
A	2.05	2.89	2
A1	1.82	2.67	
A2	-	0.356	2
b	0.406	0.508	2, 4
c	0.22	0.31	2
D, E	44.16	45.86	
D1, E1	28.96	29.46	
e	1.27 BSC		2, 3
L	7.6	8.2	2

NOTES:

1. Index mark: a notch or lead 1 identification mark shall be located adjacent to lead 1.
2. All terminals.
3. 80 places. The true position pin spacing is 1.27mm between centrelines. Each lead centreline shall be located within ±0.13mm of its true longitudinal position relative to the package centrelines.
4. 21 leads per side.

1.8 FUNCTIONAL DIAGRAM



1.9 PIN ASSIGNMENT

Pin	Function
1	I/O8L Input/Output (Left Port)
2	I/O9L Input/Output (Left Port)
3	I/O10L Input/Output (Left Port)
4	I/O11L Input/Output (Left Port)
5	I/O12L Input/Output (Left Port)
6	I/O13L Input/Output (Left Port)
7	V_{SS}
8	I/O14L Input/Output (Left Port)
9	I/O15L Input/Output (Left Port)
10	V_{DD}
11	V_{SS}
12	I/O0R Input/Output (Right Port)

Pin	Function
13	I/O1R Input/Output (Right Port)
14	I/O2R Input/Output (Right Port)
15	V_{DD}
16	I/O3R Input/Output (Right Port)
17	I/O4R Input/Output (Right Port)
18	I/O5R Input/Output (Right Port)
19	I/O6R Input/Output (Right Port)
20	I/O7R Input/Output (Right Port)
21	I/O8R Input/Output (Right Port)
22	I/O9R Input/Output (Right Port)
23	I/O10R Input/Output (Right Port)
24	I/O11R Input/Output (Right Port)
25	I/O12R Input/Output (Right Port)
26	I/O13R Input/Output (Right Port)
27	I/O14R Input/Output (Right Port)
28	V_{SS}
29	I/O15R Input/Output (Right Port)
30	$\overline{OE}$R Input (Output Enable, Right Port)
31	R/$\overline{W}$R Input (Read/Write Enable, Right Port)
32	V_{SS}
33	$\overline{SEM}$R Input (Semaphore Enable, Right Port)
34	$\overline{CS}$R Input (Chip Select, Right Port)
35	$\overline{UB}$R Input (Upper Byte Select, Right Port)
36	$\overline{LB}$R Input (Lower Byte Select, Right Port)
37	A12R Input (Address, Right Port)
38	A11R Input (Address, Right Port)
39	A10R Input (Address, Right Port)
40	A9R Input (Address, Right Port)
41	A8R Input (Address, Right Port)
42	A7R Input (Address, Right Port)
43	A6R Input (Address, Right Port)
44	A5R Input (Address, Right Port)
45	A4R Input (Address, Right Port)
46	A3R Input (Address, Right Port)
47	A2R Input (Address, Right Port)
48	A1R Input (Address, Right Port)

Pin	Function
49	A0R Input (Address, Right Port)
50	$\overline{\text{INT}}$R Output (Interrupt Flag, Right Port)
51	$\overline{\text{BUSY}}$R Input (Slave)/Output (Master) (Busy Flag, Right Port)
52	M/$\overline{\text{S}}$ Input (Master or Slave Select)
53	V_{SS}
54	$\overline{\text{BUSY}}$L Input (Slave)/Output (Master) (Busy Flag, Left Port)
55	$\overline{\text{INT}}$L Output (Interrupt Flag, Left Port)
56	A0L Input (Address, Left Port)
57	A1L Input (Address, Left Port)
58	A2L Input (Address, Left Port)
59	A3L Input (Address, Left Port)
60	A4L Input (Address, Left Port)
61	A5L Input (Address, Left Port)
62	A6L Input (Address, Left Port)
63	A7L Input (Address, Left Port)
64	A8L Input (Address, Left Port)
65	A9L Input (Address, Left Port)
66	A10L Input (Address, Left Port)
67	A11L Input (Address, Left Port)
68	A12L Input (Address, Left Port)
69	$\overline{\text{LB}}$L Input (Lower Byte Select, Left Port)
70	$\overline{\text{UB}}$L Input (Upper Byte Select, Left Port)
71	$\overline{\text{CS}}$L Input (Chip Select, Left Port)
72	$\overline{\text{SEM}}$L Input (Semaphore Enable, Left Port)
73	R/$\overline{\text{W}}$L Input (Read/Write Enable, Left Port)
74	V_{DD}
75	$\overline{\text{OE}}$L Input (Output Enable, Left Port)
76	I/O0L Input/Output (Left Port)
77	I/O1L Input/Output (Left Port)
78	V_{SS}
79	I/O2L Input/Output (Left Port)
80	I/O3L Input/Output (Left Port)
81	I/O4L Input/Output (Left Port)
82	I/O5L Input/Output (Left Port)

Pin	Function
83	I/O6L Input/Output (Left Port)
84	I/O7L Input/Output (Left Port)

1.10 TRUTH TABLES AND TIMING DIAGRAMS

Consolidated notes for the truth table and the instruction set follow the tables.

1.10.1 Non Contention and Semaphore Read/Write Control

Inputs						Outputs		Mode
$\overline{CS}$	R/$\overline{W}$	$\overline{OE}$	$\overline{UB}$	$\overline{LB}$	$\overline{SEM}$	I/O8 - I/O15	I/O0 - I/O7	
H	X	X	X	X	H	Z	Z	Deselected: Power Down (Note 2)
X	X	X	H	H	H	Z	Z	Both Bytes Deselected: Power Down (Note 2)
L	L	X	L	H	H	$DATA_{IN}$	Z	Write to Upper Byte Only (Note 2)
L	L	X	H	L	H	Z	$DATA_{IN}$	Write to Lower Byte Only (Note 2)
L	L	X	L	L	H	$DATA_{IN}$	$DATA_{IN}$	Write to Both Bytes (Note 2)
L	H	L	L	H	H	$DATA_{OUT}$	Z	Read Upper Byte Only (Note 2)
L	H	L	H	L	H	Z	$DATA_{OUT}$	Read Lower Byte Only (Note 2)
L	H	L	L	L	H	$DATA_{OUT}$	$DATA_{OUT}$	Read Both Bytes (Note 2)
X	X	H	X	X	X	Z	Z	Outputs Disabled (Note 2)
H	H	L	X	X	L	$DATA_{OUT}$	$DATA_{OUT}$	Read Data in Semaphore Flag
X	H	L	H	H	L	$DATA_{OUT}$	$DATA_{OUT}$	Read Data in Semaphore Flag
H	↑	X	X	X	L	$DATA_{IN}$	$DATA_{IN}$	Write D_{IN0} into Semaphore Flag
X	↑	X	H	H	L	$DATA_{IN}$	$DATA_{IN}$	Write D_{IN0} into Semaphore Flag
L	X	X	L	X	L	-	-	Not Allowed
L	X	X	X	L	L	-	-	Not Allowed

1.10.2 Arbitration Options

Options	Inputs					Outputs	
	$\overline{CS}$	$\overline{UB}$	$\overline{LB}$	M/$\overline{S}$	$\overline{SEM}$	$\overline{BUSY}$	$\overline{INT}$
Busy Logic Master	L	X	L	H	H	Output	-
	L	L	X	H	H	Signal	-
Busy Logic Slave	L	X	L	L	H	Input	-
	L	L	X	L	H	Signal	-
Interrupt Logic	L	X	L	X	H	-	Output
	L	L	X	X	H	-	Signal
Semaphore Logic (Note 3)	H	X	X	H	L	H	-
	H	X	X	L	L	Z	-

1.10.3 Interrupt Flag

Left Port					Right Port					Function Note 4
R/$\overline{W}$L	$\overline{CS}$L	$\overline{OE}$L	A0L - A12L	$\overline{INT}$L	R/$\overline{W}$R	$\overline{CS}$R	$\overline{OE}$R	A0R - A12R	$\overline{INT}$R	
L	L	X	1FFF	X	X	X	X	X	L (5)	Set Right $\overline{INT}$R Flag
X	X	X	X	X	X	L	L	1FFF	H (6)	Reset Right $\overline{INT}$R Flag
X	X	X	X	L (6)	L	L	X	1FFE	X	Set Left $\overline{INT}$L Flag
X	L	L	1FFE	H (5)	X	X	X	X	X	Reset Left $\overline{INT}$L Flag

1.10.4 Arbitration

Left Port		Right Port		Flags Note 7		Function
$\overline{CS}$L	A0L - A12L	$\overline{CS}$R	A0R - A12R	$\overline{BUSY}$L	$\overline{BUSY}$R	
H	X	H	X	H	H	No Contention
L	Any	H	X	H	H	No Contention
H	X	L	Any	H	H	No Contention
L	≠A0R - A12R	L	≠A0L - A12L	H	H	No Contention
Address Arbitration With $\overline{CS}$ Low Before Address Match						
L	LV5R	L	LV5R	H	L	L-Port Wins
L	RV5L	L	RV5L	L	H	R-Port Wins
L	Same	L	Same	H	L	Arbitration Resolved
L	Same	L	Same	L	H	Arbitration Resolved
$\overline{CS}$ Arbitration With Address Match Before $\overline{CS}$						
LL5R	= A0R - A12R	LL5R	= A0L - A12L	H	L	L-Port Wins

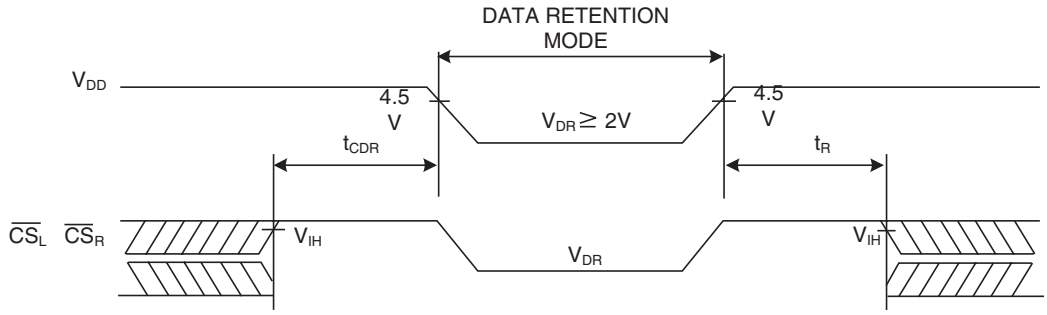
Left Port		Right Port		Flags Note 7		Function
$\overline{CS}$L	A0L - A12L	$\overline{CS}$R	A0R - A12R	$\overline{BUSY}$L	$\overline{BUSY}$R	
RL5L	= A0R - A12R	RL5L	= A0L - A12L	L	H	R-Port Wins
LW5R	= A0R - A12R	LW5R	= A0L - A12L	H	L	Arbitration Resolved
LW5R	= A0R - A12R	LW5R	= A0L - A12L	L	H	Arbitration Resolved

1.10.5 Consolidated Notes for Truth Tables

1. Logic Level Definitions: L = Low Level, H = High Level, X = Irrelevant, Z = High Impedance, ↑ = Rising edge of signal, NC = No Change, LV5R = Left Address Valid ≥ 5ns before Right Address, RV5L = Right Address Valid ≥ 5ns before Left Address, Same = Left and Right Addresses match within 5ns of each other, LL5R = $\overline{CS}$L = Low ≥5ns before $\overline{CS}$R, RL5L = $\overline{CS}$R = Low ≥5ns before $\overline{CS}$L, LW5R = $\overline{CS}$L and $\overline{CS}$R = Low within 5ns of each other.
2. A0L - A12L ≠ A0R - A12R.
3. Input Signals are for Semaphore Flags set and test (Write and Read) operations.
4. Assumes $\overline{BUSY}$L = $\overline{BUSY}$R = H.
5. If $\overline{BUSY}$L = L, then NC.
6. If $\overline{BUSY}$R = L, then NC.
7. $\overline{INT}$L, $\overline{INT}$R flags = X.

1.10.6 Timing Diagrams

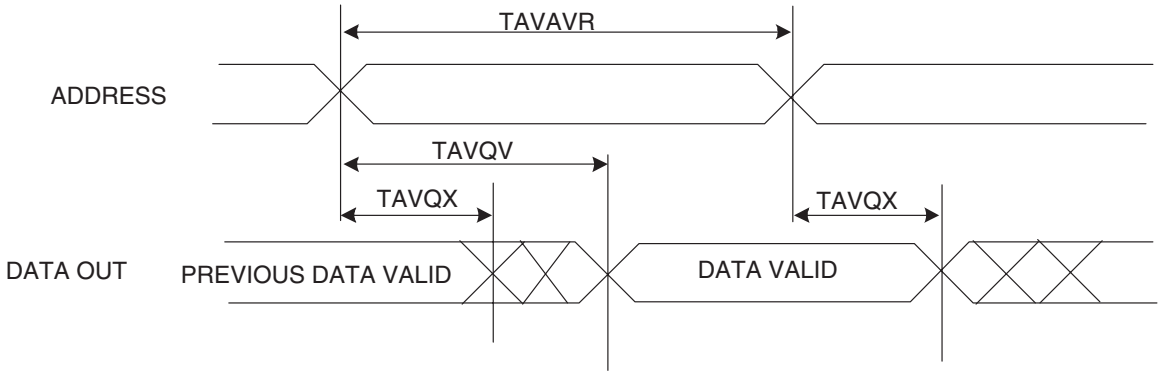
Data Retention (Notes 1, 2, 3)



NOTES:

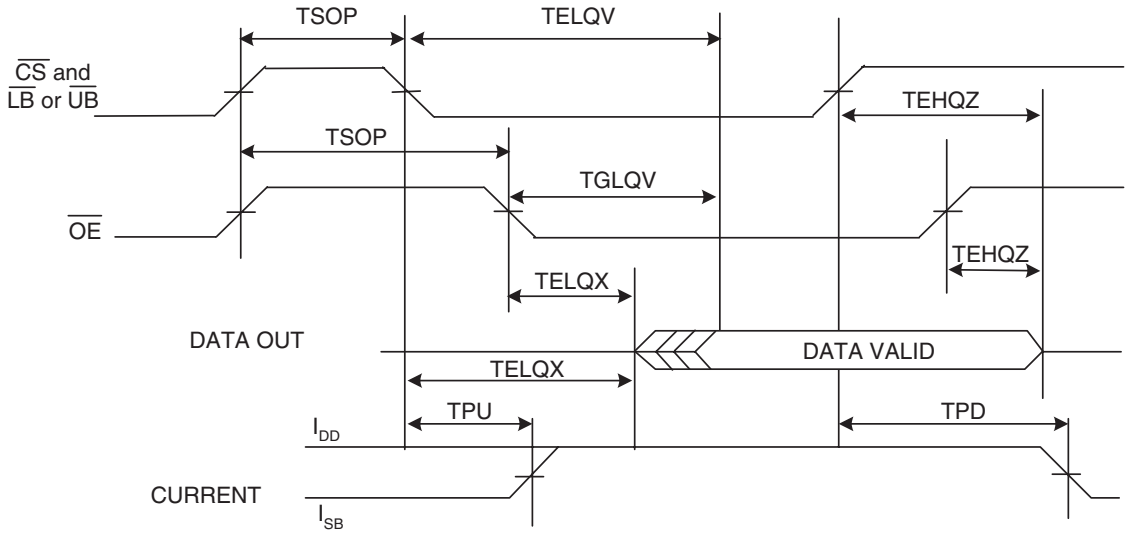
1. Chip select ($\overline{CS}$L, $\overline{CS}$R) must be held high during data retention within V_{DD} to V_{DD}-0.2V.
2. $\overline{CS}$L, $\overline{CS}$R must be kept between V_{DD} - 0.2V and 70% of V_{DD} during the power up and power down transitions.
3. The RAM shall begin operation > t_R after V_{DD} reaches the minimum operating voltage (4.5 Volts).

Read Cycle 1, Either Side (Notes 1, 2, 3)



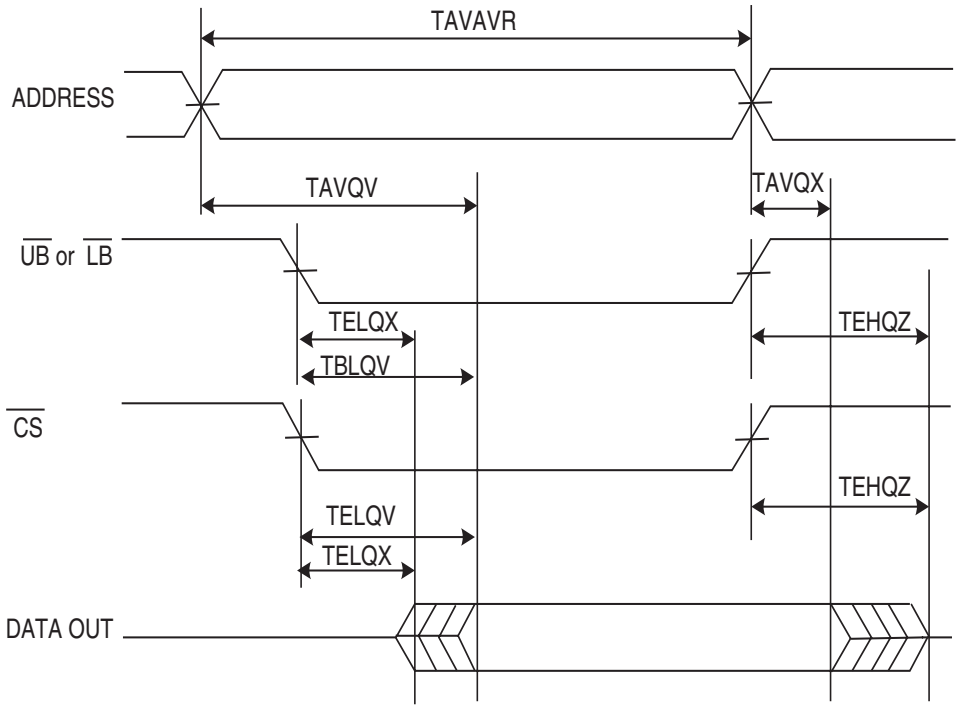
NOTES:
1. R/$\overline{W}$ is high for read cycles.
2. Device is continuously enabled: $\overline{CS}$ = V_{IL}, $\overline{UB}$ or $\overline{LB}$ = V_{IL}. This waveform cannot be used for semaphore reads.
3. $\overline{OE}$ = V_{IL}.

Read Cycle 2, Either Side (Notes 1, 2, 3, 4)



NOTES:
1. R/$\overline{W}$ is high for read cycles.
2. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
3. To access RAM, $\overline{CS}$ = V_{IL}, $\overline{UB}$ or $\overline{LB}$ = V_{IL}, $\overline{SEM}$ = V_{IH}. To access semaphore, $\overline{CS}$ = V_{IH}, $\overline{SEM}$ = V_{IL}. Refer to Non Contention and Semaphore Read/Write Control table.
4. $\overline{OE}$ = V_{IL}.

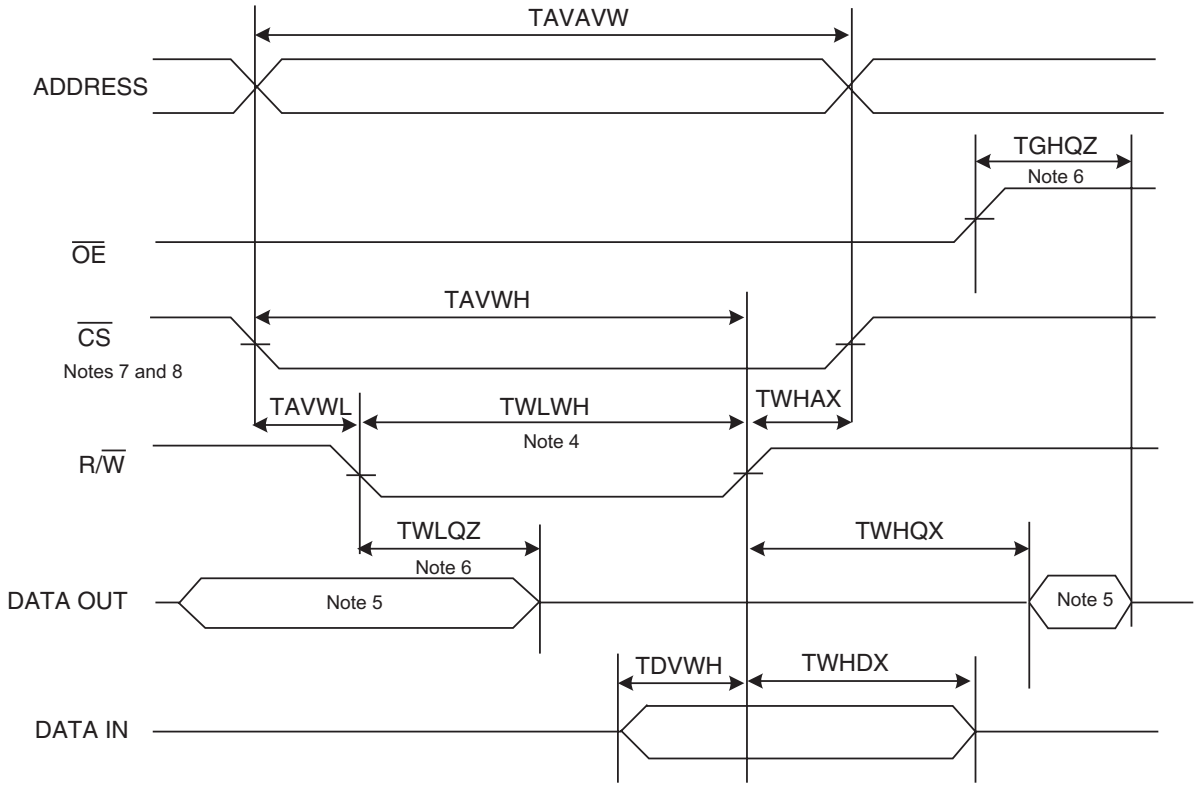
Read Cycle 3, Either Side (Notes 1, 2, 3, 4)



NOTES:

1. R/$\overline{W}$ is high for read cycles.
2. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
3. To access RAM, $\overline{CS} = V_{IL}$, $\overline{UB}$ or $\overline{LB} = V_{IL}$, $\overline{SEM} = V_{IH}$. To access semaphore, $\overline{CS} = V_{IH}$, $\overline{SEM} = V_{IL}$. Refer to Non Contention and Semaphore Read/Write Control table.
4. $\overline{OE} = V_{IL}$.

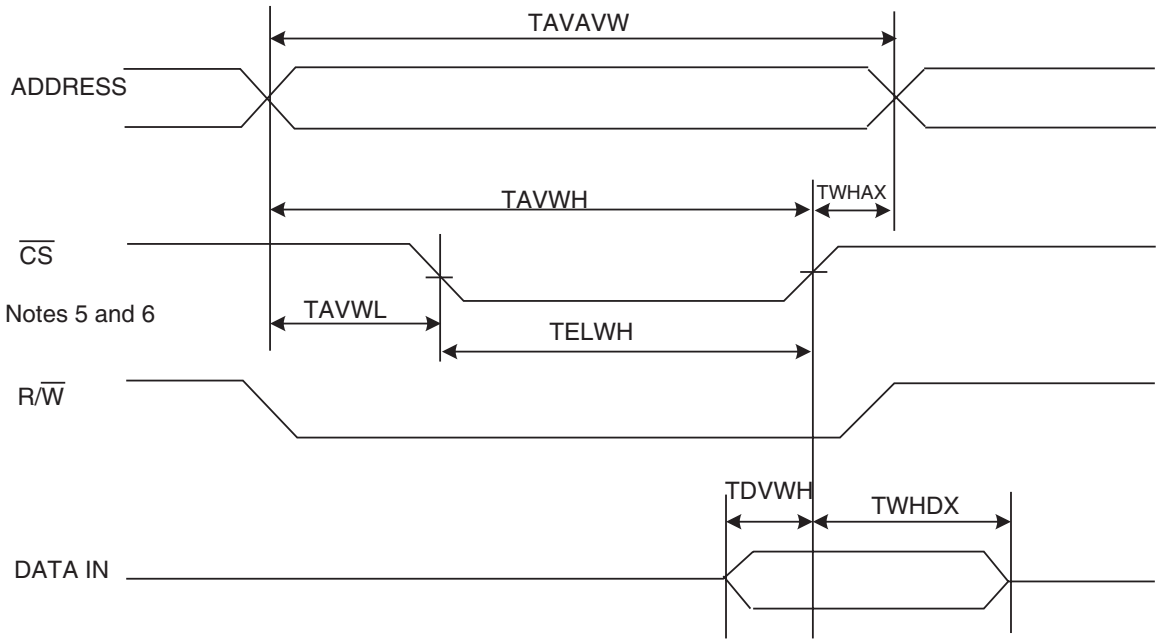
Write Cycle 1 (R/$\overline{W}$ Controlled) (Notes 1, 2, 3, 4)



NOTES:

1. R/$\overline{W}$ must be high during all address transitions.
2. A write occurs during the overlap (TWLWH) of a low $\overline{CS}$ or $\overline{SEM}$ and a low R/$\overline{W}$.
3. TWHAX is measured from the earlier of $\overline{CS}$ or R/$\overline{W}$ (or $\overline{SEM}$ or R/$\overline{W}$) going high to the end of write cycle.
4. If $\overline{OE}$ is low during an R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of TWLWH or (TWLQZ+TDVWH) to allow the I/O drivers to turn off and data to be placed on the bus for the required TDVWH. If $\overline{OE}$ is high during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified TWLWH.
5. During this period, the I/O pins are in the output state, and input signals must not be applied.
6. Transition is measured ±500mV from steady state with a 5pF load (including scope and jig). This parameter is sampled and not 100% tested.
7. To access RAM, $\overline{CS}$ = V_{IL}, $\overline{SEM}$ = V_{IH}.
8. To access upper byte, $\overline{CS}$ = V_{IL}, $\overline{UB}$ = V_{IL}, $\overline{SEM}$ = V_{IH}. To access lower byte, $\overline{CS}$ = V_{IL}, $\overline{LB}$ = V_{IL}, $\overline{SEM}$ = V_{IH}.

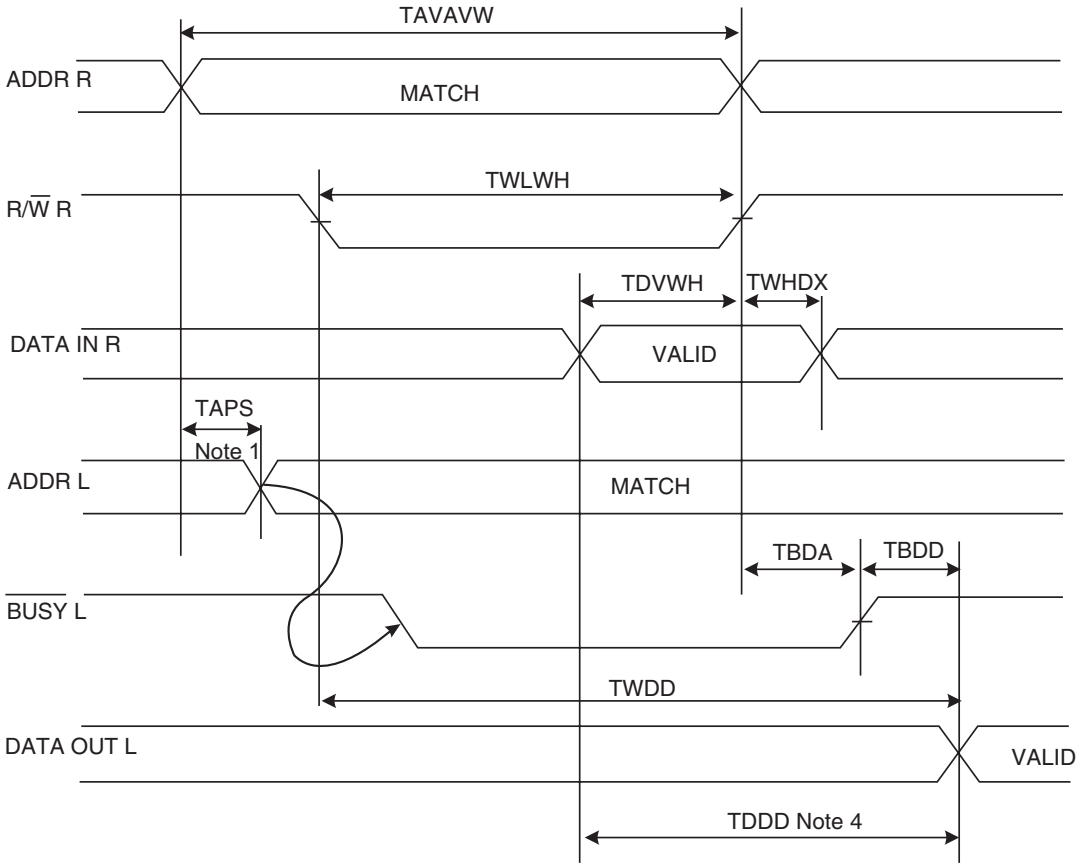
Write Cycle 2 ($\overline{CS}$ Controlled) (Notes 1, 2, 3, 4)



NOTES:

1. $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (TELWH) of a low $\overline{CS}$ or $\overline{SEM}$ and a low R/$\overline{W}$.
3. TWHAX is measured from the earlier of $\overline{CS}$ or R/$\overline{W}$ (or $\overline{SEM}$ or R/$\overline{W}$) going high to the end of write cycle.
4. If the $\overline{CS}$ or $\overline{SEM}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
5. To access RAM, $\overline{CS} = V_{IL}$. $\overline{SEM} = V_{IH}$.
6. To access upper byte $\overline{CS} = V_{IL}$, $\overline{UB} = V_{IL}$, $\overline{SEM} = V_{IH}$. To access lower byte, $\overline{CS} = V_{IL}$, $\overline{LB} = V_{IL}$, $\overline{SEM} = V_{IH}$.

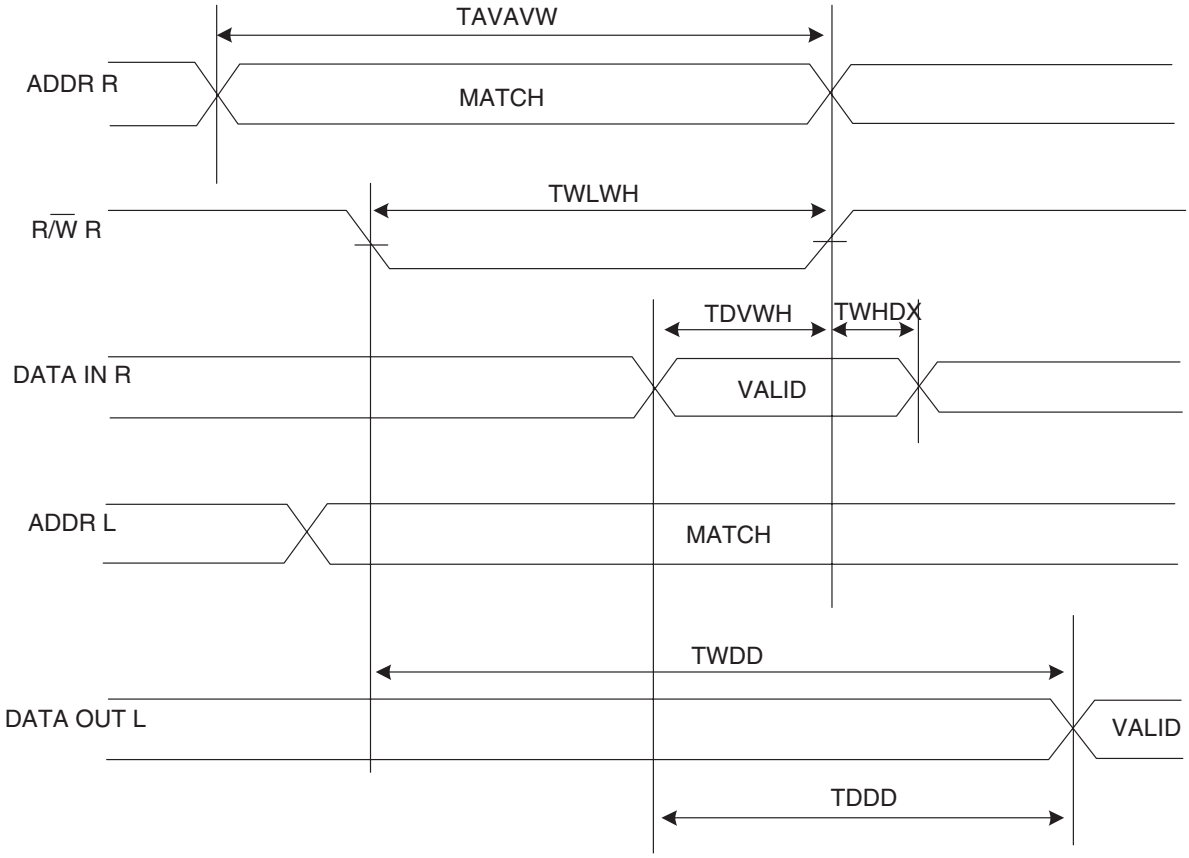
Arbitration Read with Busy for Master 67025E (Notes 2, 3, 4)



NOTES:

1. To ensure that the earlier of the 2 ports wins.
2. Write cycle parameters should be adhered to, to ensure proper writing.
3. Device is continuously enabled for both ports.
4. $\overline{OE}$ is low for the reading port.

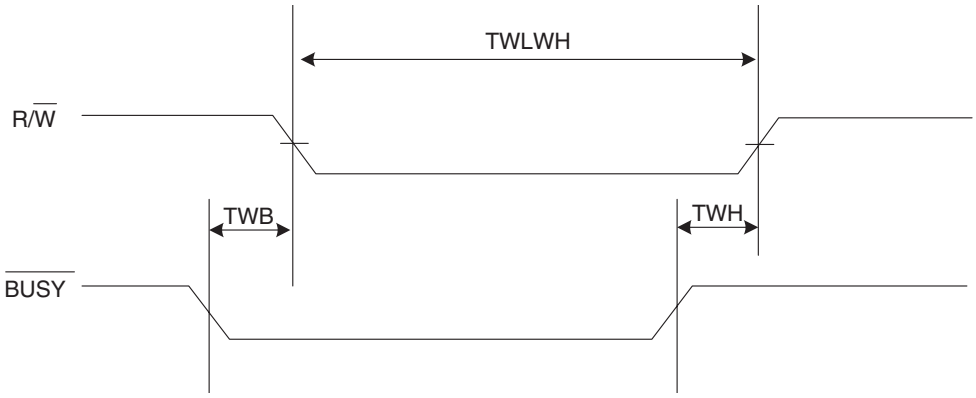
Arbitration Write with Port-to-Port for Slave 67025E (Notes 1, 2, 3)



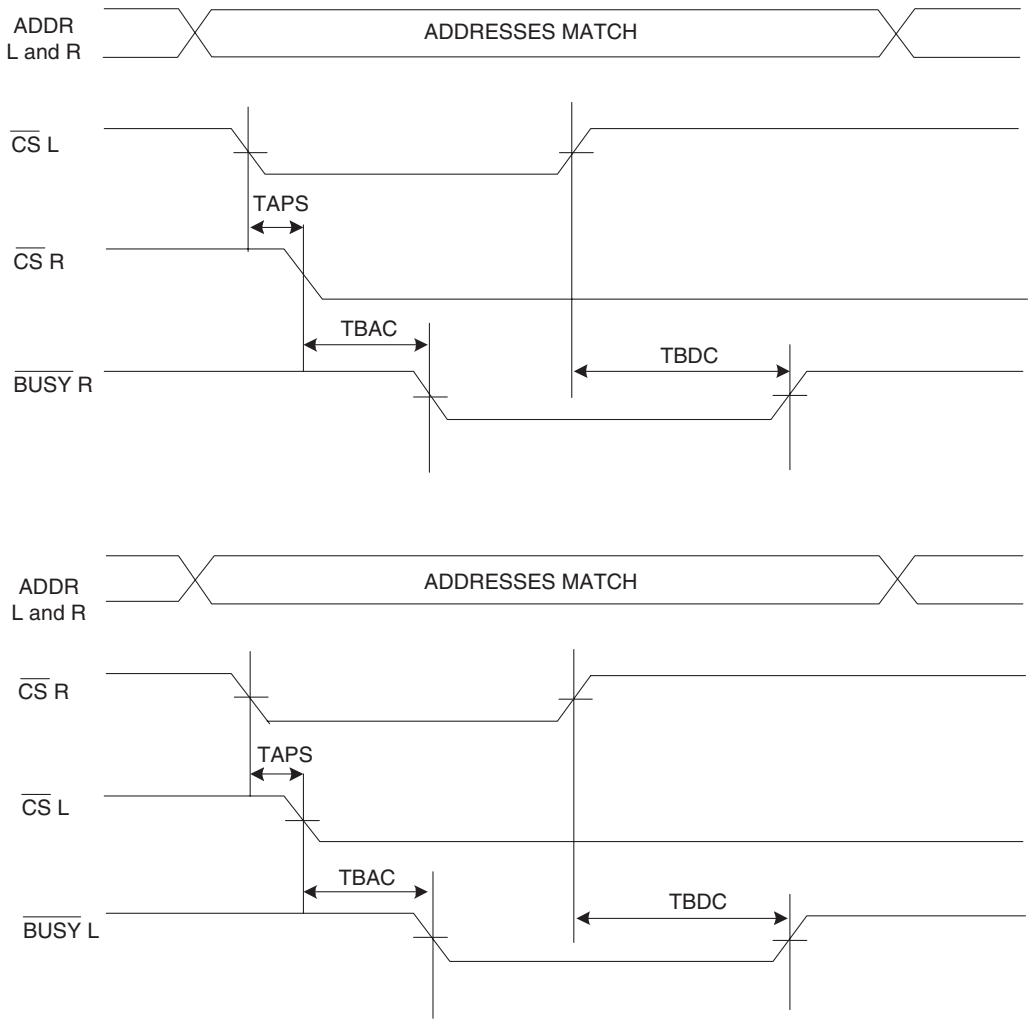
NOTES:

1. Assume $\overline{BUSY}$ is high for the writing port and $\overline{OE}$ is low for the reading port.
2. Write cycle parameters should be adhered to ensure proper writing.
3. Device is continuously enabled for both ports.

Write with Busy for Slave 67025E

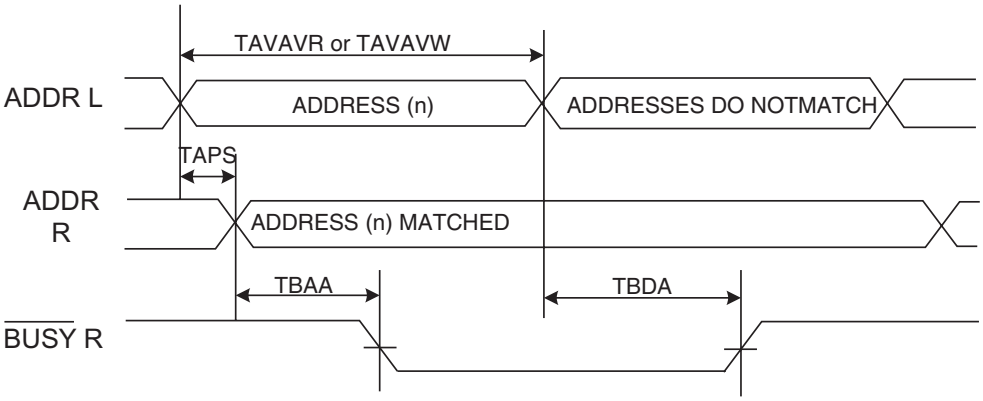


Contention Cycle No. 1 - $\overline{CS}$ Arbitration for Master 67025E

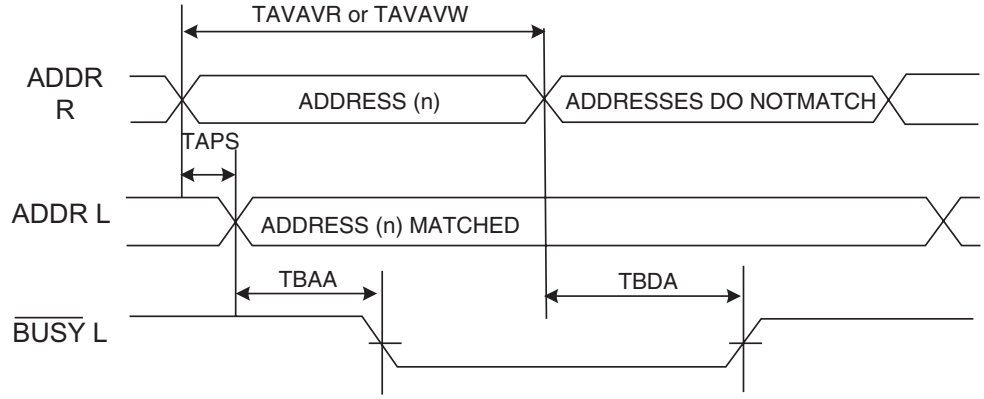


Contention Cycle No. 2 - Address Valid Arbitration for Master 67025E (Note 1)

Left Address Valid First:



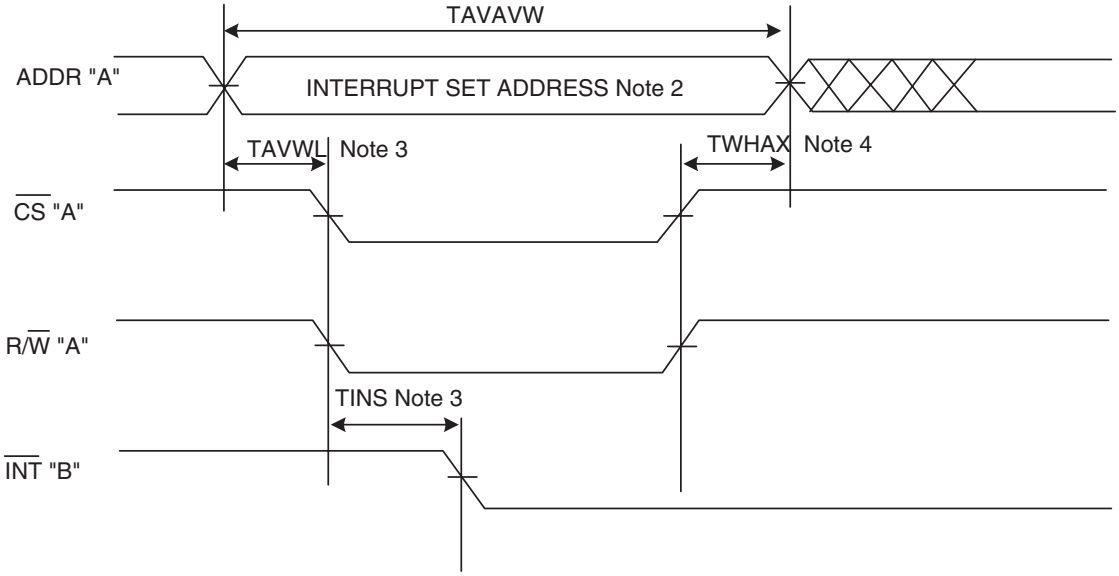
Right Address Valid First:

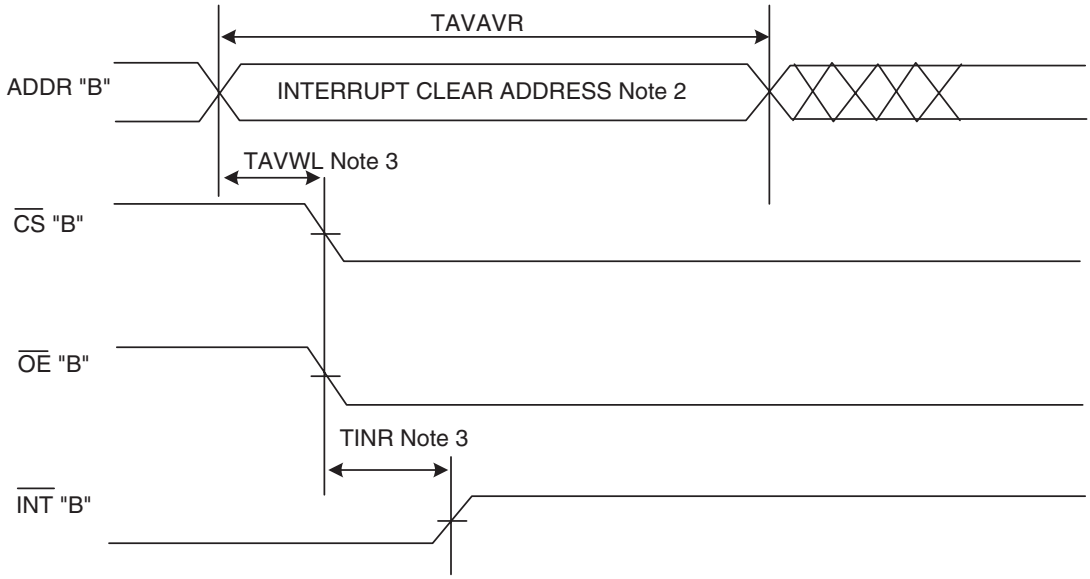


NOTES:

1. $\overline{CS}R = \overline{CS}L = V_{IL}$.

Interrupt Timing (Note 1)

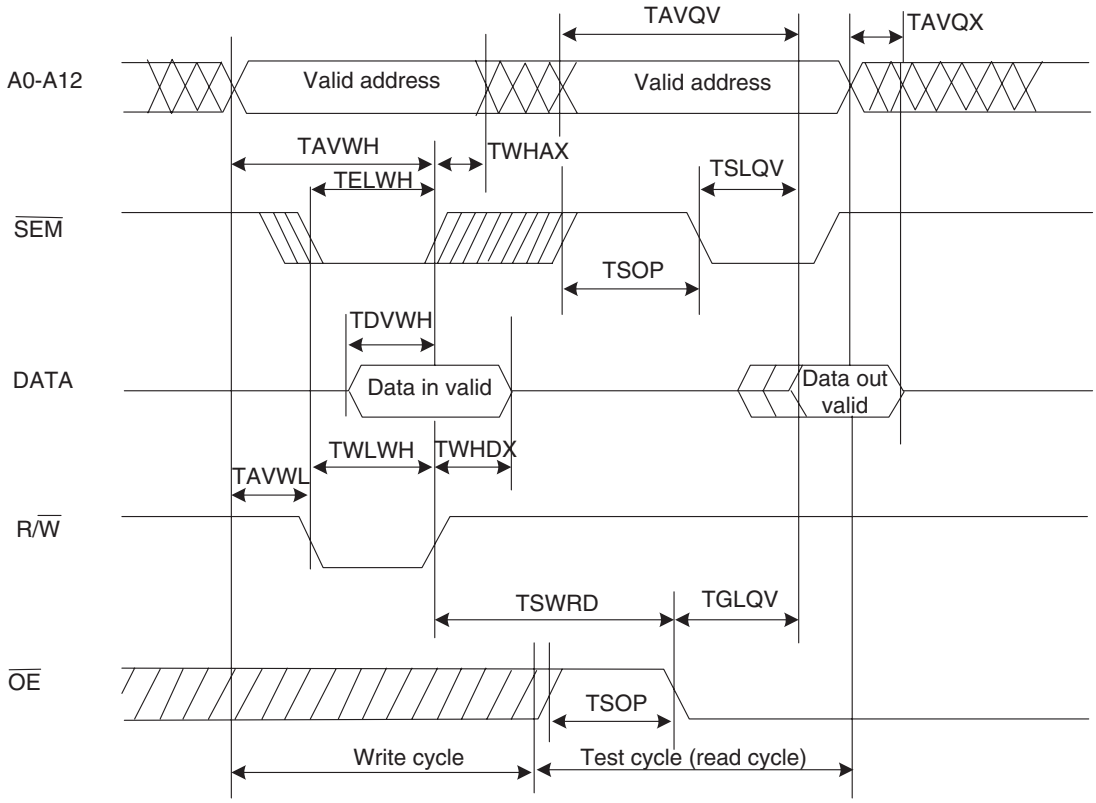




NOTES:

1. All timings are the same for both ports. Port “A” may be either the left or right port. Port “B” is the port opposite to “A”.
2. See interrupt truth table.
3. Timing depends on which enable signal is asserted last.
4. Timing depends on which enable signal is de-asserted first.

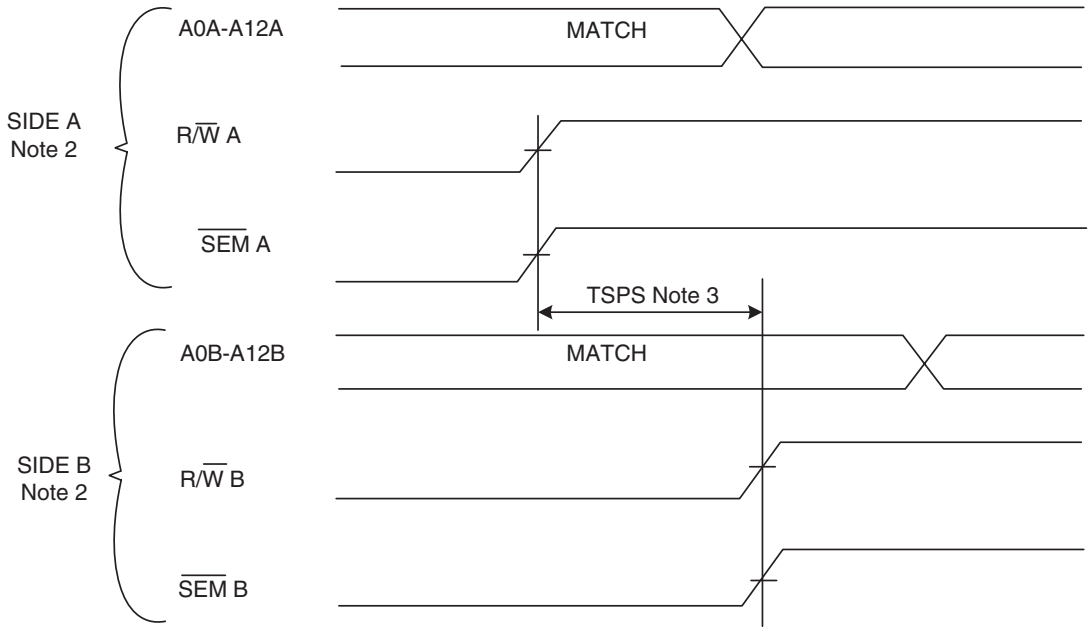
Semaphore Read After Write Timing, Either Side (Note 1)



NOTES:

1. $\overline{CS}$ = V_{IH} for the duration of the above timing (both read and write cycle).

Semaphore Contention (Notes 1, 3, 4)



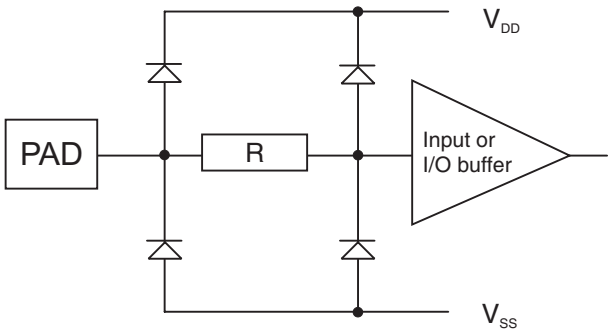
NOTES:

1. D_{OR} = D_{OL} = V_{IL}, $\overline{CSR}$ = $\overline{CSL}$ = V_{IH}, semaphore flag is released from both sides (reads as ones from

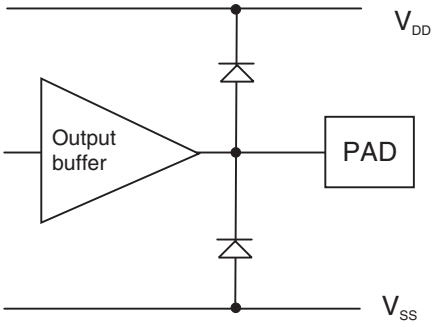
both sides) at cycle start.
2. Either side A = left and side B = right, or side A = right and side B = left.
3. This parameter is measured from the point where R/$\overline{W}$A or $\overline{SEM}$A goes high until R/$\overline{W}$B or $\overline{SEM}$B goes high.
4. If TSPS is violated, the semaphore will fall positively to one side or the other, but there is no guarantee on which side will obtain the flag.

1.11 PROTECTION NETWORKS

EQUIVALENT OF EACH INPUT



EQUIVALENT OF EACH OUTPUT



2. REQUIREMENTS

2.1 GENERAL

The complete requirements for procurement of the components specified herein are as stated in this specification and the ESCC Generic Specification. Permitted deviations from the Generic Specification, applicable to this specification only, are listed below.

Permitted deviations from the Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESCC requirement and do not affect the component's reliability, are listed in the appendices attached to this specification.

2.1.1 Deviations from the Generic Specification

2.1.1.1 Deviations from Screening Tests-Chart F3

(a) High Temperature Reverse Bias Burn-in shall not be performed.

2.2 MARKING

The marking shall be in accordance with the requirements of ESCC Basic Specification No. 21700 and as follows.

The information to be marked on the component shall be:

(a) Terminal identification.
(b) The ESCC qualified components symbol (for ESCC qualified components only).
(c) The ESCC Component Number.
(d) Traceability information.

2.3 ELECTRICAL MEASUREMENTS AT ROOM, HIGH AND LOW TEMPERATURES

Electrical measurements shall be performed at room, high and low temperatures.

2.3.1 Room Temperature Electrical Measurements

The measurements shall be performed at T_{amb}=+22 ±3°C.

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Functional Test 1	-	3014	Verify Truth Table Note 2	-	-	-
Functional Test 2	-	3014	Verify Truth Table Note 2	-	-	-
Functional Test 3	-	3014	Verify Truth Table Note 2	-	-	-
Functional Test 4	-	3014	Verify Truth Table Note 2	-	-	-
Input Clamp Voltage	V_{IC}	3008	I_{IN}(Under Test)=-300µA All Other Pins =0V V_{DD}=V_{SS}=0V	-0.2	-1.2	V
Low Level Input Current	I_{IL}	3009	V_{IN} (Under Test)=0V V_{IN} (Remaining Inputs)=0V or 5.5V V_{DD}=5.5V, V_{SS}=0V	-	-5	µA
High Level Input Current	I_{IH}	3010	V_{IN} (Under Test)=5.5V V_{IN} (Remaining Inputs)=0V or 5.5V V_{DD}=5.5V, V_{SS}=0V	-	5	µA
Output Leakage Current, Third State, Low Level Applied	I_{OZL}	3020	V_{OUT} (Under Test)=0V Other Outputs Floating V_{IN}($\overline{CSL}$, $\overline{CSR}$, $\overline{OEL}$, $\overline{OER}$)=5.5V V_{IN}(R/$\overline{W}$L, R/$\overline{W}$R)=0V V_{DD}=5.5V, V_{SS}=0V	-	-5	µA

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Output Leakage Current, Third State, High Level Applied	I_{OZH}	3021	V_{OUT} (Under Test)=5.5V Other Outputs Floating V_{IN}($\overline{CSL}$, $\overline{CSR}$, $\overline{OEL}$, $\overline{OER}$)=5.5V V_{IN}(R/$\overline{WL}$, R/$\overline{WR}$)=0V V_{DD}=5.5V, V_{SS}=0V	-	5	µA
Low Level Output Voltage	V_{OL}	3007	V_{IL}=0.8V, V_{IH}=2.2V I_{OL}=4mA V_{DD}=4.5V, V_{SS}=0V Note 3	-	400	mV
High Level Output Voltage	V_{OH}	3006	V_{IL}=0.8V, V_{IH}=2.2V I_{OH}=-4mA V_{DD}=4.5V, V_{SS}=0V Note 4	2.4	-	V
Stand-by Supply Current 1 (Both Ports TTL Level Inputs)	I_{DDSB1}	3005	V_{IN}($\overline{CSR}$, $\overline{CSL}$, $\overline{SEMR}$, $\overline{SEML}$)=5.3V V_{IN}(Remaining Inputs)=0.2V f=0Hz V_{DD}=5.5V, V_{SS}=0V Note 5	-	10	mA
Stand-by Supply Current 2 (Both Ports CMOS Level Inputs)	I_{DDSB2}	3005	V_{IN}($\overline{CSL}$, $\overline{CSR}$, $\overline{SEML}$, $\overline{SEMR}$)=5.3V V_{IN}(Remaining Inputs)=0.2V or 5.3V I_{OUT}=0mA f=0Hz V_{DD}=5.5V, V_{SS}=0V Note 5	-	500	µA
Dynamic Operating Current 1 (Both Ports Active)	I_{DDOP1}	3005	V_{IN}($\overline{SEM}$, $\overline{OE}$)=2.2V V_{IN}($\overline{CSR}$, $\overline{CSL}$)=0.8V All Outputs Open f_{write}=33MHz (Variant 01) 22.2MHz (Variant 02) V_{DD}=5.5V, V_{SS}=0V Variant 01 Variant 02	 - -	 320 260	mA

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Dynamic Operating Current 2 (One Port Active - One Port Stand By)	I_{DDOP2}	3005	V_{IN}($\overline{SEM}$, $\overline{OE}$, $\overline{CSR}$ or $\overline{CSL}$)=2.2V V_{IN}($\overline{CS}$ opposite port)=0.8V All Outputs Open f_{write}=33MHz (Variant 01) 22.2MHz (Variant 02) V_{DD}=5.5V, V_{SS}=0V Variant 01 Variant 02	 - -	 200 180	mA
Data Retention Current	I_{DDDR}	3005	V_{DR}=2V V_{IN}($\overline{CSL}$, $\overline{CSR}$, $\overline{SEML}$, $\overline{SEMR}$)=2V V_{IL}=0V, V_{IH}=2V Notes 5 and 6	-	400	µA
Data Retention Test	-	-	Note 6	-	-	-
Input Capacitance	C_{IN}	3012	V_{IN}=V_{DD}=V_{SS}=0V f=1MHz Note 7	-	5	pF
Output Capacitance	C_{OUT}	3012	V_{IN}=V_{DD}=V_{SS}=0V f=1MHz Note 7	-	7	pF
Read Cycle Time (Both Ports)	t_{AVAVR}	3003	V_{DD}=4.5 & 5.5V V_{SS}=0V Note 8 Variant 01 Variant 02	 30 45	 - -	ns
Address Access Time (Both Ports)	t_{AVQV}	3003	V_{DD}=4.5 & 5.5V V_{SS}=0V Note 9 Variant 01 Variant 02	 - -	 30 45	ns
Output Hold from Address Change (One Port)	t_{AVQX}	3003	V_{DD}=4.5 & 5.5V V_{SS}=0V Note 8	3	-	ns
Semaphore Flag Update Pulse (Output Enable or Semaphore Enable)	t_{SOP}	3003	V_{DD}=4.5 & 5.5V V_{SS}=0V Note 8	15	-	ns
Chip Select Access Time (Both Ports)	t_{ELQV}	3003	V_{DD}=4.5 & 5.5V V_{SS}=0V Note 9 Variant 01 Variant 02	 - -	 30 45	ns

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Output Enable Access Time (One Port)	t_{GLQV}	3003	V_{DD}=4.5 & 5.5V V_{SS}=0V Note 7 Variant 01 Variant 02	 - -	 15 25	ns
Chip Select High or Output Enable High to Z	t_{EHQZ}	3003	V_{DD}=4.5 & 5.5V V_{SS}=0V Note 7 Variant 01 Variant 02	 - -	 15 20	ns
Chip Select Low or Output Enable Low to Z	t_{ELQX}	3003	V_{DD}=4.5 & 5.5V V_{SS}=0V Note 7 Variant 01 Variant 02	 3 5	 - -	ns
Chip Select to Power Up Time (One Port)	t_{PU}	3003	V_{DD}=5.5V V_{SS}=0V Note 7	0	-	ns
Chip Select to Power Down Time (One Port)	t_{PD}	3003	V_{DD}=5.5V V_{SS}=0V Note 7	-	50	ns
Byte Enable Access Time (Both Ports)	t_{BLQV}	3003	V_{DD}=4.5 & 5.5V Note 9 V_{SS}=0V Variant 01 Variant 02	 - -	 30 45	ns
Write Cycle Time (Both Ports)	t_{AVAVW}	3003	V_{DD}=4.5 & 5.5V V_{SS}=0V Note 8 Variant 01 Variant 02	 30 45	 - -	ns
Output High Z Time	t_{GHQZ}	3003	V_{DD}=4.5 & 5.5V V_{SS}=0V Note 7 Variant 01 Variant 02	 - -	 15 20	ns
Address Valid to End of Write (Both Ports)	t_{AVWH}	3003	V_{DD}=4.5 & 5.5V V_{SS}=0V Note 8 Variant 01 Variant 02	 25 40	 - -	ns
Address Set-up Time (One Port)	t_{AVWL}	3003	V_{DD}=4.5 & 5.5V V_{SS}=0V Note 8	0	-	ns

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Write Pulse Width (Both Ports)	t_{WLWH}	3003	V_{DD}=4.5 & 5.5V V_{SS}=0V Note 9 Variant 01 Variant 02	 25 35	 - -	ns
Write Recovery Time (Both Ports)	t_{WHAX}	3003	V_{DD}=4.5 & 5.5V V_{SS}=0V Note 8	0	-	ns
Write Enable to Output Inactive	t_{WLQZ}	3003	V_{DD}=4.5 & 5.5V V_{SS}=0V Note 7 Variant 01 Variant 02	 - -	 15 20	ns
Output Active From End of Write (One Port)	t_{WHQX}	3003	V_{DD}=4.5 & 5.5V V_{SS}=0V Note 8	0	-	ns
Data Valid to End of Write (Both Ports)	t_{DVWH}	3003	V_{DD}=4.5 & 5.5V V_{SS}=0V Note 9 Variant 01 Variant 02	 20 25	 - -	ns
Data Hold Time (One Port)	t_{WHDX}	3003	V_{DD}=4.5 & 5.5V V_{SS}=0V Note 9	0	-	ns
Chip Select to End of Write (Both Ports)	t_{ELWH}	3003	V_{DD}=4.5 & 5.5V V_{SS}=0V Note 8 Variant 01 Variant 02	 25 40	 - -	ns
Write Pulse to Data Delay (Both Ports)	t_{WDD}	3003	V_{DD}=4.5 & 5.5V V_{SS}=0V Note 9 Variant 01 Variant 02	 - -	 55 70	ns
Write Data Valid to Read Data Delay (Both Ports)	t_{DDD}	3003	V_{DD}=4.5 & 5.5V V_{SS}=0V Note 9 Variant 01 Variant 02	 - -	 40 55	ns
Arbitration Priority Setup Time (Both Ports)	t_{APS}	3003	V_{DD}=4.5 & 5.5V V_{SS}=0V Note 8	5	-	ns
Busy Access Time from Chip Select Low (Both Ports)	t_{BAC}	3003	V_{DD}=4.5 & 5.5V V_{SS}=0V Note 9 Variant 01 Variant 02	 - -	 25 30	ns

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Busy Disable Time from Chip Select High (Both Ports)	t_{BDC}	3003	V_{DD}=4.5 & 5.5V V_{SS}=0V Note 8 Variant 01 Variant 02	 - -	 20 25	ns
Busy Access Time from Address Match (Both Ports)	t_{BAA}	3003	V_{DD}=4.5 & 5.5V V_{SS}=0V Note 9 Variant 01 Variant 02	 - -	 30 35	ns
Busy Disable Time from Address not Matched (Both Ports)	t_{BDA}	3003	V_{DD}=4.5 & 5.5V V_{SS}=0V Note 9 Variant 01 Variant 02	 - -	 25 30	ns
Busy Disable Time to Valid Data Out	t_{BDD}	3003	-	Note 10		ns
Interrupt Set Time (Both Ports)	t_{INS}	3003	V_{DD}=4.5 & 5.5V V_{SS}=0V Note 9 Variant 01 Variant 02	 - -	 25 35	ns
Interrupt Reset Time (Both Ports)	t_{INR}	3003	V_{DD}=4.5 & 5.5V V_{SS}=0V Note 9 Variant 01 Variant 02	 - -	 25 35	ns
Busy Input to Write (Both Ports)	t_{WB}	3003	V_{DD}=4.5 & 5.5V V_{SS}=0V Note 8	0	-	ns
Write Hold After Busy (Both Ports)	t_{WH}	3003	V_{DD}=4.5 & 5.5V V_{SS}=0V Note 8 Variant 01 Variant 02	 20 25	 - -	ns
Semaphore Flag Contention Window (Both Ports)	t_{SPS}	3003	V_{DD}=4.5 & 5.5V V_{SS}=0V Note 8	10	-	ns
Semaphore Address Access Time	t_{SLQV}	3003	V_{DD}=4.5 & 5.5V V_{SS}=0V Note 8 Variant 01 Variant 02	 30 45	 - -	ns

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Semaphore Flag Write to Read Time	t_{SWRD}	3003	V_{DD}=4.5 & 5.5V V_{SS}=0V Note 8	10	-	ns

NOTES:

1. Unless otherwise specified all inputs shall be tested for each characteristic, inputs not under test shall be $V_{IN} = V_{SS}$ or V_{DD} and outputs not under test shall be open.
2. Functional go-no-go test with the following test sequences:

FUNCTIONAL TEST 1

Pattern	Timing (ns)	Access Note (c)	V_{DD} (V)	V_{SS} (V)	V_{IL} (V)	V_{IH} (V)	I_{OL} (mA)	I_{OH} (mA)	$V_{out\ comp}$ (V) Note (b)
MARCH	110	L	4.5 & 5.5	0	0	3	+4	-4	1.5
CHECKERBOARD	110	R/L	4.5 & 5.5	0	0	3	+4	-4	1.5
CEDES	110	L	4.5 & 5.5	0	0	3	+4	-4	1.5
DUAL PORT	110	R/L	4.5 & 5.5	0	0	3	+4	-4	1.5

FUNCTIONAL TEST 2

Pattern	Timing (ns)	Access Note (c)	V_{DD} (V)	V_{SS} (V)	V_{IL} (V)	V_{IH} (V)	I_{OL} (mA)	I_{OH} (mA)	$V_{out\ comp}$ (V) Note (b)
MARCH	110	L	4.5	0	-0.5	4.5	+4	-4	1.5
MARCH	110	L	5.5	0	-0.5	6	+4	+4	1.5
MARCH	110	L	6.5	0	0	6.5	+4	+4	1.5
CHECKERBOARD	110	R	4.5	0	-0.5	4.5	+4	+4	1.5
CHECKERBOARD	110	R	5.5	0	-0.5	6	+4	-4	1.5
CHECKERBOARD	110	R	6.5	0	0	6.5	+4	-4	1.5
V_{IL}	110	R/L	5.5	0	0	2.2	+4	-4	1.5
V_{IH}	110	R/L	4.5	0	0.8	3	+4	-4	1.5

FUNCTIONAL TEST 3

Pattern Note (a)	Timing (ns)	Access Note (c)	V_{DD} (V)	V_{SS} (V)	V_{IL} (V)	V_{IH} (V)	I_{OL} (mA)	I_{OH} (mA)	$V_{out\ comp}$ (V) Note (b)
BUSY	110	R/L	4.5 & 5.5	0	0	3	+4	+4	1.5
INT	110	R/L	4.5 & 5.5	0	0	3	+4	+4	1.5
SEM	110	R/L	4.5 & 5.5	0	0	3	+4	+4	1.5

FUNCTIONAL TEST 4

Pattern Note (a)	Timing (ns)		Access Note (c)	V_{DD} (V)	V_{SS} (V)	V_{IL} (V)	V_{IH} (V)	$V_{out\ comp}$ (V) Note (b)
	Variant 01	Variant 02	R/L					
MARCH/ CHECKERBOARD/ BUSY/ INT/ SEM/ DUAL PORT	30	45		4.5 & 5.5	0	0	3	1.5

(a)

The Busy Left shall be performed with:

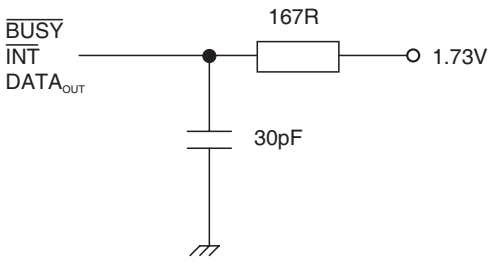
- Busy read right with left contention
- Busy left generation arbitration
- Busy arbitration port left

The Busy Right pattern shall be performed with:

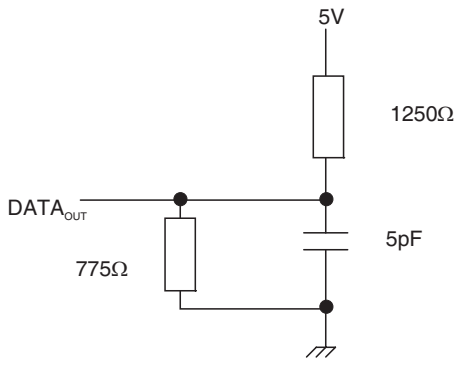
- Busy read left with right contention
- Busy right generation arbitration
- Busy arbitration port right

(b) The maximum input rise and fall time shall be 5ns.
(c) When both ports R/L are specified, only the worst case shall be recorded.
(d) Input Timing Reference Level = 1.5V
(e) Output Loading including jig & scope = 30pF except for t_{ELQX}, t_{EHQZ}, t_{WHQX}, and t_{WLQZ} where this = 5pF, see circuits below:

GENERAL OUTPUT LOAD



OUTPUT LOAD FOR t_{ELQX}, t_{EHQZ}, t_{WHQX} AND t_{WLQZ}



3. Select address inputs to produce a low level at pin under test.
4. Select address inputs to produce a high level at the pin under test.
5. Measurements are performed with the memory loaded with a background of zeros, then with a

background of ones, for all inputs High, then Low. Only the worst case is recorded.

6. Data retention procedure:
   (a) Write memory at V_{DD} = 4.5V with CHECKERBOARD pattern with V_{IL} = 0V and V_{IH} = 3V, Timing = 110ns.
   (b) Power down to V_{DD} = 2V for 250ms.
   (c) Restore V_{DD} to 4.5V, wait t_R (operation recovery time, see (e) below) and compare with the original pattern.
   (d) Repeat the procedure with $\overline{\text{CHECKERBOARD}}$ pattern.
   (e) t_R = 30ns for Variant 01 and 45ns for Variant 02.

7. Guaranteed but not tested.
8. Measurements shall be performed, on a go-no-go basis, during Functional Test 4.
9. Measurements shall be performed during Functional Test 4.
10. t_{BBD} is a calculated parameter and shall be:
    either 0ns < $t_{BDD} \leq (t_{DDD} - t_{DVWH})$ or 0ns < $t_{BDD} \leq (t_{WDD} - t_{WLWH})$

2.3.2 High and Low Temperatures Electrical Measurements

The measurements shall be performed at T_{amb}=+125 (+0 -5)°C and T_{amb}=- 55 (+5 -0)°C.

The characteristics, test methods, conditions and limits shall be the same as specified for Room Temperature Electrical Measurements.

2.4 PARAMETER DRIFT VALUES

Unless otherwise specified, the measurements shall be performed at T_{amb}=+22 ±3°C.

The test methods and test conditions shall be as per the corresponding test defined in Room Temperature Electrical Measurements.

The drift values (Δ) shall not be exceeded for each characteristic specified. The corresponding absolute limit values for each characteristic shall not be exceeded.

Characteristics Note 1	Symbols	Limits			Units
		Drift Value Δ	Absolute		
			Min	Max	
Low Level Input Current	I_{IL}	±0.1	-	-5	µA
High Level Input Current	I_{IH}	±0.1	-	5	µA
Output Leakage Current, Third State, Low Level Applied	I_{OZL}	±0.1	-	-5	µA
Output Leakage Current, Third State, High Level Applied	I_{OZH}	±0.1	-	5	µA
Low Level Output Voltage	V_{OL}	±100	-	400	mV
High Level Output Voltage	V_{OH}	±0.1	2.4	-	V
Stand-by Supply Current 1	I_{DDSB1}	±1	-	10	mA
Stand-by Supply Current 2	I_{DDSB2}	±50	-	500	µA
Data Retention Current	I_{DDDR}	±40	-	400	µA

NOTES:

1. Unless otherwise specified all inputs and outputs shall be tested for each characteristic.

2.5 INTERMEDIATE AND END-POINT ELECTRICAL MEASUREMENTS

Unless otherwise specified, the measurements shall be performed at T_{amb}=+22 ±3°C.

The test methods, test conditions and limits shall be as specified for Room Temperature Electrical Measurements.

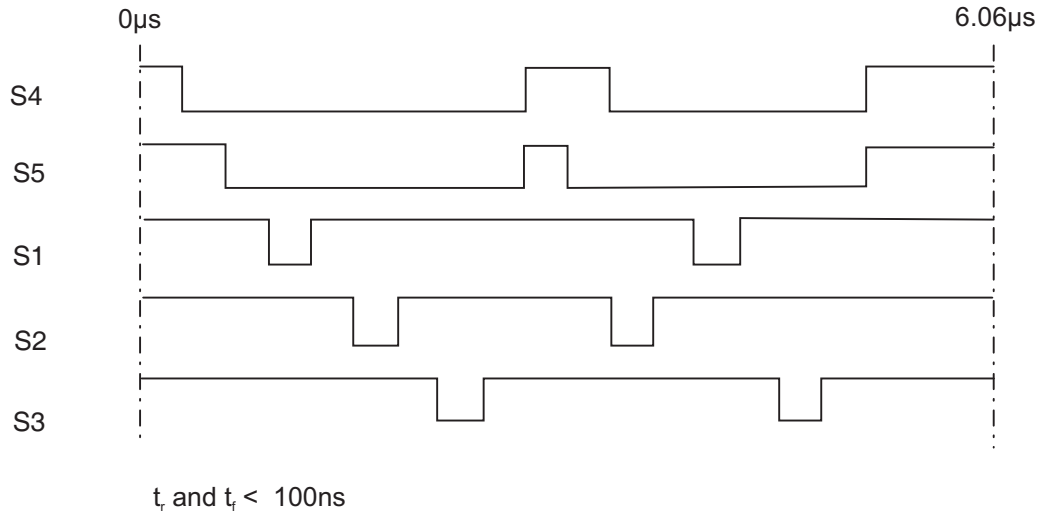
2.6 POWER BURN-IN CONDITIONS

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	T_{amb}	125 (+0 -5)	°C
Outputs $\overline{BUSY}$L, $\overline{BUSY}$R, $\overline{INT}$L, $\overline{INT}$R	V_{OUT}	V_{DD} and V_{SS}	V
Inputs A0L and A0R	V_{IN}	V_{GEN}(S6)	V
Inputs A1L, R to A12L, R	V_{IN}	V_{GEN}(S7) to V_{GEN}(S18) (Note 1)	V
Input R/$\overline{W}$L	V_{IN}	V_{GEN}(S1) (Note 2)	V
Input R/$\overline{W}$R	V_{IN}	V_{GEN}(S2) (Note 2)	V
Inputs $\overline{OE}$L, $\overline{OE}$R	V_{IN}	V_{GEN}(S3) (Note 2)	V
Inputs $\overline{CS}$L, $\overline{LB}$L, $\overline{UB}$L	V_{IN}	V_{GEN}(S4) (Note 2)	V
Inputs $\overline{CS}$R, $\overline{LB}$R, $\overline{UB}$R	V_{IN}	V_{GEN}(S5) (Note 2)	V
Inputs $\overline{SEM}$L, $\overline{SEM}$R, M/$\overline{S}$	V_{IN}	V_{DD}	V
Inputs/Outputs I/O0L, I/O2L, I/O4L, I/O6L, I/O8L, I/O10L, I/O12L, I/O14L, I/O0R, I/O2R, I/O4R, I/O6R, I/O8R, I/O10R, I/O12R, I/O14R	V_{IN}	V_{GEN}(S19) (Note 1)	V
Inputs/Outputs I/O1L, I/O3L, I/O5L, I/O7L, I/O9L, I/O11L, I/O13L, I/O15L, I/O1R, I/O3R, I/O5R, I/O7R, I/O9R, I/O11R, I/O13R, I/O15R	V_{IN}	V_{GEN}(S20) (Note 1)	V
Pulse Voltage	V_{GEN}	0V to V_{DD}	V
Pulse Frequency Square Wave	$f_{GEN(S6)}$	82.5 50 ± 15% duty cycle	kHz

Characteristics	Symbols	Test Conditions	Units
Positive Supply Voltage	V_{DD}	5 (+0.5 -0)	V
Negative Supply Voltage	V_{SS}	0	V

NOTES:

1. $f_{GEN(Sn)} = f_{GEN(Sn-1)}/2$, for n=7 to 20
2. Signals S1 to S5 are shown below:



t_r and t_f < 100ns

3. Input Protection Resistor = Output Load = 1kΩ.

2.7 OPERATING LIFE CONDITIONS

The conditions shall be as specified for Power Burn-in.

2.8 TOTAL DOSE RADIATION TESTING

2.8.1 Bias Conditions and Total Dose Level for Total Dose Radiation Testing

Continuous bias shall be applied during radiation testing as specified below.

The total dose level applied shall be as specified in the component type variant information herein or in the Purchase Order.

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	T_{amb}	+22 ±3	^{o}C
Outputs $\overline{INTL}$, $\overline{INTR}$, $\overline{BUSYL}$, $\overline{BUSYR}$	V_{OUT}	Open	V
Inputs A12L, A12R	V_{IN}	Open	V
Inputs A0L to A11L, A0R to A11R, $\overline{CSL}$, $\overline{CSR}$, $\overline{SEML}$, $\overline{SEMR}$, R/$\overline{WL}$, R/$\overline{WR}$, $\overline{UBL}$, $\overline{UBR}$, $\overline{LBL}$, $\overline{LBR}$, M/$\overline{S}$, $\overline{OEL}$, $\overline{OER}$	V_{IN}	V_{DD}	V

Characteristics	Symbols	Test Conditions	Units
Input/Outputs I/OnL, I/OnR	V_{IN}	Open	V
Positive Supply Voltage	V_{DD}	5(+0.5 -0)	V
Negative Supply Voltage	V_{SS}	0	V

NOTES:

1. Input protection resistors = 1 kΩ.

2.8.2 Electrical Measurements for Total Dose Radiation Testing

Prior to, during and on completion of radiation testing the devices shall successfully meet the Room Temperature Electrical Measurements specified herein.

Unless otherwise specified the measurements shall be performed at T_{amb} = +22±3°C.

The characteristics, test methods, conditions and limits shall be the same as specified for Room Temperature Electrical Measurements.