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INTEGRATED CIRCUITS, MONOLITHIC, CMOS SILICON ON SAPPHIRE, 3.5GHZ INTEGER-N PLL FREQUENCY SYNTHESISER

BASED ON TYPE PE33382

ESCC Detail Specification No. 9202/079

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DOCUMENTATION CHANGE NOTICE

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DCR No.	CHANGE DESCRIPTION

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1. GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics and test and inspection data for the component type variants and/or the range of components specified below. It supplements the requirements of, and shall be read in conjunction with, the ESCC Generic Specification listed under Applicable Documents.

1.2 APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:

(a) ESCC Generic Specification No. 9000.
(b) MIL-STD-883, Test Methods and Procedures for Microelectronics.

1.3 TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESCC Basic Specification No. 21300 shall apply.

1.4 THE ESCC COMPONENT NUMBER AND COMPONENT TYPE VARIANTS

1.4.1 The ESCC Component Number

The ESCC Component Number shall be constituted as follows:

Example: 920207901R

- Detail Specification Reference: 9202079
- Component Type Variant Number: 01
- Total Dose Radiation Level Letter: R (as required)

1.4.2 Component Type Variants

The component type variants applicable to this specification are as follows:

Variant Number	Based on Type	Case	Lead/Terminal Material and Finish	Weight max g	Total Dose Radiation Level Letter
01	PE33382	CQFPJ-44	G2	10	R [100kRAD(Si)]

The lead/terminal material and finish shall be in accordance with the requirements of ESCC Basic Specification No. 23500.

Total dose radiation level letters are defined in ESCC Basic Specification No. 22900. If an alternative radiation test level is specified in the Purchase Order the letter shall be changed accordingly.

1.5 MAXIMUM RATINGS

The maximum ratings shall not be exceeded at any time during use or storage. Prolonged use of the

device at the maximum ratings may reduce the device's overall reliability.

Maximum ratings shall only be exceeded during testing to the extent specified in this specification and when stipulated in Test Methods and Procedures of the ESCC Generic Specification.

Characteristics	Symbols	Maximum Ratings	Units	Remarks
Supply Voltage Range	V_{DD}	-0.3 to 4	V	Note 1
Input Voltage Range	V_{IN}	-0.3 to V_{DD}+0.3	V	Note 2
DC Input Current Range	I_{IN}	-10 to +10	mA	
DC Output Current Range	I_{OUT}	-90 to +110	mA	Note 3
Device Power Dissipation (Continuous)	P_D	500	mW	
Operating Temperature Range	T_{op}	-40 to +85	^oC	T_{amb}
Storage Temperature Range	T_{stg}	-65 to +150	^oC	
Junction Temperature	T_j	+150	^oC	
Thermal Resistance, Junction to Case	$R_{th(j-c)}$	15	$^oC/W$	
Soldering Temperature	T_{sol}	+260	^oC	Note 4

NOTES:
1. All voltages are with respect to V_{SS}. Device is functional for $2.85 \leq V_{DD} \leq 3.45V$.
2. V_{DD} + 0.3V shall not exceed 4V.
3. The maximum output current of any single output for a maximum duration of 1 second.
4. Duration 10 seconds maximum at a distance of not less than 1.6mm from the device body and the same terminal shall not be re-soldered until 3 minutes have elapsed.

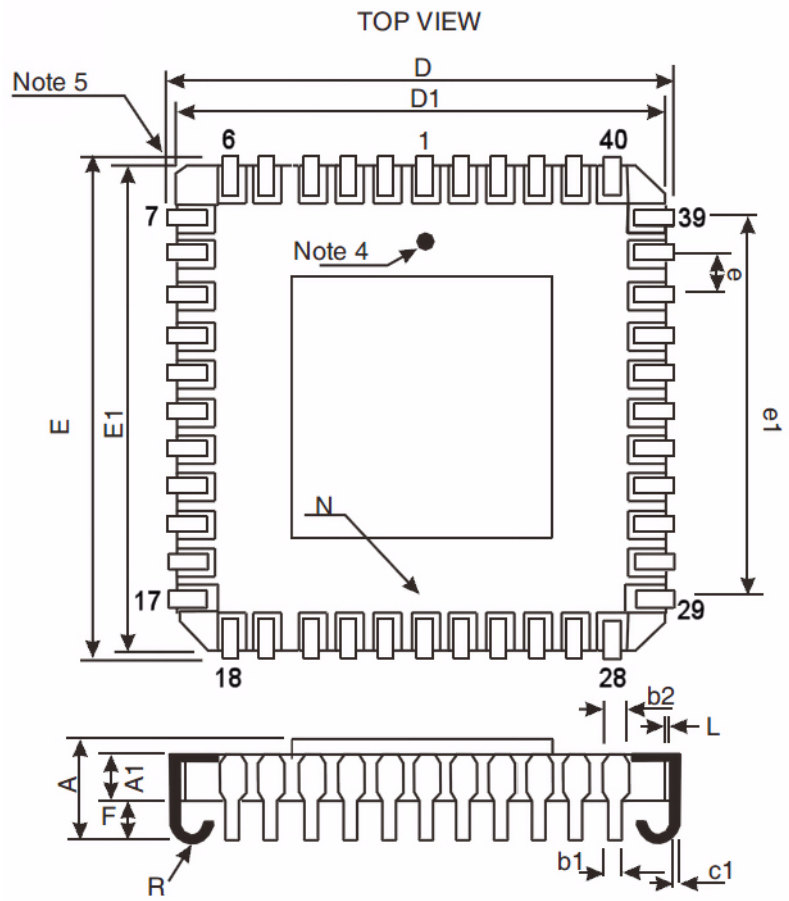
1.6 HANDLING PRECAUTIONS

These devices are susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacture, testing, packaging, shipment and any handling.

These components are categorised as Class 1 per ESCC Basic Specification No. 23800 with a minimum Critical Path Failure Voltage of 1000 Volts.

1.7 PHYSICAL DIMENSIONS AND TERMINAL IDENTIFICATION

1.7.1 Ceramic Quad Flat Package J-BEND (CQFPJ-44) - 44 Terminals



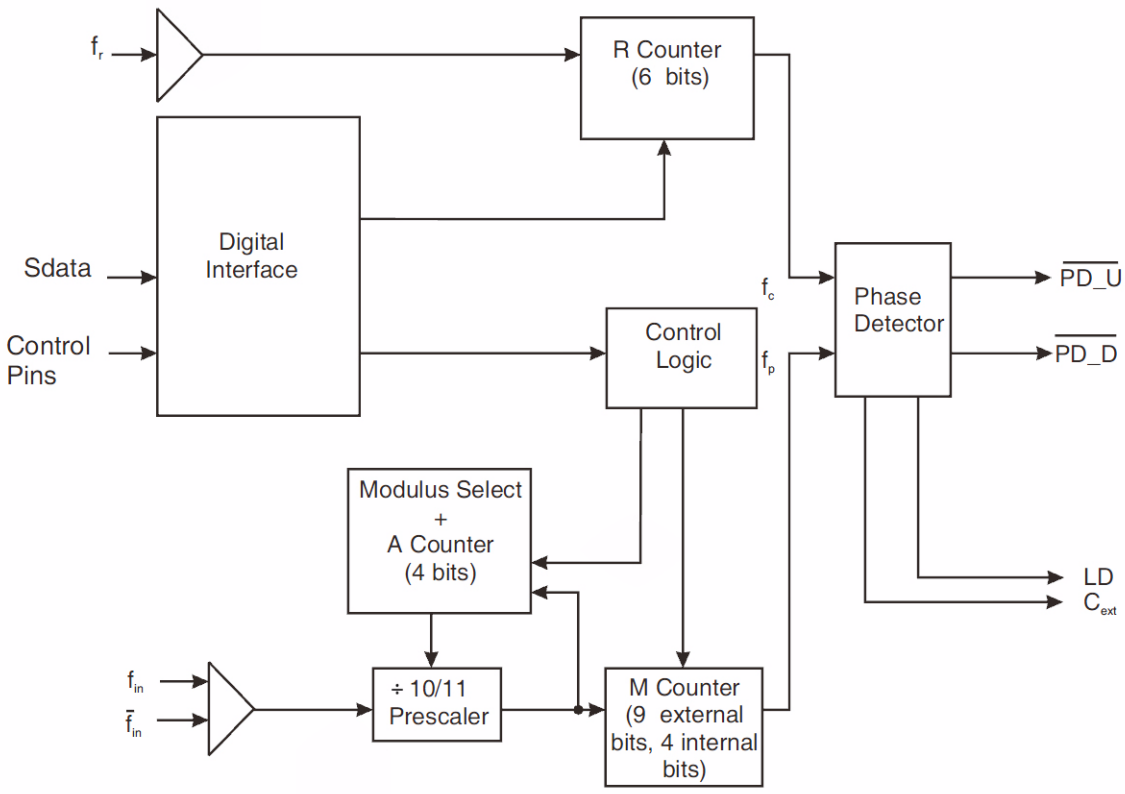
Symbols	Dimensions mm		Notes
	Min	Max	
A	2.41	3.18	1
A1	1.49	1.81	
b1	0.432 TYPICAL		1
b2	0.762 TYPICAL		1
c1	0.2	0.28	1
D/E	17.27	17.78	
D1/E1	16.3	16.72	
e	1.27 BSC		1, 2
e1	12.49	12.91	3
F	0.66	1.17	1
L	0.508 TYPICAL		1
N	11 TERMINALS PER SIDE		3

Symbols	Dimensions mm		Notes
	Min	Max	
R	0.5	1.02	1, 6

NOTES:

1. Applies to all 44 terminals (11 per side).
2. 40 places. The true position pin spacing is 1.27mm between centrelines. Each pin centreline shall be located within ±0.13mm of its true longitudinal position relative to the package centrelines.
3. 4 places.
4. A terminal identification mark shall be located in the region of Pin 1 as shown. Terminal numbers shall increase counter clockwise when viewed as shown starting from the centre terminal (Pin 1).
5. Index corner: Terminal identification is specified by reference to the index corner as shown.
6. Radius.

1.8 FUNCTIONAL DIAGRAM



1.9 PIN ASSIGNMENT AND DESCRIPTION

The table below describes each pin's assignment, type and standard, plus a brief description of its functionality.

Pin No.	Pin Name	Pin Type	Pin Standard	Valid Mode	Description
Top side					
1	V_{DD}	Power	-	-	Power Supply (Note 1).
2	R_0	Input	CMOS	Direct	R Counter, bit 0 (LSB).
3	R_1	Input	CMOS	Direct	R Counter, bit 1.
4	R_2	Input	CMOS	Direct	R Counter, bit 2.
5	R_3	Input	CMOS	Direct	R Counter, bit 3.
6	V_{SS}	Ground	-	-	V_{SS}
Left-hand side					
7	R_4	Input	CMOS	Direct	R Counter, bit 4.
8	R_5	Input	CMOS	Direct	R Counter, bit 5 (MSB).
9	M_0	Input	CMOS	Direct	M Counter, bit 0 (LSB).
10	M_1	Input	CMOS	Direct	M Counter, bit 1.
11	V_{DD}	Power	-	-	Power Supply (Note 1).
12	V_{DD}	Power	-	-	Power Supply (Note 1).
13	M_2	Input	CMOS	Direct	M Counter, bit 2.
14	M_3	Input	CMOS	Direct	M Counter, bit 3.
15	S_WR	Input	CMOS	Serial	Frequency register load enable input.
	M_4	Input	CMOS	Direct	M Counter, bit 4.
16	SDATA	Input	CMOS	Serial	Binary serial data input, input data entered LSB first.
	M_5	Input	CMOS	Direct	M Counter, bit 5.
17	V_{SS}	Ground	-	-	V_{SS}
Bottom side					
18	SCLK	Input	CMOS	Serial	Serial Clock Input.
	M_6	Input	CMOS	Direct	M Counter, bit 6.
19	M_7	Input	CMOS	Direct	M Counter, bit 7.
20	M_8	Input	CMOS	Direct	M Counter, bit 8 (MSB).
21	A_0	Input	CMOS	Direct	A Counter, bit 0 (LSB).
22	DMODE	Input	CMOS	All	Direct interface mode selection.
23	V_{DD}	Power	-	-	Power Supply (Note 1).
24	E_WR	Input	CMOS	Serial	Enhancement register write enable.
	A_1	Input	CMOS	Direct	A Counter, bit 1.
25	A_2	Input	CMOS	Direct	A Counter, bit 2.
26	A_3	Input	CMOS	Direct	A Counter, bit 3 (MSB).
27	FIN	Input	RF	All	Prescaler input.

Pin No.	Pin Name	Pin Type	Pin Standard	Valid Mode	Description
28	$\overline{FIN}$	Input	RF	All	Prescaler complementary input.
Right-hand side					
29	V_{SS}	Ground	-	-	V_{SS}
30	N/C	-	-	-	Not connected.
31	V_{DD}	Power	-	-	Power Supply (Note 1).
32	DOUT	Output	CMOS	Serial	Data out.
33	V_{DD}	Power	-	-	Power Supply (Note 1).
34	N/C	-	-	-	Not connected.
35	V_{SS}	Ground	-	-	V_{SS}
36	$\overline{PD\_D}$	Output	CMOS	All	Pulses down when f_p leads f_c.
37	$\overline{PD\_U}$	Output	CMOS	All	Pulses down when f_c leads f_p.
38	V_{DD}	Power	-	-	Power Supply (Note 1).
39	CEXT	Output	CMOS	All	External capacitor.
Top side					
40	V_{SS}	Ground	-	-	V_{SS}
41	V_{SS}	Ground	-	-	V_{SS}
42	FR	Input	CMOS	All	Reference frequency.
43	$\overline{ENH}$	Input	CMOS	All	Enhancement mode.
44	LD	Output	Open drain	All	Lock detect.

NOTES:

1. All V_{DD} pins are connected by diodes and must be supplied with the same positive voltage level.
2. All digital input pins (i.e. CMOS inputs of Group 1 below) have a 70kΩ pull-down resistor to ground.

The table below describes the pin groups to be tested.

Group No.	Type	Total No. of Pins	Pin Numbers
1	CMOS Input with Pull-down	21	2 to 5, 7 to 10, 13 to 16, 18 to 22, 24 to 26 and 43
2	CMOS Input	1	42 (FR)
3	RF Input	2	27 (FIN) and 28 ($\overline{FIN}$)
4	High Current CMOS Output	2	36 ($\overline{PD\_D}$) and 37 ($\overline{PD\_U}$)
5	Low Current CMOS Output	1	32 (DOUT)
6	High Resistance CMOS Output	1	39 (CEXT)
7	Open Drain Output	1	44 (LD)
8	Power	7	1, 11, 12, 23, 31, 33 and 38
9	Ground	5	6, 17, 29, 35, 40 and 41

1.10 FUNCTIONAL DESCRIPTION

1.10.1 Overview

The PE33382 consists of a prescaler, several counters, a phase detector and control logic. The dual modulus prescaler divides the VCO frequency by either 10 or 11, depending on the value of the modulus select. Counters “R” and “M” divide the reference and prescaler outputs, respectively, by the integer values stored in a 20-bit register. An additional counter (“A”) is used in the modulus select logic.

The phase-frequency detector generates up and down frequency control signals. The control logic includes a selectable chip interface. Data can be written via serial bus or hardwired directly to the pins. There are also various operational and test modes and a lock detect output.

1.10.2 Main Counter Chain

1.10.2.1 Normal Operating Mode

Setting the PB control bit “low” enables the ÷10/11 prescaler. The main counter chain then divides the RF input frequency (f_{in}) by an integer derived from the values in the “M” and “A” Counters.

In this mode, the output from the main counter chain (f_p) is related to the VCO frequency (f_{in}) by the following equation:

$$f_p = f_{in}/[10 \times (M + 1) + A] \qquad (1)$$

Where $A \leq M + 1$, $1 \leq M \leq 511$

When the loop is locked, f_{in} is related to the reference frequency (f_r) by the following equation:

$$f_{in} = [10 \times (M + 1) + A] \times (f_r/(R + 1)) \qquad (2)$$

Where $A \leq M + 1$, $1 \leq M \leq 511$

A consequence of the upper limit on A is that f_{in} must be greater than or equal to $90 \times (f_r / (R + 1))$ to obtain contiguous channels. The A Counter can accept values as high as 15 but in typical operations it will cycle from 0 to 9 between increments in M.

Programming the M Counter with the minimum allowed value of “1” will result in a minimum M Counter divide ratio of “2”.

1.10.2.2 Prescaler Bypass Mode

Setting the enhancement register bit PB “high” allows f_{in} to bypass the ÷10/11 prescaler. In this mode, the prescaler and A Counter are powered down, and the input VCO frequency is divided by the M Counter directly. This mode is only available when using the serial port to set the frequency control bits. The following equation relates f_{in} to the reference frequency (f_r):

$$f_{in} = (M + 1) \times (f_r/(R + 1)) \qquad (3)$$

Where $1 \leq M \leq 511$

1.10.3 Reference Counter Chain

The reference counter chain divides the reference frequency (f_r) down to the phase detector comparison frequency (f_c).

The output frequency of the 6-bit R Counter is related to the reference frequency by the following equation:

$$f_c = f_r/(R + 1) \qquad (4)$$

Where $0 \leq R \leq 63$

Note that programming R with "0" will pass the reference frequency (f_r) directly to the phase detector.

1.10.4 Register Programming

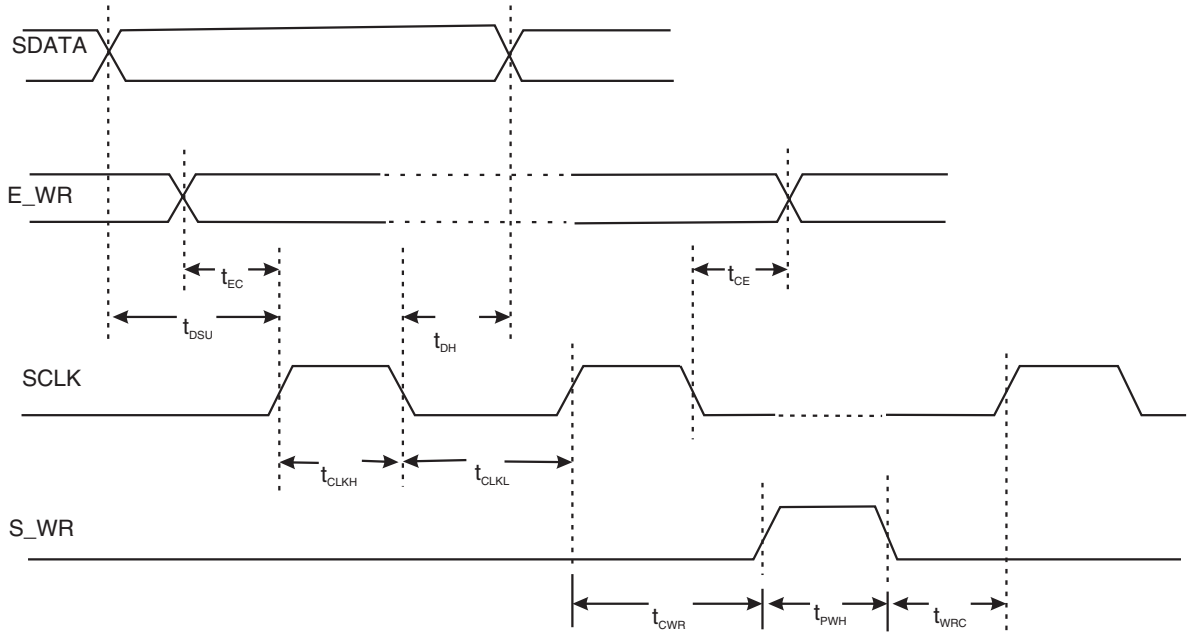
1.10.4.1 Serial Interface Mode

The Serial Interface mode is selected by setting the DMODE input "low".

While the E_WR input is "low", serial input data (SDATA input), B_0 to B_{19}, are clocked serially into the primary register on the rising edge of SCLK, LSB (B_0) first. The contents from this buffer register are transferred into the frequency control register on the rising edge of S_WR according to the timing chart shown below. This data controls the counters as shown in the table below.

While the E_WR input is "high", serial input data (SDATA input), B_0 to B_7, are clocked serially into a buffer register on the rising edge of SCLK, LSB (B_0) first. The contents from this buffer register are transferred into the enhancement register on the falling edge of E_WR according to the timing chart shown below. After the falling edge of E_WR, the data provides control bits as shown in the table below. These bits are active when the $\overline{\text{ENH}}$ input is "low".

Serial Interface Timing Chart



1.10.4.2 Direct Interface Mode

Direct Interface mode is selected by setting the DMODE input “high”.

In this mode, the counter values are set directly at external pins as shown in the table below. All frequency control register bits are addressable except PB (it is not possible to by-pass the ÷10/11 dual modulus prescaler in Direct Mode).

Interface Mode	$\overline{ENH}$	DMODE	R_5	R_4	M_8	M_7	X	M_6	M_5	M_4	M_3	M_2	M_1	M_0	R_3	R_2	R_1	R_0	A_3	A_2	A_1	A_0
Direct	1	1	R_5	R_4	M_8	0	0	M_6	M_5	M_4	M_3	M_2	M_1	M_0	R_3	R_2	R_1	R_0	A_3	A_2	A_1	A_0
Serial (Note 1)	1	0	B_0	B_1	B_2	B_3	B_4	B_5	B_6	B_7	B_8	B_9	B_{10}	B_{11}	B_{12}	B_{13}	B_{14}	B_{15}	B_{16}	B_{17}	B_{18}	B_{19}

↑LSB (first in) MSB (last in)↑

Interface Mode	$\overline{ENH}$	DMODE	Reserved	Reserved	FP Output	Power Down	Counter Load	MSEL Output	FC Output	PB
Serial (Note 1)	0	0	B_0	B_1	B_2	B_3	B_4	B_5	B_6	B_7

↑LSB (first in) MSB(last in) ↑

NOTES:

1. Serial data clocked serially on SCLK rising edge while E_WR “low” and transferred to frequency register on S_WR rising edge.

1.10.4.3 Enhancement Register

The functions of the enhancement register bits are shown below with all bits active “high”. Operation is undefined if more than one output is sent to DOUT.

Bit Number	Bit Function	Description
0	Reserved	Reserve bit - program to 0.
1	Reserved	Reserve bit - program to 0.
2	FP Output	Drives the M Counter output onto the DOUT output.
3	Power Down	Power down of all functions except programming interface.
4	Counter Load	Immediate and continuous load of counter programming.
5	MSEL Output	Drives the internal dual modulus prescaler modulus select (MSEL) output onto the DOUT output.
6	FC Output	Drives the R counter output onto the DOUT output.
7	PB	Allows f_{in} to bypass the ÷10/11 prescaler.

1.10.5 Phase Detector

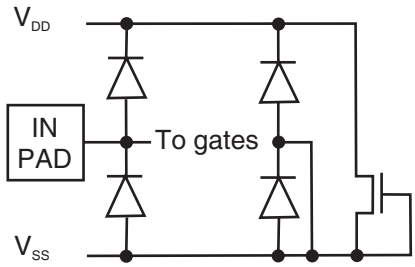
The phase detector is triggered by rising edges from the main Counter (f_p) and the reference Counter (f_c). It has two outputs, namely $\overline{PD\_U}$ and $\overline{PD\_D}$. If the divided VCO leads the divided reference in phase or frequency (f_p leads f_c), $\overline{PD\_D}$ pulses “low”. If the divided reference leads the divided VCO in phase or frequency (f_c leads f_p), $\overline{PD\_U}$ pulses “low”. The width of either pulse is directly proportional to phase offset between the two input signals, f_p and f_c. The phase detector gain is 430mV per radian.

$\overline{PD\_U}$ and $\overline{PD\_D}$ are designed to drive an active loop filter which controls the VCO tune voltage. $\overline{PD\_U}$ pulses cause an increase in VCO frequency and $\overline{PD\_D}$ pulses cause a decrease in VCO frequency, for a positive Kv VCO.

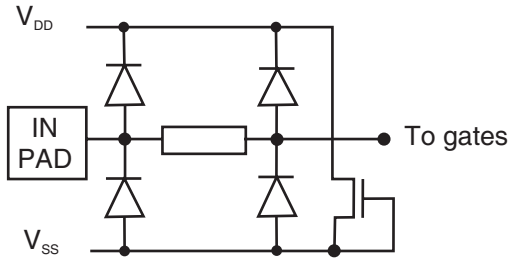
A “lock detect” output, LD, is also provided via the pin CEXT. CEXT is the logical “NAND” of $\overline{PD\_U}$ and $\overline{PD\_D}$ waveforms, which is driven through a serial 2kΩ resistor. Connecting CEXT to an external shunt capacitor provides integration of this signal.

1.11 INPUT AND OUTPUT PROTECTION NETWORKS

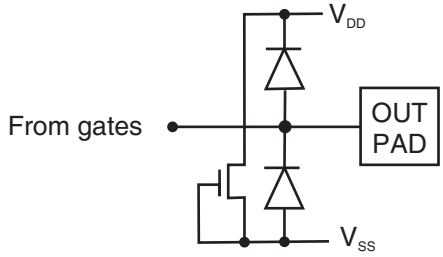
RF Inputs



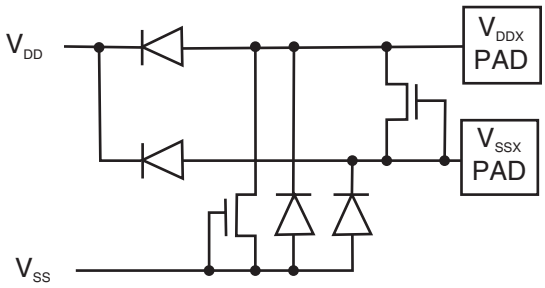
Other Inputs



Outputs



Supplies



2. REQUIREMENTS

2.1 GENERAL

The complete requirements for procurement of the components specified herein are as stated in this specification and the ESCC Generic Specification. Permitted deviations from the Generic Specification, applicable to this specification only, are listed below.

Permitted deviations from the Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESCC requirement and do not affect the component's reliability, are listed in the appendices attached to this specification.

2.1.1 Deviations from the Generic Specification

2.1.1.1 Deviations from Screening Tests - Chart F3

High Temperature Reverse Bias Burn-in and the subsequent Final Measurements for HTRB Burn-in shall be omitted.

2.2 MARKING

The marking shall be in accordance with the requirements of ESCC Basic Specification No. 21700 and as follows.

The information to be marked on the component shall be:

(a) Terminal identification.
(b) The ESCC qualified components symbol (for ESCC qualified components only).
(c) The ESCC Component Number.
(d) Traceability information.

2.3 ELECTRICAL MEASUREMENTS AT ROOM, HIGH AND LOW TEMPERATURES

Electrical measurements shall be performed at room, high and low temperatures.

2.3.1 Room Temperature Electrical Measurements

The measurements shall be performed at T_{amb}=+22 ±3°C.

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions	Limits		Units
				Min	Max	
Input Clamp Voltage to V_{SS}	V_{ICL}	3022	Inputs: Pin Groups 1 to 3 Outputs: Pin Groups 4 to 7 V_{DD}=V_{SS}=0V I_{IN}=200µA Note 1	-1.5	-	V
Input Clamp Voltage to V_{DD}	V_{ICH}	3022	Inputs: Pin Groups 1 to 3 Outputs: Pin Groups 4 to 7 V_{DD}=V_{SS}=0V I_{IN}=-200µA Note 1	-	1.5	V
Shorts / Continuity Check	V_{SH}	-	Inputs: Pin Groups 1 to 3 Outputs: Pin Groups 4 to 7 V_{DD}=V_{SS}=0V I_{IN}=-200µA Note 1	-	200	mV
Standby Supply Current with Prescaler	I_{DDQ1}	3005	V_{DD}=3.45V, V_{SS}=0V Use pattern *main_pattern*, stop at label *pdwn_sp* Note 3	-	750	µA

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions	Limits		Units
				Min	Max	
Dynamic Supply Current with Prescaler	$I_{DDOPENA}$	3005	V_{DD}=3.45V, V_{SS}=0V V_{IH}=3.45V, V_{IL}=0V (Pin Groups 1 to 3) V_{OH}=1.8V, V_{OL}=1.3V I_{OL}=I_{OH}=0A (Pin Groups 4 to 6) I_{OL}=-1mA (Pin Group 7) C_{LOAD}<62pF Use pattern *main_pattern*@10MHz Loop from first to last vector Note 2	30	52	mA
Dynamic Supply Current without Prescaler	$I_{DDOPDIS}$	3005	V_{DD}=3.45V, V_{SS}=0V V_{IH}=3.45V, V_{IL}=0V (Pin Groups 1 to 3) V_{OH}=1.8V, V_{OL}=1.3V I_{OL}=I_{OH}=0A (Pin Groups 4 to 6) I_{OL}=-1mA (Pin Group 7) C_{LOAD}<62pF Use pattern *main_pattern*@10MHz Loop from first to last vector Note 2	8	23	mA
Functional Test, Typical Voltage (Relaxed Limits)	-	3014	V_{DD}=3.3V, V_{SS}=0V V_{IH}=3.3V, V_{IL}=0V (Pin Groups 1 to 3) V_{OH}=1.8V, V_{OL}=1.3V I_{OL}=I_{OH}=0A (Pin Groups 4 to 6) I_{OL}=0A (Pin Group 7) C_{LOAD}<62pF Use pattern *main_pattern* @10MHz Note 4	Go/NoGo		-

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions	Limits		Units
				Min	Max	
Functional Test, Minimum Voltage (Specified Limits)	-	3014	V_{DD}=2.85V, V_{SS}=0V V_{IH}=1.98V, V_{IL}=870mV (Pin Groups 1 and 2) V_{IH}=2.85V, V_{IL}=0V (Pin Group 3) V_{OH}=2.465V, V_{OL}=385mV (Pin Groups 4 to 7) I_{OL}/ I_{OH}=-3 / +6mA (Pin Group 4) I_{OL}/ I_{OH}=±200µA (Pin Group 5) I_{OL}/ I_{OH}=±100µA (Pin Group 6) I_{OL}=-1mA (Pin Group 7) C_{LOAD}<62pF Use pattern *main_pattern* @10MHz Note 4	Go/NoGo		-
Functional Test, Maximum Voltage (Specified Limits)	-	3014	V_{DD}=3.45V, V_{SS}=0V V_{IH}=2.4V, V_{IL}=1.05V (Pin Groups 1 and 2) V_{IH}=3.45V, V_{IL}=0V (Pin Group 3) V_{OH}=3.065V, V_{OL}=385mV (Pin Groups 4 to 7) I_{OL}/ I_{OH}=-3 / +6mA (Pin Group 4) I_{OL}/ I_{OH}=±200µA (Pin Group 5) I_{OL}/ I_{OH}=±100µA (Pin Group 6) I_{OL}=-1mA (Pin Group 7) C_{LOAD}<62pF Use pattern *main_pattern* @10MHz Note 4	Go/NoGo		-
CMOS Input Voltage, Low Level (Minimum V_{DD})	V_{IL1}	-	Pin Groups 1 and 2 V_{DD}=2.85V, V_{SS}=0V Use pattern *main_pattern* Note 5	855	-	mV
CMOS Input Voltage, High Level (Minimum V_{DD})	V_{IH1}	-	Pin Groups 1 and 2 V_{DD}=2.85V, V_{SS}=0V Use pattern *main_pattern* Note 5	-	1995	mV
CMOS Output Voltage, Low Level (High Current Buffer at Minimum V_{DD})	V_{OL1_H}	3007	Pin Group 4 V_{DD}=2.85V, V_{SS}=0V I_{OL}=-6mA Use pattern *main_pattern* Note 6	-	400	mV

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions	Limits		Units
				Min	Max	
CMOS Output Voltage, Low Level (Low Current Buffer at Minimum V_{DD})	V_{OL1_L}	3007	Pin Group 5 V_{DD}=2.85V, V_{SS}=0V I_{OL}=-200µA Use pattern *main_pattern* Note 6	-	400	mV
CMOS Output Voltage, Low Level (Buffer with Serial Resistor at Minimum V_{DD})	V_{OL1_R}	3007	Pin Group 6 V_{DD}=2.85V, V_{SS}=0V I_{OL}=-100µA Use pattern *main_pattern* Note 6	-	400	mV
CMOS Output Voltage, Low Level (Open Drain Buffer at Minimum V_{DD})	V_{OL1_OD}	3007	Pin Group 7 V_{DD}=2.85V, V_{SS}=0V I_{OL}=-1mA Use pattern *main_pattern* Note 6	-	400	mV
CMOS Output Voltage, Low Level (High Current Buffer at Maximum V_{DD})	V_{OL2_H}	3007	Pin Group 4 V_{DD}=3.45V, V_{SS}=0V I_{OL}=-6mA Use pattern *main_pattern* Note 6	-	400	mV
CMOS Output Voltage, Low Level (Low Current Buffer at Maximum V_{DD})	V_{OL2_L}	3007	Pin Group 5 V_{DD}=3.45V, V_{SS}=0V I_{OL}=-200µA Use pattern *main_pattern* Note 6	-	400	mV
CMOS Output Voltage, Low Level (Buffer with Serial Resistor at Maximum V_{DD})	V_{OL2_R}	3007	Pin Group 6 V_{DD}=3.45V, V_{SS}=0V I_{OL}=-100µA Use pattern *main_pattern* Note 6	-	400	mV
CMOS Output Voltage, Low Level (Open Drain Buffer at Maximum V_{DD})	V_{OL2_OD}	3007	Pin Group 7 V_{DD}=3.45V, V_{SS}=0V I_{OL}=-1mA Use pattern *main_pattern* Note 6	-	400	mV
CMOS Output Voltage, High Level (High Current Buffer at Minimum V_{DD})	V_{OH1_H}	3006	Pin Group 4 V_{DD}=2.85V, V_{SS}=0V I_{OH}=3mA Use pattern *main_pattern* Note 6	2.45	-	V

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions	Limits		Units
				Min	Max	
CMOS Output Voltage, High Level (Low Current Buffer at Minimum V_{DD})	V_{OH1_L}	3006	Pin Group 5 V_{DD}=2.85V, V_{SS}=0V I_{OH}=200µA Use pattern *main_pattern* Note 6	2.45	-	V
CMOS Output Voltage, High Level (Buffer with Serial Resistor at Minimum V_{DD})	V_{OH1_R}	3006	Pin Group 6 V_{DD}=2.85V, V_{SS}=0V I_{OH}=100µA Use pattern *main_pattern* Note 6	2.45	-	V
CMOS Output Voltage, High Level (High Current Buffer at Maximum V_{DD})	V_{OH2_H}	3006	Pin Group 4 V_{DD}=3.45V, V_{SS}=0V I_{OH}=3mA Use pattern *main_pattern* Note 6	3.05	-	V
CMOS Output Voltage, High Level (Low Current Buffer at Maximum V_{DD})	V_{OH2_L}	3006	Pin Group 5 V_{DD}=3.45V, V_{SS}=0V I_{OH}=200µA Use pattern *main_pattern* Note 6	3.05	-	V
CMOS Output Voltage, High Level (Buffer with Serial Resistor at Maximum V_{DD})	V_{OH2_R}	3006	Pin Group 6 V_{DD}=3.45V, V_{SS}=0V I_{OH}=100µA Use pattern *main_pattern* Note 6	3.05	-	V
CMOS Input Leakage Current, Low Level (with Pull-down)	I_{IL_PD}	3009	Pin Group 1 V_{DD}=3.45V V_{SS}=0V V_{IN}(Under Test)=0V V_{IN}(Remaining Inputs)=3.45V	-250	250	nA
CMOS Input Leakage Current, Low Level	I_{IL}	3009	Pin Group 2 V_{DD}=3.45V V_{SS}=0V V_{IN}(Under Test)=0V V_{IN}(Remaining Inputs)=3.45V	-15	-50	µA
CMOS Input Leakage Current, High Level (with Pull-down)	I_{IH_PD}	3010	Pin Group 1 V_{DD}=3.45V V_{SS}=0V V_{IN}(Under Test)=3.45V V_{IN}(Remaining Inputs)=0V	30	75	µA

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions	Limits		Units
				Min	Max	
CMOS Input Leakage Current, High Level	I_{IH}	3010	Pin Group 2 V_{DD}=3.45V V_{SS}=0V V_{IN}(Under Test)=3.45V V_{IN}(Remaining Inputs)=0V	15	50	µA
High-Impedance Output Leakage Current, High Level	I_{OZH}	3021	Pin Group 7 V_{DD}=3.45V, V_{SS}=0V V_{OUT}=3.45V Use pattern *main_pattern*, stop at label *pdwn_sp* Note 7	-	10	µA
Serial Clock Minimum Pulse Width High (Minimum V_{DD})	t_{CLKH}	3003	V_{DD}=2.85V, V_{SS}=0V From posedge SCLK (↑ #18) to negedge SCLK (↓ #18) Use pattern *main_pattern* Note 10	-	30	ns
Serial Clock Minimum Pulse Width Low (Minimum V_{DD})	t_{CLKL}	3003	V_{DD}=2.85V, V_{SS}=0V From negedge SCLK (↓ #18) to posedge SCLK (↑ #18) Use pattern *main_pattern* Note 10	-	30	ns
Serial Data to Serial Clock Setup Time (Minimum V_{DD})	t_{DSU}	3003	V_{DD}=2.85V, V_{SS}=0V From any edge of SDATA (#16) to posedge SCLK (↑ #18) Use pattern *main_pattern* Note 10	-	10	ns
Serial Data to Serial Clock Hold Time (Minimum V_{DD})	t_{DH}	3003	V_{DD}=2.85V, V_{SS}=0V From posedge SCLK (↑ #18) to any edge of SDATA (#16) Use pattern *main_pattern* Note 10	-	10	ns
Serial Load Minimum Pulse Width High (Minimum V_{DD})	t_{PWH}	3003	V_{DD}=2.85V, V_{SS}=0V From posedge S_WR (↑ #15) to negedge S_WR (↓ #15) Use pattern *main_pattern* Note 10	-	30	ns
Serial Clock Rising Edge to Serial Load Rising Edge (Minimum V_{DD})	t_{CWR}	3003	V_{DD}=2.85V, V_{SS}=0V From posedge SCLK (↑ #18) to posedge S_WR (↑ #15) Use pattern *main_pattern* Note 10	-	30	ns

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions	Limits		Units
				Min	Max	
Serial Clock Falling Edge to Enhancement Write Transition (Minimum V_{DD})	t_{CE}	3003	V_{DD}=2.85V, V_{SS}=0V From negedge SCLK (↓ #18) to any edge of E_WR (#24) Use pattern *main_pattern* Note 10	-	30	ns
Serial Load Falling Edge to Serial Clock Rising Edge (Minimum V_{DD})	t_{WRC}	3003	V_{DD}=2.85V, V_{SS}=0V From negedge S_WR (↓ #15) to posedge SCLK (↑ #18) Use pattern *main_pattern* Note 10	-	30	ns
Enhancement Transition to Serial Clock Rising Edge (Minimum V_{DD})	t_{EC}	3003	V_{DD}=2.85V, V_{SS}=0V From any edge of E_WR (#24) to posedge SCLK (↑ #18) Use pattern *main_pattern* Note 10	-	30	ns
MSEL Output Rising Delay from FIN Rising Edge (Minimum V_{DD})	t_{DOH}	3003	V_{DD}=2.85V, V_{SS}=0V From posedge FIN (↑ #27) to posedge DOUT (↑ #32) Use pattern *main_pattern* Note 10	-	30	ns
MSEL Output Falling Delay from FIN Rising Edge (Minimum V_{DD})	t_{DOL}	3003	V_{DD}=2.85V, V_{SS}=0V From posedge FIN (↑ #27) to negedge DOUT (↓ #32) Use pattern *main_pattern* Note 10	-	30	ns
Reference Clock Input Sensitivity	S_{FR}	-	V_{DD}=2.85V, V_{SS}=0V f_{IN}=100MHz Use pattern *mode*, stop at label *mode_sp2* Note 11	-	-5	dBm
Prescaler Input Sensitivity (Minimum f_{IN})	S_{FIN250}	-	V_{DD}=2.85V, V_{SS}=0V f_{IN}=250MHz Use pattern *mode*, stop at label *mode_sp2* Note 11	-	-5	dBm
Prescaler Input Sensitivity (Medium 1 f_{IN})	S_{FIN300}	-	V_{DD}=2.85V, V_{SS}=0V f_{IN}=300MHz Use pattern *mode*, stop at label *mode_sp2* Note 11	-	-5	dBm
Prescaler Input Sensitivity (Medium 2 f_{IN})	S_{FIN500}	-	V_{DD}=2.85V, V_{SS}=0V f_{IN}=500MHz Use pattern *mode*, stop at label *mode_sp2* Note 11	-	-5	dBm

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions	Limits		Units
				Min	Max	
Prescaler Input Sensitivity (Medium 3 f_{IN})	$S_{FIN1000}$	-	V_{DD}=2.85V, V_{SS}=0V f_{IN}=1000MHz Use pattern *mode*, stop at label *mode_sp2* Note 11	-	-5	dBm
Prescaler Input Sensitivity (Medium 4 f_{IN})	$S_{FIN2000}$	-	V_{DD}=2.85V, V_{SS}=0V f_{IN}=2000MHz Use pattern *mode*, stop at label *mode_sp2* Note 11	-	-5	dBm
Prescaler Input Sensitivity (Medium 5 f_{IN})	$S_{FIN3000}$	-	V_{DD}=2.85V, V_{SS}=0V f_{IN}=3000MHz Use pattern *mode*, stop at label *mode_sp2* Note 11	-	-5	dBm
Prescaler Input Sensitivity (Maximum f_{IN})	$S_{FIN3250}$	-	V_{DD}=2.85V, V_{SS}=0V f_{IN}=3250MHz Use pattern *mode*, stop at label *mode_sp2* Note 11	-	-5	dBm
Prescaler Input Sensitivity (Maximum f_{IN}, Typical V_{DD})	$S_{FIN3300}$	-	V_{DD}=3.15V, V_{SS}=0V f_{IN}=3300MHz Use pattern *mode*, stop at label *mode_sp2* Note 11	-	0	dBm
Prescaler Input Sensitivity (> Maximum f_{IN}, Typical V_{DD})	$S_{FIN3550}$	-	V_{DD}=3.15V, V_{SS}=0V f_{IN}=3550MHz Use pattern *mode*, stop at label *mode_sp2* Note 11	-	0	dBm
Supply Current during Phase Noise Measurements, Typical Low V_{DD}	$I_{DDOPPN1}$	3005	V_{DD}=3V, V_{SS}=0V Note 13	5	80	mA
Supply Current during Phase Noise Measurements, Typical High V_{DD}	$I_{DDOPPN2}$	3005	V_{DD}=3.3V, V_{SS}=0V Note 13	5	80	mA
Phase Noise @ 100Hz Offset, Typical Low V_{DD}	$PN_{100}1$	-	V_{DD}=3V, V_{SS}=0V Note 12	-95	-70	dBc/Hz
Phase Noise @ 1kHz Offset, Typical Low V_{DD}	$PN_{1K}1$	-	V_{DD}=3V, V_{SS}=0V Note 12	-101	-81	dBc/Hz

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions	Limits		Units
				Min	Max	
Phase Noise @ 10kHz Offset, Typical Low V_{DD}	$PN_{10K}1$	-	V_{DD}=3V, V_{SS}=0V Note 12	-107	-89	dBc/Hz
Phase Noise @ 100Hz Offset, Typical High V_{DD}	$PN_{100}2$	-	V_{DD}=3.3V, V_{SS}=0V Note 12	-95	-83	dBc/Hz
Phase Noise @ 1kHz Offset, Typical High V_{DD}	$PN_{1K}2$	-	V_{DD}=3.3V, V_{SS}=0V Note 12	-101	-91	dBc/Hz
Phase Noise @ 10kHz Offset, Typical High V_{DD}	$PN_{10K}2$	-	V_{DD}=3.3V, V_{SS}=0V Note 12	-107	-96	dBc/Hz

NOTES:

1. Continuity test
   Comparison limit value, no measurement value recorded.
2. Dynamic current
   For measurement of the dynamic current, the pattern *main_pattern* is used and loops from first to last vector. Instantaneous current is measured and recorded (without any link to a specific vector number). Total combined current for all V_{DD} pins. During the test, outputs are loaded with a capacitive load < 62 pF (tester load) but without active load. Comparators are disabled during this test.
3. Quiescent current
   During quiescent current test, outputs are loaded without active current load but with a capacitive load < 62 pF (tester load).
   The measurement is performed with the device having been initialised using pattern *mode*, stopped at end of vector labelled *pdwn_sp*. Total combined current of all V_{DD} pins.
   The measurement accuracy is better than 1µA.
4. Functional test
   During functional test, outputs are loaded with an active current load (when specified) and a capacitive load < 62 pF (tester load). For the active current load, the threshold load switching is set to $V_{DD}/2$.
   Output comparison is performed as “strobe comparison”. Strobe is placed 5% before the end of the period. For the open-drain output (i.e. pin 44, LD), comparison to the “High-Impedance” state may be masked for some vectors.
5. Input voltages
   During input voltage test, outputs are loaded with an active current load (when specified) and a capacitive load < 62 pF (tester load). For the active current load, the threshold load switching is set to $V_{DD}/2$.
   Measurements are performed using the test pattern *main_pattern* (between the labels “main_st” and “end_u_d”). The pattern is run with increasing or decreasing input voltage value of the pin under test until the first output fails. Remaining pins toggle with nominal input voltages.
   All the values are tested and recorded for each input.
   The measurement accuracy is better than 100mV.
6. Output voltages
   Measurements are performed using the test pattern *main_pattern*.
   The device is configured into correct state so that outputs are placed in high or low voltages. Output current is sourced/sinked and the resulting voltage is measured.
   All the values are tested and recorded for each output.
7. High impedance leakage current
   The device is configured into the correct state using the pattern *main_pattern* so that the pin under

test is in high impedance condition (i.e. stop at label “llzhh”).
All the values are tested and recorded for each output.

8. Test patterns
Number of vectors (clock periods) for patterns used during test are:

- *main_pattern* 4371 vectors @ 1MHz (period = 1000ns) and 10MHz (period = 100ns)
- *mode* 41 vectors @ 1 MHz (period = 1000ns)

9. Timing generators
All inputs use DATA mode timing generators (i.e. NRZ mode with zero delay) unless otherwise specified. The table below describes the timing generators. All patterns use the same set of timing generators:

Timing Generator Number	Period (ns)	Pin Group	Delay (ns)	Width (ns)	Comp. Start (ns)	Comp. Stop (ns)	Format
0	1000	1 to 3	0	-	-	-	NRZ
		4 to 7	-	-	-	900	EDGE
1	1000	1	0	-	-	-	NRZ
		2 and 3	100	-	-	-	NRZ
		4 to 7	-	-	-	950	EDGE
2	1000	1 (except SCLK pin)	0	-	-	-	NRZ
		SCLK pin	250	-	-	-	NRZ
		2 and 3	100	-	-	-	NRZ
		4 to 7	-	-	-	950	EDGE
3	1000	1	0	-	-	-	NRZ
		2 and 3	100	-	-	-	NRZ
		4 to 7	-	-	-	950	EDGE
4	1000	1	0	-	-	-	NRZ
		2 and 3	100	-	-	-	NRZ
		4 to 7	-	-	-	950	EDGE
5	100	1 (except SCLK pin)	0	-	-	-	NRZ
		SCLK pin	25	-	-	-	NRZ
		2 and 3	10	-	-	-	NRZ
		4 to 7	-	-	-	95	EDGE
6	1000	1	0	-	-	-	NRZ
		2 and 3	100	-	-	-	NRZ
		4 to 7	-	-	-	950	EDGE
11	1000	2 and 3	100	-	-	-	NRZ
		4 to 7	-	-	-	950	EDGE

10. Dynamic measurements
Parameters shall be measured and recorded for each dynamic parameter to be tested. The

measurement accuracy is better than 0.5ns.

11. RF measurements
The frequency is set to the target frequency and output level at the FIN pin. The resulting output power is measured on DOUT.
The measurement accuracy is better than 0.1dB.

12. Phase Noise measurements
The Phase Noise measurements use a "Stack-and-Rack" solution. The parametric test settings are described hereafter:
– f_{IN} =1920 MHz
– f_r = 100 MHz (0dBm)
– f_c = 20MHz
– Loop Bandwidth = 50kHz
– Register M = 8
– Register R = 4
– Register A = 6
– Modulus = 10

13. Operating current during Phase Noise measurement
The parametric test settings are described in Note 12 above.

2.3.2 High and Low Temperatures Electrical Measurements

The measurements shall be performed at T_{amb}=+85 (+0 -5)°C and T_{amb}=- 40(+5-0)°C.

The characteristics, test methods, conditions and limits shall be the same as specified for Room Temperature Electrical Measurements, except as follows:

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions	Limits		Units
				Min	Max	
Standby Supply Current with Prescaler	I_{DDQ1}	3005	V_{DD}=3.45V, V_{SS}=0V Use pattern *mode,* stop at label *pdwn_sp*	-	1000	µA

2.4 PARAMETER DRIFT VALUES

Unless otherwise specified, the measurements shall be performed at T_{amb}=+22 ± 3°C.

The test methods and test conditions shall be as per the corresponding test defined in Room Temperature Electrical Measurements.

The drift values (Δ) shall not be exceeded for each characteristic specified. The corresponding absolute limit values for each characteristic shall not be exceeded.

Characteristics	Symbols	Limits			Units
		Drift Value Δ	Absolute		
			Min	Max	
Supply Current during Phase Noise Measurements, Typical High V_{DD}	$I_{DDOPPN2}$	±10%	5	80	mA
CMOS Output Voltage, Low Level (High Current Buffer at Minimum V_{DD})	V_{OL1_H}	±50	-	400	mV
CMOS Output Voltage, High Level (High Current Buffer at Minimum V_{DD})	V_{OH1_H}	±0.1	2.45	-	V
Prescaler Input Sensitivity (Medium 1 f_{IN})	S_{FIN300}	±3	-	-5	dBm

2.5 INTERMEDIATE AND END-POINT ELECTRICAL MEASUREMENTS

Unless otherwise specified, the measurements shall be performed at T_{amb}=+22 ±3°C.

The characteristics, test methods, conditions and limits shall be as specified for Room Temperature Electrical Measurements.

2.6 POWER BURN-IN CONDITIONS

2.6.1 Electrical Test Conditions

Electrical test conditions shall be in accordance with the table below:

Characteristics	Symbols	Test Conditions	Units
Core Supply Voltage	V1	3.45 (+0 -5%)	V
Output Bias Voltage	V2	1.725 (±5%)	V
Input Voltage (Digital Inputs)	V_{IN}	0 to V1	V
Vector Length	t_O	1	µs

2.6.2 Environmental Test Conditions

Environmental test conditions shall be in accordance with the table below:

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	T_{amb}	+125 (+0 -5)	°C

2.6.3 Burn-in Stimulus

The device shall be burned-in using “functional” vectors.

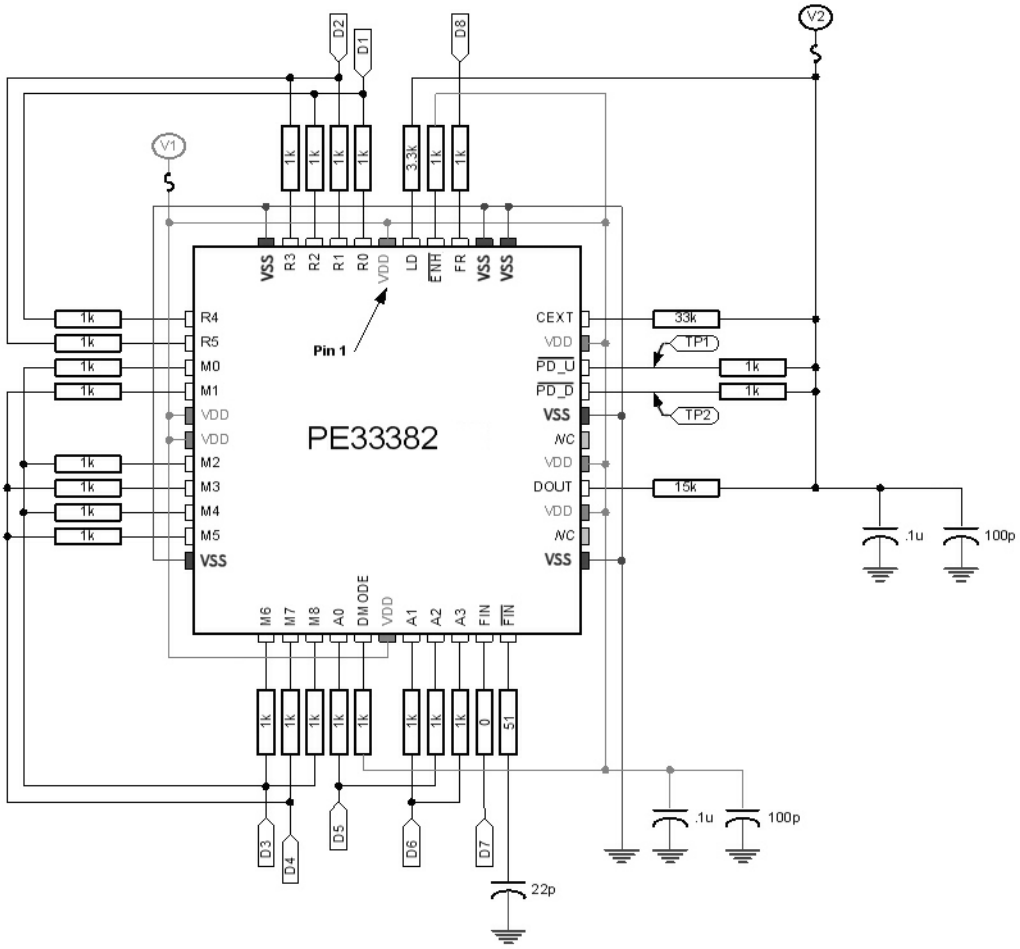
The Burn-in stimulus shall be made with vectors looping indefinitely. Each vector shall be made with thirteen (13) drivers. Each driver uses DATA mode, i.e. Non Return to Zero (NRZ) mode with toggling at the beginning of the vector. Looping this burn-in pattern exercises the PLL and $\overline{PD\_U}$/$\overline{PD\_D}$ outputs toggle.

The device shall be set up in direct mode and counters loaded with checkerboard values in such a way that the $\overline{PD\_U}$ and $\overline{PD\_D}$ pins toggle alternately. The device shall go sequentially through eight (8) normal modes. Each mode includes two hundred and eighteen (218) vectors or one hundred and nine (109) FIN clock cycles. FR toggles every eleven (11) periods of FIN. There shall be 1962 vectors.

A (hex)	M (hex)	R (hex)
5	55	5
5	55	A
5	2A	5
5	2A	A
A	55	5
A	55	A
A	2A	5
A	2A	A

2.6.4 Burn-in Schematic

The following schematic shows a suitable burn-in configuration for a single socket.



NOTES:

1. V1 is connected via a 250mA fuse.
2. V2 is connected via a 20mA fuse.
3. All resistors have a tolerance of ±1%. All capacitors have a tolerance of ±10%.
4. D1, D2, D3 etc. are Driver Numbers.
5. TP1 and TP2 are the Test Probes.

2.7 OPERATING LIFE CONDITIONS

The conditions shall be as specified for Power Burn-in.

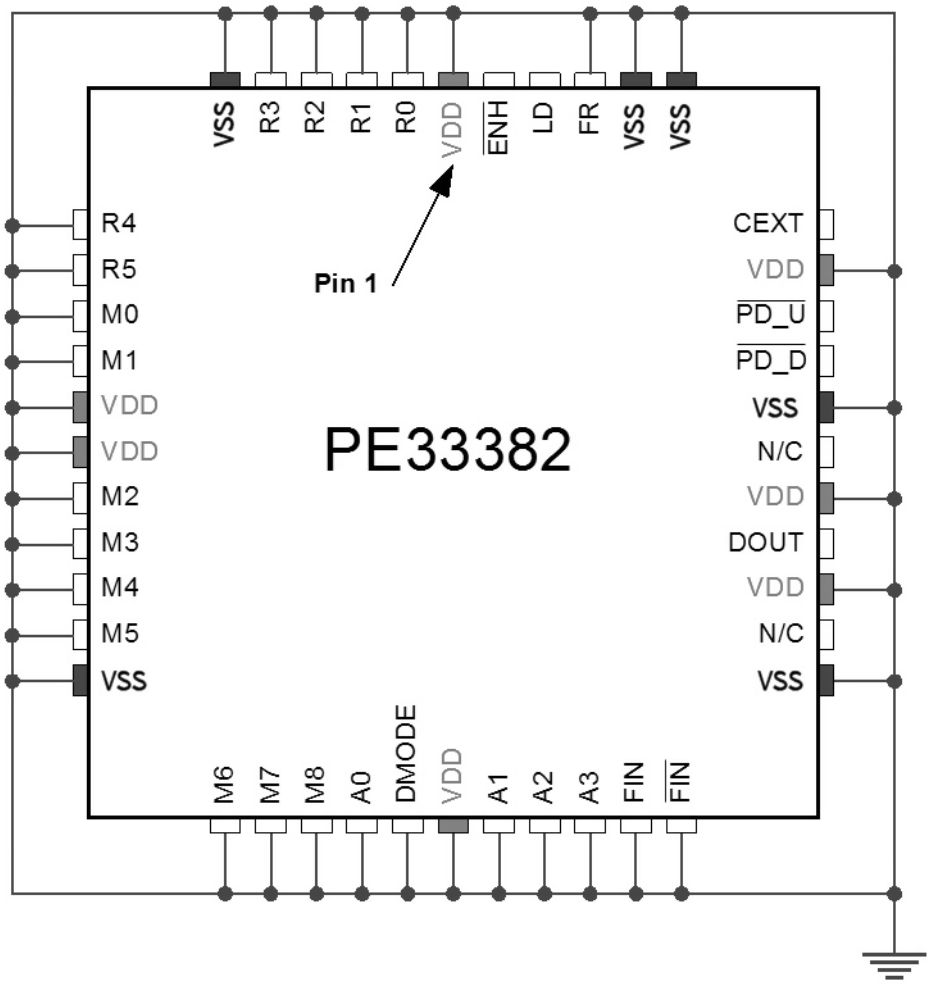
2.8 TOTAL DOSE RADIATION TESTING

2.8.1 Bias Conditions and Total Dose Level for Total Dose Radiation Testing

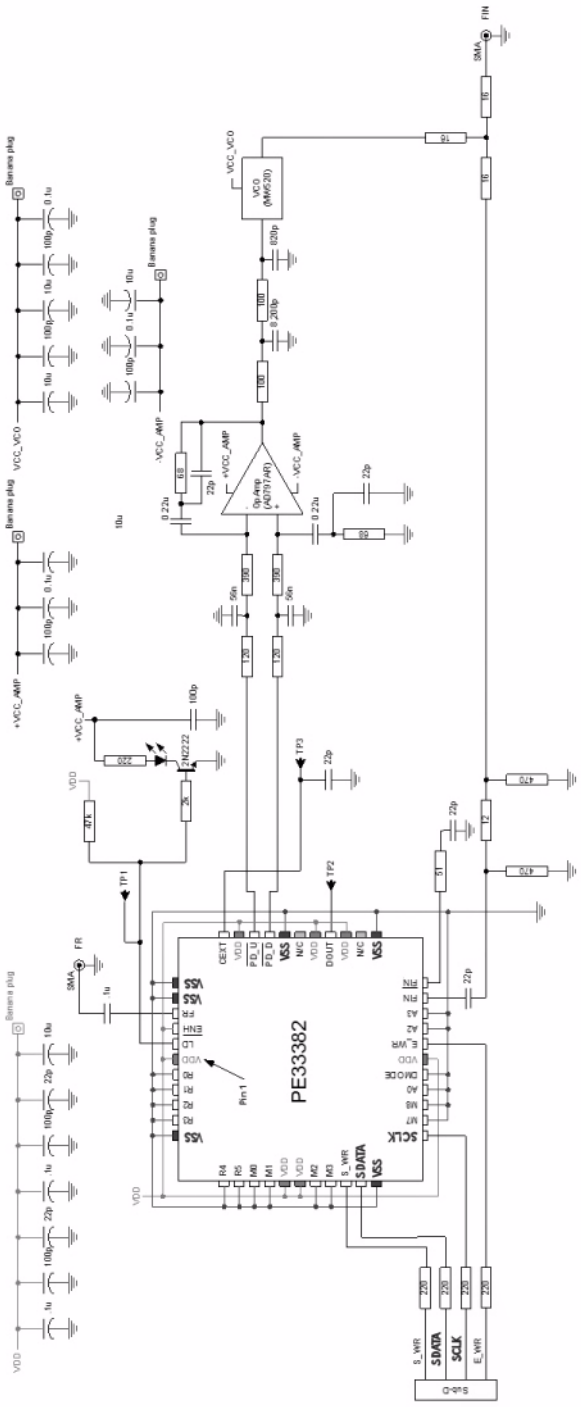
Bias shall be applied during irradiation testing as specified below.

The total dose level applied shall be as specified in the component type variant information herein or in the Purchase Order.

The following schematic shows a suitable test configuration for a single socket in unbiased condition (OFF).



The following schematic shows a suitable test configuration for a single socket in biased condition (ON).



NOTES:

1. V_{DD}=3.3V, V_{CC}_VCO=5±0.2V, +V_{CC}_AMP=5V and -V_{CC}_AMP=-5V.
2. f_r=40MHz, V_P=V_{SS} to V_{DD}.
3. f_{IN}=1920 MHz, V_P=V_{SS} to V_{DD}.
4. All resistors have a tolerance of ±1%. All capacitors have a tolerance of ±10%.
5. TP1, TP2 and TP3 are the Test Probes.
6. The table below shows how the device shall be serially programmed during Total Dose Radiation Testing so the f_{IN} frequency is 1920 MHz.

Description	Value
R Counter	1
M Counter	8
A Counter	6
Reference Frequency	40 MHz

2.8.2 Electrical Measurements for Total Dose Radiation Testing

Unless otherwise specified the measurements shall be performed at T_{amb}=22±3°C.

The characteristics, test methods, conditions and limits shall be as specified for Room Temperature Electrical Measurements.

APPENDIX 'A'

AGREED DEVIATIONS FOR PEREGRINE SEMICONDUCTOR EUROPE

ITEMS AFFECTED	DESCRIPTION OF DEVIATIONS
Deviations from Wafer Lot Acceptance - Chart F2	The SEM inspection may be performed using the specified ESCC Method or, alternatively, may be carried out in accordance with the requirements of MIL-STD-883 Test Method 2018.
Deviations from Screening Tests - Chart F3	Following the PIND test, a Seal Test (Fine and Gross Leak) shall be performed in accordance with MIL-STD-883 Test Method 1014. An External Visual Inspection shall then be performed in accordance with ESCC Basic Specification No. 20500. Initial High and Low Temperatures Electrical Measurements may be performed prior to Burn-in at the option of the Manufacturer. The Check for Lot Failure shall only take into account any failures during Room Temperature Electrical Measurements. The number of failed components shall not exceed 5% of the components submitted to Burn-in. Room Temperature Electrical Measurements may be performed after Seal Test (Fine and Gross Leak).
Deviations from Qualification and Periodic Tests - Chart F4	Permanence of Marking shall not be performed on devices which have been laser marked.