TRANSISTORS, MICROWAVE, FIELD EFFECT,

POWER, GALLIUM ARSENIDE

BASED ON TYPE CLY35 AND CLY38

ESCC Detail Specification No. 5614/008

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Pages 1 to 24

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1. GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics, test and inspection data for a Transistor, Microwave, Metal Semiconductor Field Effect (MESFET), L/C Band, Power, Gallium Arsenide, based on Types CLY35 and CLY38. It shall be read in conjunction with ESA/SCC Generic Specification No. 5010, the requirements of which are supplemented herein.

1.2 COMPONENT TYPE VARIANTS

Variants of the basic type transistors specified herein, which are also covered by this specification, are given in Table 1(a).

1.3 MAXIMUM RATINGS

The maximum ratings, which shall not be exceeded at any time during use or storage, applicable to the transistors specified herein, are as scheduled in Table 1(b).

1.4 PARAMETER DERATING INFORMATION

The derating information applicable to the transistors specified herein is shown in Figure 1.

1.5 PHYSICAL DIMENSIONS

The physical dimensions of the transistors specified herein are shown in Figure 2.

1.6 FUNCTIONAL DIAGRAM

The functional diagram, showing lead identification of the transistors specified herein, is shown in Figure 3.

1.7 HANDLING PRECAUTIONS

These devices are susceptible to damage by electrostatic discharge. Therefore suitable precautions shall be employed for protection during all phases of manufacture test, packaging, shipping and handling.

These components are catagorised as follows:-

(a) Variants 01 to 03 - Class 3 with a Minimum Critical Path Failure Voltage of 6000V.

(b) Variants 04 to 06 - Class 2 with a Minimum Critical Path Failure Voltage of 3000V.

2. APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:

(a) ESA/SCC Generic Specification No. 5010 for Discrete Microwave Semiconductor Components.

(b) MIL-STD-750, Test Methods for Semiconductor Devices.

TABLE 1(a) - TYPE VARIANTS

(1) VARIANT	(2) BASED ON TYPE	(3) CASE	(4) FIGURE	(5) OUTPUT POWER @ 1dB GAIN COMPRESSION	(6) LID AND LEAD MATERIAL AND FINISH
01	CLY38-10	MWP35	2	38.5	D2
02	CLY38-05	MWP35	2	38	D2
03	CLY38-00	MWP35	2	37.5	D2
04	CLY35-10	MWP35	2	35.5	D2
05	CLY35-05	MWP35	2	35	D2
06	CLY35-00	MWP35	2	34.5	D2

TABLE 1(b) - MAXIMUM RATINGS

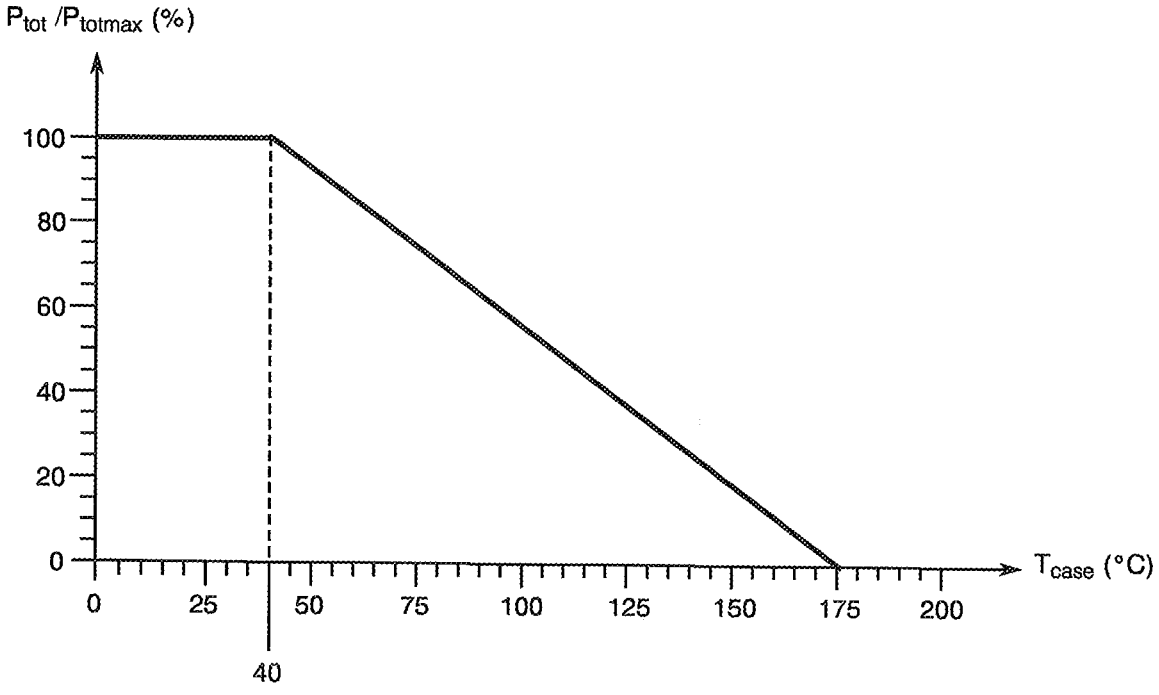
No.	CHARACTERISTICS	SYMBOL	MAXIMUM RATINGS	UNIT	REMARKS
1	Drain-Source Voltage	V_{DS}	14	V	
2	Drain-Gate Voltage	V_{DG}	16	V	Note 1
3	Gate-Source Voltage	V_{GS}	−6.0	V	Note 1
4	Drain Current Variants 01 to 03 Variants 04 to 06	I_D	 5.6 at $V_{DS} \leq 5.6V$ 2.8 at $V_{DS} \leq 6.4V$	A	
5	Gate Current Variants 01 to 03 Variants 04 to 06	I_G	 32 16	mA	
6	Operational Gate Current Variants 01 to 03 Variants 04 to 06	I_{GO}	 -8 to +32 -4 to +16	mA	
7	Compression Level Variants 01 to 03 Variants 04 to 06	P_c	 <1.5 at $V_{DS} \leq 9.0V$, $0.9A < I_D < 1.9A$ <2.5 at $V_{DS} \leq 8.0V$, $0.9A < I_D < 1.9A$ <3.5 at $V_{DS} \leq 7.0V$, $0.9A < I_D < 1.9A$ <1.5 at $V_{DS} \leq 9.0V$, $0.5A < I_D < 1.0A$ <2.5 at $V_{DS} \leq 8.0V$, $0.5A < I_D < 1.0A$ <3.5 at $V_{DS} \leq 7.0V$, $0.5A < I_D < 1.0A$	dB	Note 2
8	Power Dissipation Variants 01 to 03 Variants 04 to 06	P_{tot}	 31.4 18	W	Note 3
9	Channel Temperature Range	T_{Ch}	- 65 to + 175	°C	
10	Storage Temperature Range	T_{stg}	−65 to +175	°C	
11	Soldering Temperature	T_{sol}	+230	°C	Note 4

NOTES: See Page 7.

NOTES

1. For the purpose of I_{Dp1} and I_{Gp1} measurements, $16V < V_{DG} \leq 22V$ and $-6.0V < V_{GS} \leq -10V$ is allowed for <1sec in total.
2. Under continuous wave.
3. At $T_C = +40°C$. For derating at $T_C > +40°C$, see Figure 1.
4. Duration 15 seconds maximum for the leads, 5 seconds maximum for the body at a distance of not less than 0.5mm from the device body and the same termination shall not be resoldered until 3 minutes have elapsed.

FIGURE 1 - PARAMETER DERATING INFORMATION

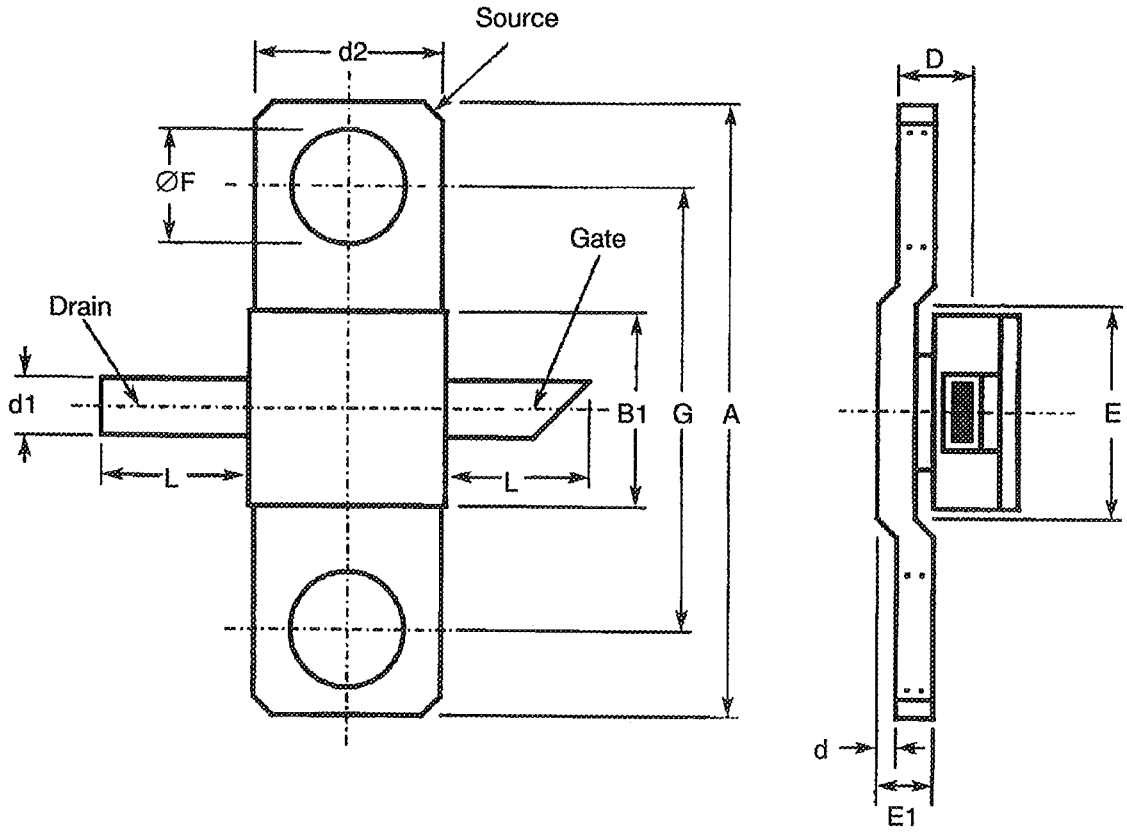


Power Dissipation versus Temperature

NOTES

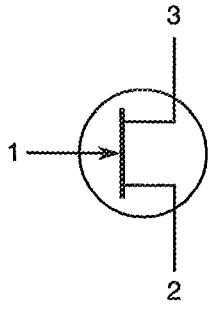
1. Thermal Resistance ($R_{TH(ch-c)}$)
   Variants 01 to 03 4.3 °C/W.
   Variants 04 to 06 7.5 °C/W.

FIGURE 2 - PHYSICAL DIMENSIONS



SYMBOL	MILLIMETRES		NOTES
	MIN.	MAX.	
A	9.8	10.2	
B1	3.3	3.7	
d	0.03	0.2	
d1	0.43	0.59	
d2	3.1	3.5	
D	1.63	1.67	
E	3.5	4.1	
E1	0.8	1.2	
ØF	1.6	2.0	
G	6.5	6.9	
L	1.7	2.7	

FIGURE 3 - FUNCTIONAL DIAGRAM



1. Gate
2. Source
3. Drain

3. TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESA/SCC Basic Specification No. 21300 shall apply. In addition, the following symbols are used:-

D	=	Drain.
G	=	Gate.
G_{lp}	=	Linear (small signal) Gain for Power Matching Condition.
G_P	=	Power (large signal) Gain for Power Matching Condition.
g_m	=	Transconductance.
I_D	=	Drain Current.
$I_{D\text{-}1dB}$	=	D.C. Drain Current under 1dB compression.
I_{Dp}	=	Drain Leakage Current at Pinch-off.
I_{Dq}	=	Drain Quiescent Current (Drain Operational Current without RF Excitation).
I_{DSS}	=	Drain Saturation Current for Shorted Gate ($V_{GS}=0$).
I_G	=	Gate Current.
$I_{G\text{-}1dB}$	=	D.C. Gate Current under 1dB compression.
I_{GO}	=	Gate d.c. Current under RF (Gate Operational Mean Current under RF Excitation).
I_{Gp}	=	Gate Leakage Current at Pinch-off.
PAE	=	Power Added Efficiency (= $[(P_{out}-P_{in})/P_{DC}]$x100%).
P_c	=	Power Gain Compression Level.
P_{DC}	=	Dissipated d.c. Power.
P_G	=	Adjustable Voltage Divider to adjust I_D by means of V_{GS}.
P_{in}	=	RF Input Power.
P_{out}	=	RF Output Power.
P_{tot}	=	Power Dissipation (= $P_{DC}+P_{in}-P_{out}$).
PTC	=	Positive Temperature Coefficient Thermistor.
$P_{\text{-}1dB}$	=	Output Power at 1dB Gain Compression.
R_D	=	External Drain Resistance.
R_G	=	External Gate Resistance.
R_S	=	External Source Resistance.
$R_{TH(ch\text{-}c)}$	=	Thermal Resistance, Channel to Case.
$R_{TH(C\text{-}HS)}$	=	Thermal Resistance, Case to Heatsink.
$R_{TH(HS\text{-}A)}$	=	Thermal Resistance, Heatsink to Ambient.
S	=	Source.
V_{DD}	=	Output Voltage from Drain Power Supply.
V_{DG}	=	Drain-Gate Voltage.
V_{DS}	=	Drain-Source Voltage.
V_{GG}	=	Output Voltage from Gate Power Supply.
V_{GS}	=	Gate-Source Voltage.
V_{GSth}	=	Gate-Source Threshold Voltage (Turn-on Voltage).
V_{SS}	=	Output Voltage from Source Power Supply (Ground).

4. REQUIREMENTS

4.1 GENERAL

The complete requirements for procurement of the transistors specified herein shall be as stated in this specification and ESA/SCC Generic Specification No. 5010 for Discrete Microwave Semiconductor Components. Deviations from the Generic Specification applicable to this specification only, are listed in Para. 4.2.

Deviations from the applicable Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESA/SCC requirements and do not affect the components' reliability, are listed in the appendices attached to this specification.

4.2 DEVIATIONS FROM GENERIC SPECIFICATION

4.2.1 Deviations from Special In-process Controls

None.

4.2.2 Deviations from Final Production Tests (Chart II)

(a) Para. 9.5, Thermal Shock: May also be performed in accordance with MIL-STD-883, Test Method 1010, Test Condition C.

(b) Para. 9.7, Particle Impact Noise Detection (PIND) Test: May be performed at any point after the position indicated in Chart II(b), but before a final seal test, gross leak and fine leak.

4.2.3 Deviations from Burn-in and Electrical Measurements (Chart III)

(a) Para. 9.9.2, Table 3 measurements: May be performed at any stage after power burn-in and shall be performed on the complete lot.

(b) Para. 9.9.3, Table 2 measurements: May be performed at any stage after power burn-in.

4.2.4 Deviations from Qualification Tests (Chart IV)

(a) Paras. 9.8.1 and 9.8.2, Seal Test: The tests following Para. 9.15, Constant Acceleration shall not be performed.

(b) Para. 9.13, Shock Test: Shall not be performed.

(c) Para. 9.14, Vibration Test: Shall not be performed.

(d) Para. 9.15, Constant Acceleration: Shall not be performed.

(e) Para. 9.23, Special Testing: Shall not be performed.

(f) Assembly/Capability tests (Subgroup II): In addition to the permitted electrical rejects, components rejected from radiographic inspection, seal test or external visual inspection may also be used for these tests, if they are considered capable of passing the Assembly/Capability test sequence.

4.2.5 Deviations from Lot Acceptance Tests (Chart V)

(a) Para. 9.8.1 and 9.8.2, Seal Test: The tests following Para. 9.15, Constant Acceleration shall not be performed.

(b) Para. 9.13, Shock Test: Shall not be performed.

(c) Para. 9.14, Vibration Test: Shall not be performed.

(d) Para. 9.15, Constant Acceleration: Shall not be performed.

(e) Para. 9.23, Special Testing: Shall not be performed.

(f) Assembly/Capability tests (Subgroup II): In addition to the permitted electrical rejects, components rejected from radiographic inspection, seal test or external visual inspection may also be used for these tests, if they are considered capable of passing the Assembly/Capability test sequence.

4.3 MECHANICAL REQUIREMENTS

4.3.1 Dimension Check

The dimensions of the transistors specified herein shall be checked. They shall conform to those shown in Figure 2.

4.3.2 Weight

The maximum weight of the transistors specified herein shall be 0.6 grammes.

4.3.3 Terminal Strength

The requirements for terminal strength testing are specified in Section 9 of ESA/SCC Generic Specification No. 5010. The test conditions shall be as follows:-

(a) Condition: 'A' (Tension).

(b) Force: 2.2N.

(c) Duration: 5 seconds.

4.3.4 Bond Strength

The requirements for bond strength are specified in Section 9 of ESA/SCC Generic Specification No. 5010. The test conditions shall be as follows:-

(a) Condition: 'A'.

(b) Bond Strength: 0.03N force minimum at pre-seal tests, 0.025N force minimum at post-seal tests.

4.3.5 Die Shear

The requirements for die shear are specified in Section 9 of ESA/SCC Generic Specification No. 5010. The test conditions shall be alternatively as follows:-

(a) Minimum acceptable die shear strength: 7.3N.

(b) In those cases where the clearances in the package do not allow application of the die shear force with a suitable tool, the chip shall be pushed away with a suitable tool and the die attach area inspected afterwards.

Sufficient die attach quality is achieved if objective evidence for sufficient mechanical and thermal contact is found, i.e. more than 50% semiconductor material remains.

4.4 MATERIALS AND FINISHES

The materials and finishes shall be as specified herein. Where a definite material is not specified, a material which will enable the transistors specified herein to meet the performance requirements of this specification shall be used. Acceptance or approval of any constituent material does not guarantee acceptance of the finished product.

4.4.1 Case

The case shall be hermetically sealed and have a ceramic body on an Au over Ni plated Cu-flange.

4.4.2 Lead Material and Finish

The lid and lead material shall be Type 'D' with Type '2' finish in accordance with the requirements of ESA/SCC Basic Specification No. 23500.

4.5 MARKING

4.5.1 General

The marking of components delivered to this specification shall be in accordance with the requirements of ESA/SCC Basic Specification No. 21700 and the following paragraphs. When the component is too small to accommodate all of the marking as specified, as much as space permits shall be marked and the marking information, in full, shall accompany the component in its primary package.

The information to be marked and the order of precedence, shall be as follows:-

(a) Terminal Identification.

(b) The SCC Component Number.

(d) Traceability Information.

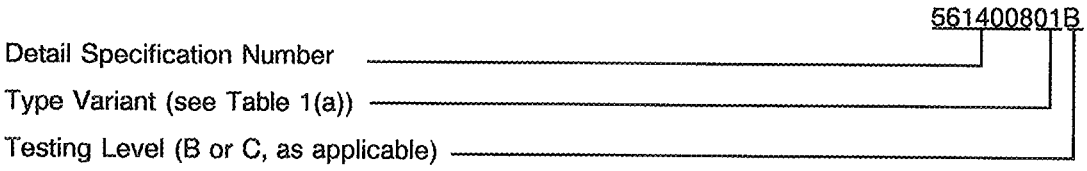
The primary package shall bear an "ESD sensitive" label.

4.5.2 Terminal Identification

Terminal identification shall be as shown in Figures 2 and 3 of this specification.

4.5.3 The SCC Component Number

Each component shall bear the SCC Component Number which shall be constituted and marked as follows:



4.5.4 Traceability Information

Each component shall be marked in respect of traceability information in accordance with the requirements of ESA/SCC Basic Specification No. 21700.

4.6 ELECTRICAL MEASUREMENTS

4.6.1 Electrical Measurements at Room Temperature

The parameters to be measured at room temperature are scheduled in Table 2. Unless otherwise specified, the measurements shall be performed at $T_{amb} = +25 \pm 3$ °C.

Within their part types, those components which fail to achieve their specified RF Classification may be assigned to another type variant, after final electrical measurements.

4.6.2 Electrical Measurements at High and Low Temperatures

The parameters to be measured at high and low temperatures are scheduled in Table 2. Unless otherwise specified, the measurements shall be performed at $T_{amb} = +140(+0-5)$°C.

4.6.3 Circuits for Electrical Measurements

Circuits for use in performing electrical measurements listed in Tables 2 and 3 of this specification are shown in Figure 4.

4.7 BURN-IN TESTS

Burn-in shall be to Chart III(b).

4.7.1 Parameter Drift Values

The parameter drift values applicable to burn-in are specified in Table 4 of this specification. Unless otherwise stated, measurements shall be performed at $T_{amb} = +25 \pm 3$ °C. The parameter drift values (Δ) applicable to the scheduled parameters shall not be exceeded. In addition to these drift value requirements, the appropriate limit value specified for a given parameter in Table 2 shall not be exceeded.

4.7.2 Conditions for High Temperature Reverse Bias Burn-in

The requirements for high temperature reverse bias burn-in are specified in Section 9 of ESA/SCC Generic Specification No. 5010. The conditions for high temperature reverse bias burn-in shall be as specified in Table 5(a) of this specification.

4.7.3 Conditions for Power Burn-in

The requirements for power burn-in are specified in Section 9 of ESA/SCC Generic Specification No. 5010. The conditions for power burn-in shall be as specified in Table 5(b) of this specification.

4.7.4 Electrical Circuits for High Temperature Reverse Bias Burn-in

The circuit for use in performing the high temperature reverse bias burn-in test is the general burn-in circuit shown in Figure 5 of this specification.

4.7.5 Electrical Circuits for Power Burn-in

The circuit for use in performing the power burn-in test is shown in Figure 5 of this specification.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - D.C. PARAMETERS

No.	CHARACTERISTICS	SYMBOL	TEST FIG.	TEST CONDITIONS	LIMITS		UNIT
					MIN.	MAX.	
1	Drain Leakage Current at Pinch-off 1	I_{Dp1}	4(a)	V_{DS} = 12V, V_{GS} = −10V (Note 1) Variants 01 to 03 Variants 04 to 06	 - -	 2.4 1.2	mA
2	Gate Leakage Current at Pinch-off 1	I_{Gp1}	4(a)	V_{DS} = 12V, V_{GS} = −10V (Note 1) Variants 01 to 03 Variants 04 to 06	 - -	 -2.4 -1.2	mA
3	Drain Leakage Current at Pinch-off 2	I_{Dp2}	4(a)	V_{DS} = 12V, V_{GS} = −4.0V Variants 01 to 03 Variants 04 to 06	 - -	 240 120	µA
4	Gate Leakage Current at Pinch-off 2	I_{Gp2}	4(a)	V_{DS} = 12V, V_{GS} = −4.0V Variants 01 to 03 Variants 04 to 06	 - -	 -240 -120	µA
5	Drain Leakage Current at Pinch-off 3	I_{Dp3}	4(a)	V_{DS} = 3.0V, V_{GS} = −3.8V Variants 01 to 03 Variants 04 to 06	 - -	 24 12	µA
6	Gate Leakage Current at Pinch-off 3	I_{Gp3}	4(a)	V_{DS} = 3.0V, V_{GS} = −3.8V Variants 01 to 03 Variants 04 to 06	 - -	 -24 -12	µA
7	Drain Saturation Current	I_{DSS}	4(a)	V_{DS} = 2.0V, V_{GS} = 0V Variants 01 to 03 Variants 04 to 06	 2.4 1.2	 5.2 2.8	A
8	Gate-Source Threshold Voltage	V_{GSth}	4(a)	V_{DS} = 3.0V Variants 01 to 03 I_D = 160mA Variants 04 to 06 I_D = 80mA	-1.6	-3.6	V
9	Transconductance	g_m	4(a)	V_{DS} = 3.0V Variants 01 to 03 I_D = 720mA Variants 04 to 06 I_D = 720mA	 900 600	 - -	mS
10	Thermal Resistance Channel to Case	$R_{TH(ch-c)}$	-	V_{DS} = 9.0V Variants 01 to 03 I_D = 720mA Variants 04 to 06 I_D = 720mA	 - -	 4.3 7.5	°C/W

NOTES: See Page 15.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - A.C. PARAMETERS

No.	CHARACTERISTICS	SYMBOL	TEST FIG.	TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNIT
11	Linear Gain	G_{lp}	4(b)	V_{DS} = 9.0V, f = 2.3GHz (Note 2) Variants 01 to 03: I_{Dq} = 1.4A, $P_{in} \leq$ 18dBm Variants 01, 02 Variant 03 Variants 04 to 06 : I_{Dq} = 0.72A, $P_{in} \leq$ 15dBm Variants 04, 05 Variant 06	 10.5 10.0 10.5 10.0	 - - - -	dB
12	Output Power @ 1dB Gain Compression	P_{-1dB}	4(b)	V_{DS} = 9.0V, f = 2.3GHz (Notes 2, 3) Variants 01 to 03: I_{Dq} = 1.4A Variants 04 to 06: I_{Dq} = 0.72A	Note 4	-	dBm
13	Power Added Efficiency @ 1dB Gain Compression	PAE	4(b)	V_{DS} = 9.0V, f = 2.3GHz (Notes 2, 3) Variants 01 to 03: I_{Dq} = 1.4A Variants 01, 02 Variant 03 Variants 04 to 06: I_{Dq} = 0.72A Variants 04, 05 Variant 06	 45 40 45 40	 - - - 	%
14	Gate-Source Quiescent Voltage	V_{GSq}	4(b)	V_{DS} = 9.0V, f = 2.3GHz Variants 01 to 03: I_{Dq} = 1.4A Variants 04 to 06: I_{Dq} = 0.72A	Note 5		V
15	D.C. Gate Current @ 1dB Gain Compression	I_{G-1dB}	4(b)	V_{DS} = 9.0V (Notes 2, 3), f = 2.3GHz Variants 01 to 03: I_{Dq} = 1.4A Variants 04 to 06: I_{Dq} = 0.72A	Note 5		V
16	D.C. Drain Current @ 1dB Gain Compression	I_{D-1dB}	4(b)	V_{DS} = 9.0V (Notes 2, 3), f = 2.3GHz Variants 01 to 03: I_{Dq} = 1.4A Variants 04 to 06: I_{Dq} = 0.72A	Note 5		V

NOTES

1. Pulsed measurements, time < 100msec. This condition shall be used only for the purpose of device characterisation, not for device operation.
2. Input and output matched for maximum P_{-1dB}.
3. P_{in} adjusted to result in $G_p = G_{lp}$-1dB.
4. See Column 5 of Table 1(a).
5. No specific limits applicable. The parameters are read and record for information only.

TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH TEMPERATURE

No.	CHARACTERISTICS	SYMBOL	TEST FIG.	TEST CONDITIONS	LIMITS		UNIT
					MIN.	MAX.	
3	Drain Leakage Current at Pinch-off 2	I_{Dp2}	4(a)	V_{DS} = 12V, V_{GS} = -4.0V Variants 01 to 03 Variants 04 to 06	 - -	 2.4 1.2	mA
4	Gate Leakage Current at Pinch-off 2	I_{Gp2}	4(a)	V_{DS} = 12V, V_{GS} = -4.0V Variants 01 to 03 Variants 04 to 06	 - -	 -2.4 -1.2	mA
5	Drain Leakage Current at Pinch-off 3	I_{Dp3}	4(a)	V_{DS} = 3.0V, V_{GS} = -3.8V Variants 01 to 03 Variants 04 to 06	 - -	 0.48 0.24	mA
6	Gate Leakage Current at Pinch-off 3	I_{Gp3}	4(a)	V_{DS} = 3.0V, V_{GS} = -3.8V Variants 01 to 03 Variants 04 to 06	 - -	 -0.24 -0.12	mA
8	Gate-Source Threshold Voltage	V_{GSth}	4(a)	V_{DS} = 2.0V, V_{GS} = 0V Variants 01 to 03 I_D = 160mA Variants 04 to 06 I_D = 80mA	-1.4	-3.8	V
9	Transconductance	g_m	4(a)	V_{DS} = 3.0V Variants 01 to 03 I_D = 720mA Variants 04 to 06 I_D = 720mA	 750 500	 - -	mS

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS

FIGURE 4(a) - TEST CIRCUIT FOR D.C. PARAMETERS

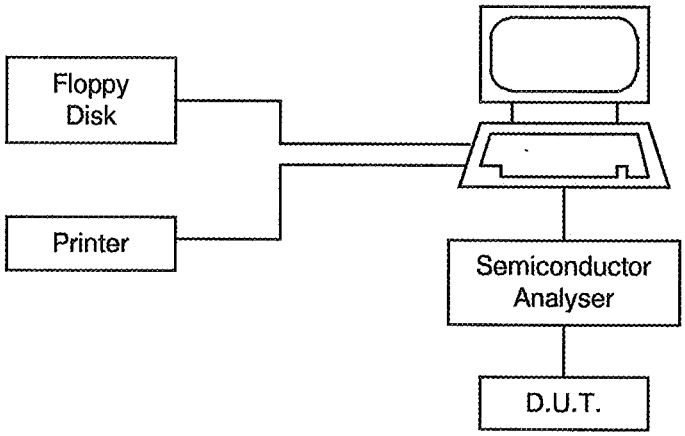
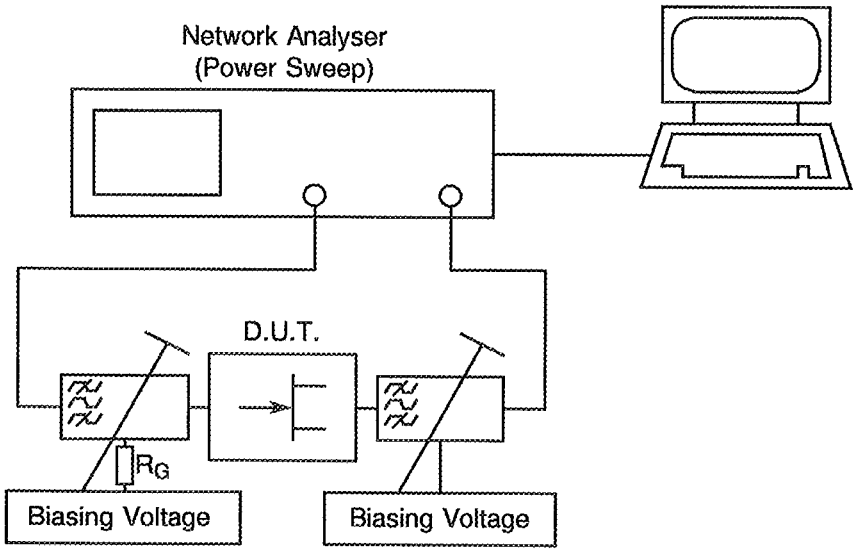


FIGURE 4(b) - TEST CIRCUIT FOR A.C. PARAMETERS



NOTES

1. D.C. Gate Resistance = 100Ω.

TABLE 4 - PARAMETER DRIFT VALUES

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	CHANGE LIMITS (Δ)	UNIT
5	Drain Leakage Current at Pinch-off 3	I_{Dp3}	As per Table 2	As per Table 2 Variants 01 to 03 Variants 04 to 06	 ±12 ±6.0	µA
6	Gate Leakage Current at Pinch-off 3	I_{Gp3}	As per Table 2	As per Table 2 Variants 01 to 03 Variants 04 to 06	 ±12 ±6.0	µA
7	Drain Saturation Current	I_{DSS}	As per Table 2	As per Table 2 Variants 01 to 03 Variants 04 to 06	 ±0.8 ±0.3	A
8	Gate-Source Threshold Voltage	V_{GSth}	As per Table 2	As per Table 2 Variants 01 to 03 Variants 04 to 06	±0.2	V
9	Transconductance	g_m	As per Table 2	As per Table 2 Variants 01 to 03 Variants 04 to 06	 ±140 ±70	mS
12	Output Power @ 1dB Gain Compression	P_{-1dB}	As per Table 2	As per Table 2	+0.5 -0.2	dBm

NOTES

1. $\Delta 1 = \Delta 2 = \Delta 3$.

TABLE 5(a) - CONDITIONS FOR HIGH TEMPERATURE REVERSE BIAS BURN-IN

No.	CHARACTERISTICS	SYMBOL	CONDITIONS	UNIT
1	Ambient Temperature	T_{amb}	+140 (+0-5)	°C
2	Gate Source Voltage	V_{GS}	-6.0 (+0.2 -0)	V
3	Drain Source Voltage	V_{DS}	10(+0 -0.2)	V

TABLE 5(b) - CONDITIONS FOR POWER BURN-IN AND OPERATING LIFE TESTS

No.	CHARACTERISTICS	SYMBOL	CONDITIONS	UNIT
1	Ambient Temperature	T_{amb}	+80 (Note 1)	°C
2	Channel Temperature	T_{ch}	+175 (+0 -5)	°C
3	Drain Source Voltage	V_{DS}	9.0 (+0 -0.2)	V
4	Drain Current	I_D	Variants 01 to 03: 700 Variants 04 to 06: 550 (±10%, Note 2)	mA

NOTES

Because the components are mechanically clamped to the burn-in fixture, an additional thermal resistance case to heatsink, e.g. $R_{TH(C-HS)} = 7.5°C/W$ must be considered for the calculation of T_{Ch}. Furthermore, the heatsink temperature will rise above the ambient (oven) temperature, characterised e.g. by a further $R_{TH(HS-A)} = 3°C/W$ per component.

1. T_{amb} shall be adjusted to provide the required T_{ch}.
2. The limits given for T_{ch} shall not be exceeded.

FIGURE 5 - ELECTRICAL CIRCUIT FOR BURN-IN

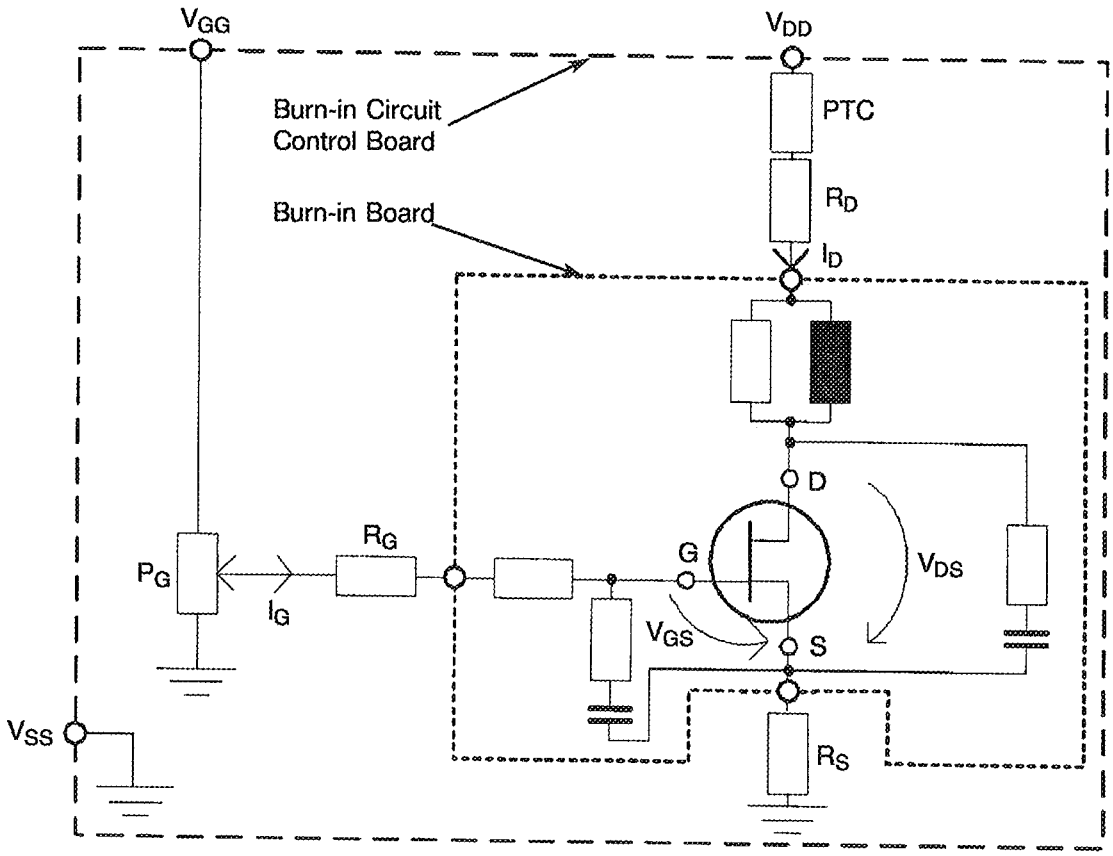
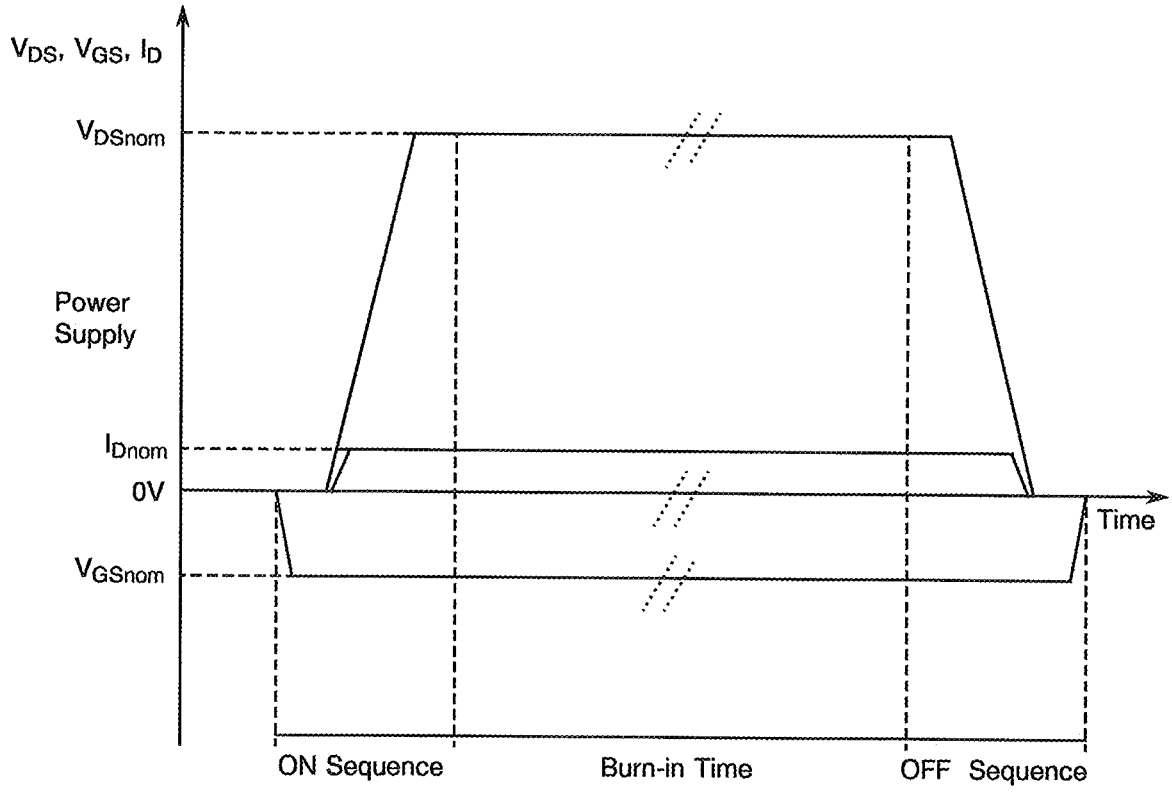
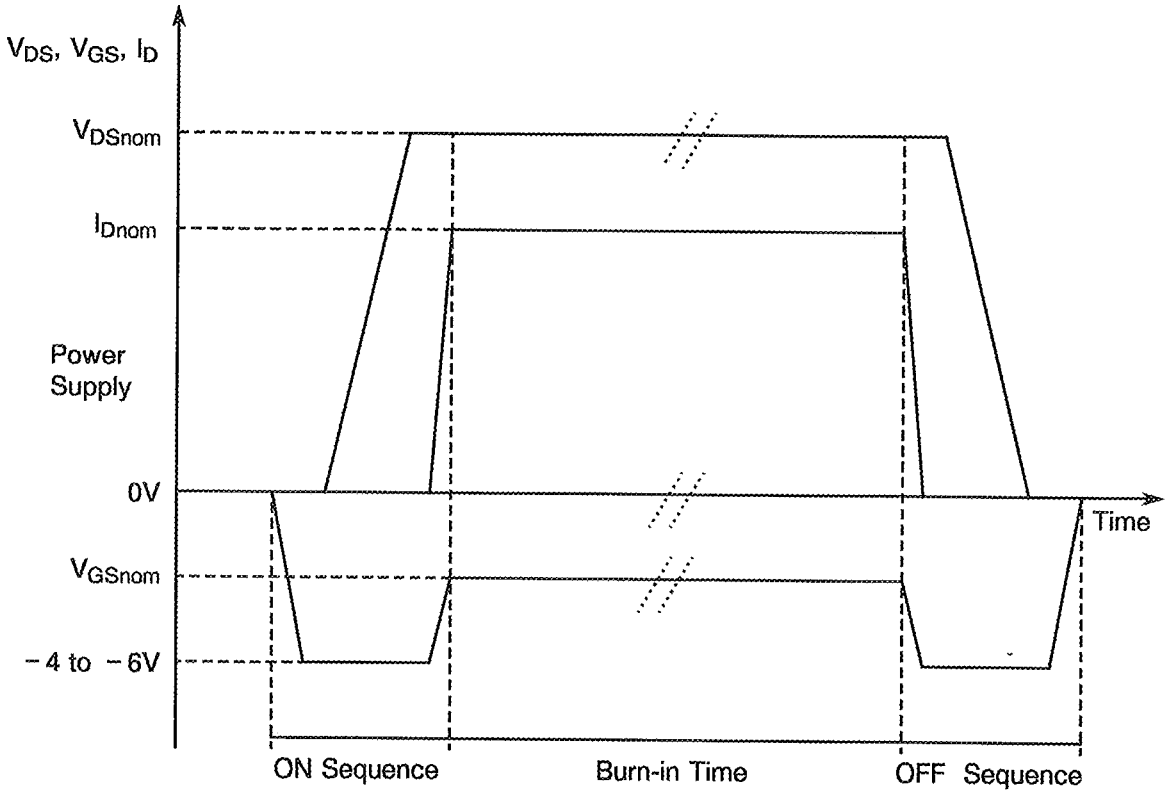


FIGURE 5 - ELECTRICAL CIRCUIT FOR BURN-IN (CONTINUED)



TIMING SEQUENCE FOR HTRB ON/OFF BIASING



TIMING SEQUENCE FOR POWER BURN-IN ON/OFF BIASING

4.8 ENVIRONMENTAL AND ENDURANCE TESTS (CHARTS IV AND V OF ESA/SCC GENERIC SPECIFICATION No. 5010)

4.8.1 Electrical Measurements on Completion of Environmental Tests

The parameters to be measured on completion of environmental tests are scheduled in Table 2. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +25 \pm 3$ °C.

4.8.2 Electrical Measurements at Intermediate Points and on Completion of Endurance Tests

The parameters to be measured at intermediate points and on completion of endurance testing are as scheduled in Table 6 of this specification. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +25 \pm 3$ °C.

4.8.3 Conditions for Operating Life Tests (Part of Endurance Testing)

The requirements for operating life testing are specified in Section 9 of ESA/SCC Generic Specification No. 5010. The conditions for operating life testing shall be as specified in Table 5(b) of this specification for Power burn-in.

4.8.4 Electrical Circuits for Operating Life Tests

The circuit for use in performing the operating life test shall be the same as shown in Figure 5 of this specification for power burn-in.

4.9 TOTAL DOSE IRRADIATION TESTING

Not applicable.

4.10 SPECIAL TESTING

Not applicable.

TABLE 6 - ELECTRICAL MEASUREMENTS AT INTERMEDIATE POINTS AND ON COMPLETION OF ENDURANCE TESTING

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	CHANGE LIMITS (Δ)	LIMITS		UNIT
						MIN.	MAX.	
5	Drain Leakage Current at Pinch-off 3	I_{Dp3}	As per Table 2	As per Table 2 Variants 01 to 03 Variants 04 to 06	 ±12 ±6.0	 - -	 30 15	µA
6	Gate Leakage Current at Pinch-off 3	I_{Gp3}	As per Table 2	As per Table 2 Variants 01 to 03 Variants 04 to 06	 ±12 ±6.0	 - -	 30 15	µA
7	Drain Saturation Current	I_{DSS}	As per Table 2	As per Table 2 Variants 01 to 03 Variants 04 to 06	 ±0.6 ±0.2	 2.2 1.1	 5.6 3.0	A
8	Gate-Source Threshold Voltage	V_{GSth}	As per Table 2	As per Table 2	±0.2	-1.5	-3.7	V
9	Transconductance	g_m	As per Table 2	As per Table 2 Variants 01 to 03 Variants 04 to 06	 ±140 ±70	 840 570	 - -	mS
12	Output Power @ 1dB Gain Compression	P_{-1dB}	As per Table 2	As per Table 2	±0.3	Note 1	-	dBm

NOTES:
1. As per Table 2, reduced by 0.2dB.

FIGURE 6 - BIAS CONDITIONS FOR IRRADIATION TESTING

Not applicable.

TABLE 7 - ELECTRICAL MEASUREMENTS DURING AND ON COMPLETION OF IRRADIATION TESTING

Not applicable.

APPENDIX 'A'

AGREED DEVIATIONS FOR INFINEON TECHNOLOGIES (D)

ITEMS AFFECTED	DESCRIPTION OF DEVIATIONS
Para 4.2.1	Paras. 5.2.4 and 10.5: If Wafer Lot Acceptance Test Data is specified in the purchase order, such data will not be delivered but will be available for review at Infineon Technologies.
Para. 4.2.2	Para. 9.11, Dimension Check: May be performed on a 100% basis using a gauge during RF Measurements.
Para. 4.2.3	Para. 9.12, Radiographic Inspection: May be replaced by a Visual Inspection for verifying the length, height and shape of the wire bonding. Paras. 9.21, HTRB and 9.22, Power Burn-in: The Infineon proprietary Burn-in circuit which provides closed loop feedback of I_D to V_{GS} may be used to replace Figure 5.
Para. 4.2.4	Para. 9.20.1, Operating Life During Qualification Testing: The Infineon proprietary Burn-in circuit which provides closed loop feedback of I_D to V_{GS} may be used to replace Figure 5.
Para. 4.2.5	Para. 9.20.2, Operating Life During Lot Acceptance Tests: The Infineon proprietary Burn-in circuit which provides closed loop feedback of I_D to V_{GS} may be used to replace Figure 5.