

Page i

TRANSISTORS, FIELD-EFFECT, N-CHANNEL, BASED ON TYPES 2N4391/4392/4393 ESCC Detail Specification No. 5205/003

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ESCC Detail Specification

PAGE	ii
ISSUE	1

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Pages 1 to 19

TRANSISTORS, FIELD-EFFECT, N-CHANNEL, BASED ON TYPES 2N4391/4392/4393 ESA/SCC Detail Specification No. 5205/003



space components coordination group

Date		
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March 1979		-
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Rev. 'B'

PAGE 2

ISSUE 2

DOCUMENTATION CHANGE NOTICE

Rev. Letter	Rev. Date	CHANGE Reference Item	Approved DCR No.
'A'	Jul. '88	This Issue incorporates all modifications agreed on the basis of Policy DCR 21016 for adaptation to new qualification requirements P1. Cover page P2. DCN P4. Table of Contents: Reference to Appendices added P6. Table 1(a): Lead Material and Finish added P9. Para. 2: MIL-STD-1276 deleted Para. 4.1: Reference to Appendices added Para. 4.2: PIND Test and Condition added P10. Para. 4.4.2: Text rewritten	None None 21019 21025 21025 21019 22639 21025
'B'	Feb. '92	P1. Cover page P2. DCN P5. Para. 1.2 : Paragraph amended P9. Para. 2 : "ESA/SCC Basic Spec. No. 23500" added Para. 4.2.2 : PIND deviation deleted P16. Table 3 : Note deleted	None None 21021 21025 21043 21047
		This document has been transferred from hardcopy to electronic format. The content is unchanged but minor differences in presentation exist.	



PAGE 3

ISSUE 2

TABLE OF CONTENTS

1.	GENERAL	Page 5
1.1	Scope	5
1.2	Component Type Variants	5
1.3	Maximum Ratings	5
1.4	Parameter Derating Information	5
1.5	Physical Dimensions	5 5 5
1.6	Functional Diagram	5
2.	APPLICABLE DOCUMENTS	9
3.	TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS	9
4.	REQUIREMENTS	9
4.1	General	9
4.2	Deviations from Generic Specification	9
4.2.1	Deviations from Special In-process Controls	9
4.2.2	Deviations from Final Production Tests (Chart II)	9
4.2.3	Deviations from Burn-in and Electrical Measurements (Chart III)	9
4.2.4	Deviations from Qualification Tests (Chart IV)	9
4.2.5	Deviations from Lot Acceptance Tests (Chart V)	9
4.3	Mechanical Requirements	10
4.3.1	Dimension Check	10
4.3.2	Weight	10
4.3.3	Terminal Strength	10
4.4	Materials and Finishes	10
4.4.1	Case	10
4.4.2	Lead Material and Finish	10
4.5	Marking	11
4.5.1	General	11
4.5.2 4.5.3	Lead Identification	11
4.5.4	The SCC Component Number	11
4.5.4	Traceability Information Marking of Small Components	11 11



Rev. 'A'

PAGE 4

ISSUE 2

		<u>Page</u>
4.6	Electrical Measurements	12
4.6.1	Electrical Measurements at Room Temperature	12
4.6.2	Electrical Measurements at High and Low Temperatures	12
4.6.3	Circuits for Electrical Measurements	12
4.7	Burn-in Tests	12
4.7.1	Parameter Drift Values	12
4.7.2	Conditions for Burn-in	12
4.7.3	Electrical Circuits for Burn-in	12
4.8	Environmental and Endurance Tests	18
4.8.1	Electrical Measurements on Completion of Environmental Tests	18
4.8.2	Electrical Measurements at Intermediate Points and on Completion of Endurance Tests	18
4.8.3	Conditions for Operating Life Tests (Part of Endurance Testing)	18
4.8.4	Electrical Circuits for Operating Life Tests	18
4.8.5	Conditions for High Temperature Storage Test (Part of Endurance Testing)	18
TABLE	<u>:s</u>	
1(a)	Type Variants	6
1(b)	Maximum Ratings	6
2	Electrical Measurements at Room Temperature	13
3	Electrical Measurements at High and Low Temperatures	16
4	Parameter Drift Values	16
5	Conditions for Burn-in	17
6	Electrical Measurements at Intermediate Points and on Completion of Endurance Testing	19
FIGUE	<u>RES</u>	
1	Parameter Derating Information	7
2	Physical Dimensions	8
3	Functional Diagram	8
4	Test Circuit	15
5	Electrical Circuits for Burn-in	17

APPENDICES (Applicable to specific Manufacturers only)

None.



Rev. 'B'

PAGE 5

ISSUE 2

1. **GENERAL**

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics, test and inspection data for Transistors, Field-Effect, N-Channel based on Types 2N4391, 2N4392 and 2N4393.

It shall be read in conjunction with ESA/SCC Generic Specification No. 5000, the requirements of which are supplemented herein.

1.2 COMPONENT TYPE VARIANTS

See Table 1(a).

1.3 MAXIMUM RATINGS

The maximum ratings, which shall not be exceeded at any time during use or storage, applicable to the transistors specified herein, are scheduled in Table 1(b).

1.4 PARAMETER DERATING INFORMATION

The applicable derating information for the transistors specified herein is shown in Figure 1.

1.5 PHYSICAL DIMENSIONS

The physical dimensions of the transistors specified herein are shown in Figure 2.

1.6 <u>FUNCTIONAL DIAGRAM</u>

The functional diagram, showing lead identification of the transistors specified herein, is shown in Figure 3.



Rev. 'A'

PAGE 6

ISSUE 2

TABLE 1(a) - TYPE VARIANTS

VARIANT	BASED ON TYPE	CHARACTERISTICS	LEAD MATERIAL AND FINISH
01	2N4391		D2
02	2N4392	See Table 2	D2
03	2N4393		D2

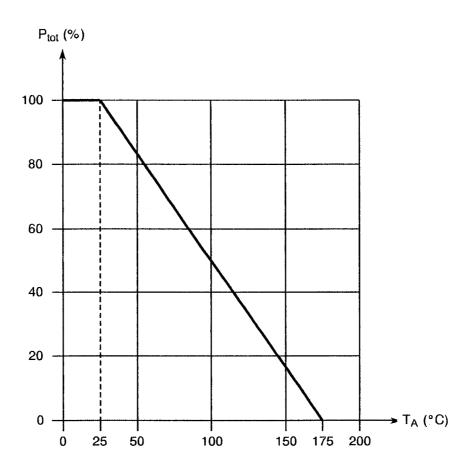
TABLE 1(b) - MAXIMUM RATINGS

No.	CHARACTERISTICS	SYMBOL	MAXIMUM RATINGS	UNIT	REMARKS
1	Drain Source Voltage	V_{DS}	40	V	
2	Gate Source Voltage	V_{GS}	- 40	V	
3	Gate Drain Voltage	V_{GD}	- 40	V	
4	Gate Current	l _G	50	mA	
5	Total Power Dissipation (see Figure 1)	P _{tot}	300	mW	T _{amb} = 25°C
6	Operating Temperature Range	T _{op}	-55 to +175	°C	T _{amb}
7	Storage Temperature Range	T _{stg}	-65 to +200	°C	
8	Soldering Temperature	T _{sol}	+ 235	°C	t ≤10 sec. Distance to case: ≥1.5mm

PAGE

ISSUE 2

FIGURE 1 - PARAMETER DERATING INFORMATION



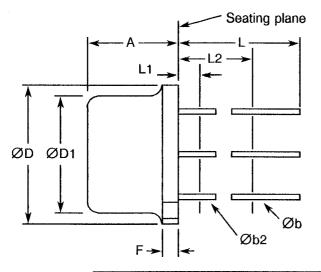
Power Dissipation versus Temperature

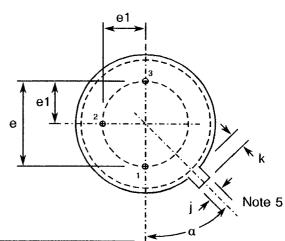


PAGE

ISSUE 2

FIGURE 2 - PHYSICAL DIMENSIONS



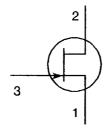


SYMBOL	INC	HES	MILLIM	ETRES	NOTES
STIVIDOL	MIN.	MAX.	MIN.	MAX.	NOTES
Α	0.170	0.210	4.32	5.33	
Øb	0.016	0.021	0.406	0.533	1
Øb2	0.016	0.019	0.406	0.483	1
ØD	0.209	0.230	5.31	5.84	
ØD1	0.178	0.195	4.52	4.95	
е	0.100 T.P.		2.54 T.P.		2, 4
e1	0.050	T.P.	1.27 T.P.		2, 4
F	-	0.030	-	0.762	
j	0.036	0.046	0.914	1.17	4
k	0.028	0.048	0.711	1.22	3
L	0.500	-	12.70	-	1
L1	-	0.050	-	1.27	1
L2	0.250	-	6.35	-	1
α	45°	T.P.	45°	T.P.	5

NOTES

- 1. (3 leads) Øb2 applies between L1 and L2. Øb applies between L2 and 0.5 inch (12.70mm) from seating plane. Diameter is uncontrolled in L1 and beyond 0.5 inch (12.70mm) from seating plane.
- 2. Leads having maximum diameter 0.019 inch (0.483mm) measured in gauging plane 0.054 inch (1.37mm) + 0.001 inch (0.025mm) 0.000 inch (0.000mm) below the seating plane of the device shall be within 0.007 inch (0.178mm) of their true positions relative to a maximum-width tab.
- 3. Measured from maximum diameter of the actual device.
- 4. The device may be measured by direct methods or by the gauge and gauging procedure described on gauge drawing GS-2.
- 5. Tab centreline.

FIGURE 3 - FUNCTIONAL DIAGRAM



- 1. Source.
- 2. Drain.
- 3. Gate (connected to case).



Rev. 'B'

PAGE 9

ISSUE 2

2. APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:-

- (a) ESA/SCC Generic Specification No. 5000 for Discrete Semiconductor Components.
- (b) MIL-STD-750, Test Methods and Procedures for Semiconductor Devices.
- (c) ESA/SCC Basic Specification No. 23500, Requirements for Lead Materials and Finishes for Components for Space Application.

3. TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESA/SCC Basic Specification No. 21300 shall apply.

4. **REQUIREMENTS**

4.1 GENERAL

The complete requirements for procurement of the transistors specified herein shall be as stated in this specification and ESA/SCC Generic Specification No. 5000 for Discrete Semiconductors. Deviations from the Generic Specification, applicable to this specification only, are listed in Para, 4.2.

Deviations from the applicable Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESA/SCC requirements and do not affect the components' reliability, are listed in the appendices attached to this specification.

4.2 DEVIATIONS FROM GENERIC SPECIFICATION

4.2.1 <u>Deviations from Special In-process Controls</u>

None.

4.2.2 <u>Deviations from Final Production Tests (Chart II)</u>

None.

4.2.3 Deviations from Burn-in and Electrical Measurements (Chart III)

High Temperature Reverse Bias Test (H.T.R.B.) is not required.

4.2.4 Deviations from Qualification Tests (Chart IV)

None.

4.2.5 Deviations from Lot Acceptance Tests (Chart V)

None.



Rev. 'A'

PAGE 10

ISSUE 2

4.3 <u>MECHANICAL REQUIREMENTS</u>

4.3.1 Dimension Check

The dimensions of the transistors specified herein shall be checked. They shall conform to those shown in Figure 2.

4.3.2 Weight

The maximum weight of the transistors specified herein shall be 0.9 grammes.

4.3.3 <u>Terminal Strength</u>

The requirements for terminal strength testing are specified in Section 9 of ESA/SCC Generic Specification No. 5000. The test conditions shall be as follows:-

Test Condition:

'A', Tension.

Applied Force:

5.0 Newtons.

Duration:

10 seconds.

4.4 MATERIALS AND FINISHES

The materials and finishes shall be as specified herein. Where a definite material is not specified, a material which will enable the transistors specified herein to meet the performance requirements of this specification shall be used. Acceptance or approval of any constituent material does not guarantee acceptance of the finished product.

4.4.1 <u>Case</u>

Metal case, hermetically sealed, similar to JEDEC TO-18.

4.4.2 Lead Material and Finish

The lead material shall be Type 'D' with Type '2' finish in accordance with the requirements of ESA/SCC Basic Specification No. 23500.



PAGE 11

ISSUE 2

4.5 MARKING

4.5.1 General

The marking of all components delivered to this specification shall be in accordance with the requirements of ESA/SCC Basic Specification No. 21700. Each component shall be marked in respect of:-

- (a) Lead Identification.
- (b) The SCC Component Number.
- (c) Traceability Information.

4.5.2 Lead Identification

Lead identification shall be as shown in Figures 2 and 3.

4.5.3 The SCC Component Number

Each component shall bear the SCC Component Number which shall be constituted and marked as follows:

	<u>520500301B</u>
Detail Specification Number	
Type Variant ——————	
Testing Level (B or C, as applicable)	***************************************

4.5.4 Traceability Information

Each component shall be marked in respect of traceability information in accordance with the requirements of ESA/SCC Basic Specification No. 21700.

4.5.5 Marking of Small Components

When it is considered that the component is too small to accommodate the marking as specified above, as much as space permits shall be marked. The order of precedence shall be as follows:-

- (a) Lead Identification.
- (b) The SCC Component Number.
- (c) Traceability Information.

The marking information in full shall accompany each component in its primary package.



PAGE 12

ISSUE 2

4.6 <u>ELECTRICAL MEASUREMENTS</u>

4.6.1 Electrical Measurements at Room Temperature

The parameters to be measured at room temperature are scheduled in Table 2. The measurements shall be performed at T_{amb} = +22 ±3 °C.

4.6.2 Electrical Measurements at High and Low Temperatures

The parameters to be measured at high and low temperatures are scheduled in Table 3.

4.6.3 <u>Circuits for Electrical Measurements</u>

Circuits for use in performing the electrical measurements listed in Tables 2 and 3 are shown in Figure 4.

4.7 BURN-IN TESTS

4.7.1 Parameter Drift Values

The parameter drift values applicable to burn-in are specified in Table 4 of this specification. Unless otherwise stated, measurements shall be performed at T_{amb} = +22 ±3 °C. The parameter drift values (Δ) applicable to the parameters scheduled, shall not be exceeded. In addition to these drift value requirements, the appropriate limit value specified for a given parameter in Table 2 shall not be exceeded.

4.7.2 Conditions for Burn-in

The requirements for burn-in are specified in Section 7 of ESA/SCC Generic Specification No. 5000. The conditions for burn-in shall be as specified in Table 5 of this specification.

4.7.3 <u>Electrical Circuits for Burn-in</u>

Circuits for use in performing the burn-in tests are shown in Figure 5 of this specification.



PAGE 13

ISSUE 2

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS

No	CHARACTERISTICS	SYMBOL	SPEC. AND/OR	TEST	LIM	ITS	UNIT
No.	CHARACTERISTICS	STIVIBUL	TEST METHOD	CONDITIONS	MIN.	MAX.	UNIT
1	Total Gate Leakage Current	lgss	MIL-STD-750 Method 3411	V _{DS} = 0V V _{GS} = -20V	•	- 0.1	nA
2	Gate Source Breakdown Voltage	V _{(BR)GSS}	MIL-STD-750 Method 3401	V _{DS} = 0 I _G = -1.0μA	- 40	-	٧
3	Drain Cut-off Current - Variant 01 - Variant 02 - Variant 03	I _{DSX}	MIL-STD-750 Method 3413	$V_{DS} = 20V$ $V_{GS} = -12V$ $V_{GS} = -7.0V$ $V_{GS} = -5.0V$	-	0.1	nA
4	Drain Current - Variant 01 - Variant 02 - Variant 03	lpss	MIL-STD-750 Method 3413	V _{DS} = 20V V _{GS} = 0V Note 1	50 25 5.0	150 75 30	mA
5	Gate Source Cut-off Voltage - Variant 01 - Variant 02 - Variant 03	V _{GSoff}	MIL-STD-750 Method 3403	V _{DS} = 20V I _D = 1.0nA	- 4.0 - 2.0 - 0.5	- 10 - 5.0 - 3.0	٧
6	Drain Source Saturation Voltage - Variant 01 - Variant 02 - Variant 03	V _{Dsat}	MIL-STD-750 Method 3405	$V_{GS} = 0V$ $I_D = 12mA$ $I_D = 6.0mA$ $I_D = 3.0mA$	-	0.4	V
7	ON-State Drain Source Resistance - Variant 01 - Variant 02 - Variant 03	^r DSon	MIL-STD-750 Method 3421	V _{GS} = 0V I _D = 1.0mA	- - -	30 60 100	Ω

NOTES

1. Pulse measurement: Pulse length ≤300μs, Duty Cycle ≤2%.



PAGE 14

ISSUE 2

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS

No	CHARACTERISTICS	SYMBOL	SPEC. AND/OR	TEST	LIM	IITS	LINIT
No.	CHARACTERISTICS	STINIBOL	TEST METHOD	CONDITIONS	MIN.	MAX.	UNIT
8	ON-State Drain Source Resistance - Variant 01 - Variant 02 - Variant 03	^r DSon	MIL-STD-750 Method 3423	V _{GS} = 0V I _D = 0A f = 1.0kHz	- - -	30 60 100	Ω
9	Input Capacitance	C _{iss}	MIL-STD-750 Method 3431	$V_{GS} = 0V$ $V_{DS} = 0V$ f = 1.0MHz	-	26	pF
10	Reverse Transfer Capacitance - Variant 01 - Variant 02 - Variant 03	C _{rss}	MIL-STD-750 Method 3433	$V_{DS} = 0V \\ f = 1.0MHz \\ V_{GS} = -12V \\ V_{GS} = -7.0V \\ V_{GS} = -5.0V$	-	4.0	pF
11	Rise Time - Variant 01 - Variant 02 - Variant 03	t _r	See Figure 4	$\begin{split} &V_{DD} = 10V \\ &V_{GS} = 0V \\ &V_{GSX} = -12V \\ &I_{D} = 12\text{mA} \\ &V_{GSX} = -7.0V \\ &I_{D} = 6.0\text{mA} \\ &V_{GSX} = -5.0V \\ &I_{D} = 3.0\text{mA} \end{split}$	-	5.0	ns
12	Turn-on Delay Time - Variant 01 - Variant 02 - Variant 03	t _{d(on)}	See Figure 4	$V_{DD} = 10V$ $V_{GS} = 0V$ $V_{GSX} = -12V$ $I_D = 12mA$ $V_{GSX} = -7.0V$ $I_D = 6.0mA$ $V_{GSX} = -5.0V$ $I_D = 3.0mA$	-	15	ns
13	Fall Time - Variant 01 - Variant 02 - Variant 03	t _f	See Figure 4	$V_{DD} = 10V \\ V_{GS} = 0V \\ V_{GSX} = -12V \\ I_{D} = 12mA \\ V_{GSX} = -7.0V \\ I_{D} = 6.0mA \\ V_{GSX} = -5.0V \\ I_{D} = 3.0mA$	- - -	15 20 30	ns
14	Turn-off Delay Time - Variant 01 - Variant 02 - Variant 03	^t d(off)	See Figure 4	$\begin{split} &V_{DD} = 10V \\ &V_{GS} = 0V \\ &V_{GSX} = -12V \\ &I_{D} = 12\text{mA} \\ &V_{GSX} = -7.0V \\ &I_{D} = 6.0\text{mA} \\ &V_{GSX} = -5.0V \\ &I_{D} = 3.0\text{mA} \end{split}$	- - -	20 35 50	ns

NOTES

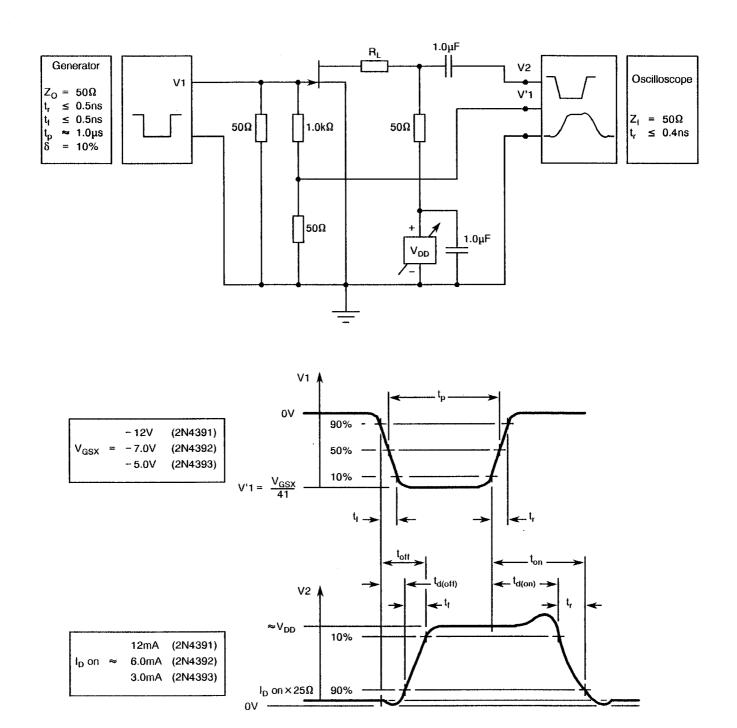
1. If more than 20 units have to be measured, the measurements shall be made on a sample basis in accordance with Para. 7.4.2 of ESA/SCC Generic Specification No. 5000. Inspection Level II with an AQL = 2.5%.



PAGE 15

ISSUE 2

FIGURE 4 - SWITCHING TIMES TEST CIRCUIT





Rev. 'B'

PAGE 16

ISSUE 2

TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES

No	No. CHARACTERISTICS	CHARACTERISTICS SYMBOL SPEC. AND/OR	TEST	LIM	UNIT		
INO.	CHARACTERISTICS	STIVIBOL	TEST METHOD	CONDITIONS	MIN.	MAX.	UNIT
1	Total Gate Leakage Current	l _{GSS}	MIL-STD-750 Method 3411	V _{DS} = 0V V _{GS} = -20V T _{amb} = +150°C	**	-0.2	μА
2	Drain Cut-off Current - Variant 01 - Variant 02 - Variant 03	I _{DSX}	MIL-STD-750 Method 3413	$V_{DS} = 20V$ $T_{amb} = +150$ °C $V_{GS} = -12V$ $V_{GS} = -7.0V$ $V_{GS} = -5.0V$	-	0.2	μА

TABLE 4 - PARAMETER DRIFT VALUES

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	CHANGE LIMITS (Δ)	UNIT
1	Total Gate Leakage Current	l _{GSS}	MIL-STD-750 Method 3411	V _{DS} = 0V V _{GS} = -20V	± 100 or (2) ± 50	% pA
2	Gate Source Cut-off Voltage	V _{GSoff}	MIL-STD-750 Method 3403	V _{DS} = 20V I _D = 1.0nA	± 10	%
3	Drain Current	loss	MIL-STD-750 Method 3413	V _{DS} = 20V V _{GS} = 0V Note 1	±15	%

NOTES

- 1. Pulse measurement: Pulse length ≤300μs, Duty Cycle ≤2%
- 2. Whichever is greater.



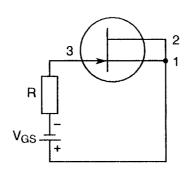
PAGE 17

ISSUE 2

TABLE 5 - CONDITIONS FOR BURN-IN

No.	CHARACTERISTICS	SYMBOL	CONDITION	UNIT
1	Ambient Temperature	T _{amb}	150	°C
2	Drain Source Voltage	V _{DS}	0	V
3	Gate Source Voltage	V_{GS}	- 28	V

FIGURE 5 - ELECTRICAL CIRCUITS FOR BURN-IN





PAGE 18

ISSUE 2

4.8 <u>ENVIRONMENTAL AND ENDURANCE TESTS (CHARTS IV AND V OF ESA/SCC GENERIC SPECIFICATION No. 5000)</u>

4.8.1 Electrical Measurements on Completion of Environmental Tests

The parameters to be measured on completion of environmental tests are scheduled in Table 2. The measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.8.2 <u>Electrical Measurements at Intermediate Points and on Completion of Endurance Tests</u>

The parameters to be measured at intermediate points and on completion of endurance tests are scheduled in Table 6.

4.8.3 Conditions for Operating Life Tests (Part of Endurance Testing)

The requirements for operating life testing are specified in Section 9 of ESA/SCC Generic Specification No. 5000. The conditions for operating life testing shall be as specified in Table 5 for the burn-in test.

4.8.4 Electrical Circuits for Operating Life Tests

The circuit to be used for performance of the operating life tests shall be as shown in Figure 5 for burn-in.

4.8.5 Conditions for High Temperature Storage Test (Part of Endurance Testing)

The requirements for the high temperature storage test are specified in ESA/SCC Generic Specification No. 5000. The temperature to be applied shall be the maximum storage temperature specified in Table 1(b) of this specification.



PAGE 19

ISSUE 2

TABLE 6 - ELECTRICAL MEASUREMENTS AT INTERMEDIATE POINTS AND ON COMPLETION OF ENDURANCE TESTING

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	LIMITS		UNIT
					MIN.	MAX.	UNIT
1	Total Gate Leakage Current	lgss	MIL-STD-750 Method 3411	V _{DS} = 0V V _{GS} = -20V	-	- 0.1	nA
2	Gate Source Cut-off Voltage - Variant 01 - Variant 02 - Variant 03	V _{GSoff}	MIL-STD-750 Method 3403	V _{DS} = 20V I _D = 1.0nA	- 4.0 - 2.0 - 0.5	- 10 - 5.0 - 3.0	V
3	Drain Current - Variant 01 - Variant 02 - Variant 03	l _{DSS}	MIL-STD-750 Method 3413	V _{DS} = 20V V _{GS} = 0V Note 1	50 25 5.0	150 75 30	mA

NOTES

1. Pulse measurement: Pulse length ≤300µs, Duty Cycle ≤2%