



**TRANSISTORS, FIELD-EFFECT, N-CHANNEL,  
BASED ON TYPES 2N4416 AND 2N4416A  
ESCC Detail Specification No. 5205/004**

**ISSUE 1  
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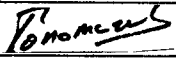
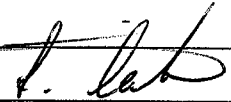
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**TRANSISTORS, FIELD-EFFECT, N-CHANNEL,  
BASED ON TYPES 2N4416 AND 2N4416A  
ESA/SCC Detail Specification No. 5205/004**



**space components  
coordination group**

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Issue 2	March 1979	-	-
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**DOCUMENTATION CHANGE NOTICE**

Rev. Letter	Rev. Date	Reference	CHANGE Item	Approved DCR No.
		This Issue incorporates all modifications agreed on the basis of Policy DCR 21016 for adaptation to new qualification requirements		
'A'	Mar. '89	P1.	Cover page	None
		P2.	DCN	None
		P4.	Table of Contents : Amended	None
		P9.	Para. 2(c) : Amended	22654
			Para. 2(d) : Amended	22654
			Para. 4.2.1 : Amended	22654
			Para. 4.2.2 : Amended	22654
			Para. 4.2.3 : Amended	22654
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		P12.	Para. 4.7.2 : Subtitle amended	22654
			Para. 4.7.3 : Subtitle amended	22654
		P13.	Table 2 : Typographic omission corrected	22654
		P14.	Table 2 : Alternative Test Methods added	22654
		P17.	Table 5 : Title amended	22654
			: Test Condition added	22654
			: Note added	22654
		P19.	Table 6 : Minimum Limit to Variant 02 added in Test 2	22654
			: Min. and Max. Limits added for Test 3	22654
'B'	Feb. '92	P1.	Cover page	None
		P2.	DCN	None
		P4.	Table of Contents : "Appendices" Title added	21019
		P5.	Para. 1.2 : Paragraph amended	21021
		P6.	Table 1(a) : "Lead Material and/or Finish" column added	21025
		P9.	Para. 4.1 : Additional text added	21019
			Para. 4.2.2 : PIND deviation deleted	21043
		P16.	Table 3 : Note deleted	21047
		This document has been transferred from hardcopy to electronic format. The content is unchanged but minor differences in presentation exist.		

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#### APPENDICES (Applicable to specific Manufacturers only)

None.

**1. GENERAL****1.1 SCOPE**

This specification details the ratings, physical and electrical characteristics, test and inspection data for Transistors, Field-Effect, N-Channel based on Types 2N4416 and 2N4416A.

It shall be read in conjunction with ESA/SCC Generic Specification No. 5000, the requirements of which are supplemented herein.

**1.2 COMPONENT TYPE VARIANTS**

See Table 1(a).

**1.3 MAXIMUM RATINGS**

The maximum ratings, which shall not be exceeded at any time during use or storage, applicable to the transistors specified herein, are scheduled in Table 1(b).

**1.4 PARAMETER DERATING INFORMATION**

The applicable derating information for the transistors specified herein is shown in Figure 1.

**1.5 PHYSICAL DIMENSIONS**

The physical dimensions of the transistors specified herein are shown in Figure 2.

**1.6 FUNCTIONAL DIAGRAM**

The functional diagram, showing lead identification of the transistors specified herein, is shown in Figure 3.

**TABLE 1(a) - TYPE VARIANTS**

VARIANT	BASED ON TYPE	CHARACTERISTICS	LEAD MATERIAL AND/OR FINISH
01	2N4416	See Table 2,	D2
02	2N4416A	Tests 2, 4, 8	D2

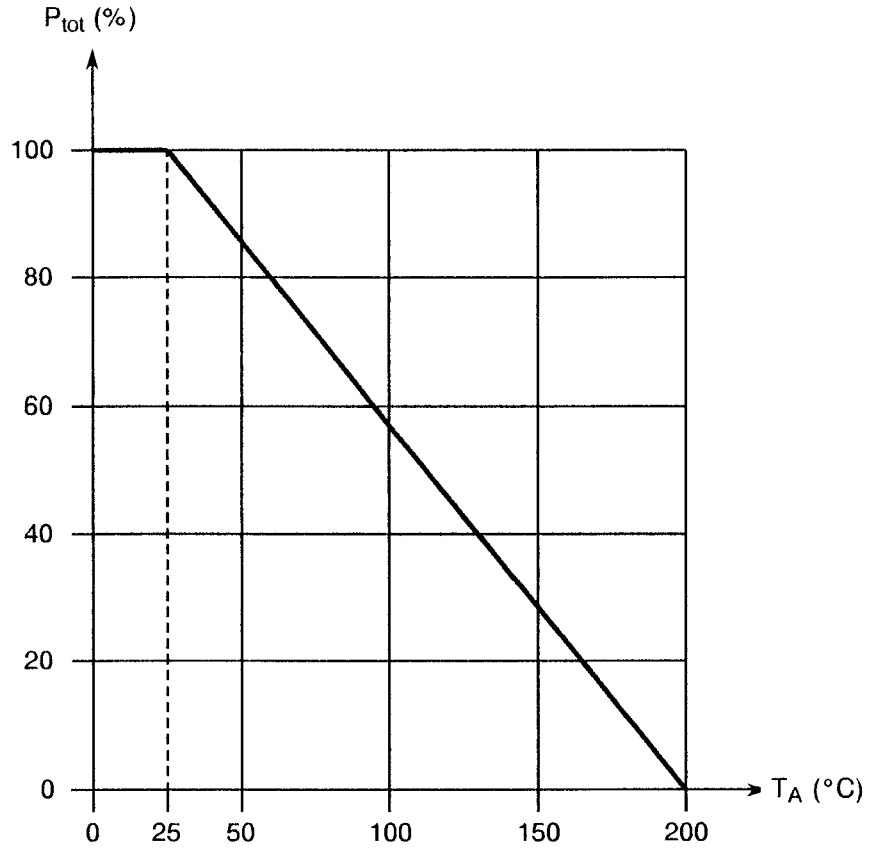
**TABLE 1(b) - MAXIMUM RATINGS**

No.	CHARACTERISTICS	SYMBOL	MAXIMUM RATINGS	UNIT	REMARKS
1	Drain Source Voltage	$V_{DS}$	30	V	
2	Gate Source Voltage - Variant 01 - Variant 02	$V_{GS}$	- 30 - 35	V	
3	Gate Drain Voltage	$V_{GD}$	- 30	V	
4	Gate Current	$I_G$	10	mA	
5	Total Power Dissipation (see Figure 1)	$P_{tot}$	300	mW	$T_{amb} = +25^{\circ}C$
6	Operating Temperature Range	$T_{op}$	- 55 to + 200	$^{\circ}C$	$T_{amb}$
7	Storage Temperature Range	$T_{stg}$	- 65 to + 200	$^{\circ}C$	
8	Soldering Temperature	$T_{sol}$	+ 235	$^{\circ}C$	$t \leq 10$ sec. Distance to case: $\geq 1.5$ mm





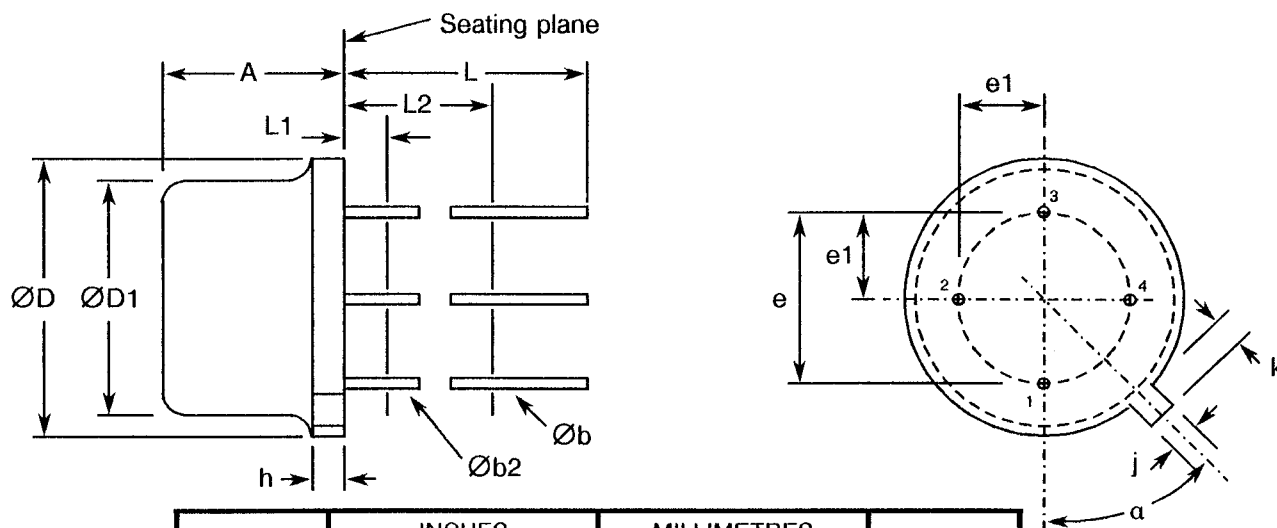
**FIGURE 1 - PARAMETER DERATING INFORMATION**



Power Dissipation versus Temperature



**FIGURE 2 - PHYSICAL DIMENSIONS**

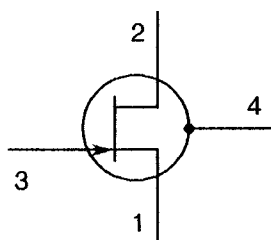


SYMBOL	INCHES		MILLIMETRES		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.170	0.210	4.32	5.33	
Øb	0.016	0.021	0.406	0.533	2
Øb2	0.016	0.019	0.406	0.483	2
ØD	0.209	0.230	5.31	5.84	
ØD1	0.178	0.195	4.52	4.95	
e	0.100 T.P.		2.54 T.P.		4
e1	0.050 T.P.		1.27 T.P.		4
h	-	0.030	-	0.762	
j	0.036	0.046	0.914	1.17	
k	0.028	0.048	0.711	1.22	3
L	0.500	-	12.70	-	2
L1	-	0.050	-	1.27	2
L2	0.250	-	6.35	-	2
a	45° T.P.		45° T.P.		4, 6



**NOTES**

- (4 leads) Maximum number of leads omitted in this outline, "none" (0). The number and position of leads actually present are indicated in the product registration. Outline designation determined by the location and minimum angular or linear spacing of any two adjacent leads.
- (All leads) Øb2 applies between L1 and L2. Øb applies between L2 and 0.5 inch (12.70mm) from seating plane. Diameter is uncontrolled in L1 and beyond 0.5 inch (12.70mm) from seating plane.
- Measured from maximum diameter of the product.
- Leads having maximum diameter 0.019 inch (0.483mm) measured in gauging plane 0.054 inch (1.37mm) + 0.001 inch (0.025mm) - 0.000 inch (0.000mm) below the seating plane of the product shall be within 0.007 inch (0.178mm) of their true positions relative to a maximum-width tab.
- The product may be measured by direct methods or by gauge.
- Tab centreline.

**FIGURE 3 - FUNCTIONAL DIAGRAM**



- Source.
- Drain.
- Gate.
- Connected to case.

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## 2. **APPLICABLE DOCUMENTS**

The following documents form part of this specification and shall be read in conjunction with it:-

- (a) ESA/SCC Generic Specification No. 5000 for Discrete Semiconductor Components.
- (b) MIL-STD-750, Test Methods and Procedures for Semiconductor Devices.
- (c) ESA/SCC Basic Specification No. 23500, Requirements for Lead Materials and Finishes for Components for Space Application.
- (d) ESA/SCC Basic Specification No. 21400, Scanning Electron Microscope Inspection.

## 3. **TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS**

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESA/SCC Basic Specification No. 21300 shall apply.

## 4. **REQUIREMENTS**

### 4.1 **GENERAL**

The complete requirements for procurement of the transistors specified herein shall be as stated in this specification and ESA/SCC Generic Specification No. 5000 for Discrete Semiconductors. Deviations from the Generic Specification, applicable to this specification only, are listed in Para. 4.2.

Deviations from the applicable Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESA/SCC requirements and do not affect the components' reliability, are listed in the appendices attached to this specification.

### 4.2 **DEVIATIONS FROM GENERIC SPECIFICATION**

#### 4.2.1 **Deviations from Special In-process Controls**

For Level B components a Scanning Electron Microscope Inspection shall be conducted in accordance with the requirements of ESA/SCC Basic Specification No. 21400.

#### 4.2.2 **Deviations from Final Production Tests (Chart II)**

None.

#### 4.2.3 **Deviations from Burn-in and Electrical Measurements (Chart III)**



Para. 7.1.1(b), Burn-in: Not applicable.

#### 4.2.4 **Deviations from Qualification Tests (Chart IV)**

None.

#### 4.2.5 **Deviations from Lot Acceptance Tests (Chart V)**

None.

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4.3 MECHANICAL REQUIREMENTS

4.3.1 Dimension Check

The dimensions of the transistors specified herein shall be checked. They shall conform to those shown in Figure 2.

4.3.2 Weight

The maximum weight of the transistors specified herein shall be 0.9 grammes.

4.3.3 Terminal Strength

The requirements for terminal strength testing are specified in Section 9 of ESA/SCC Generic Specification No. 5000. The test conditions shall be as follows:-

Test Condition: 'A', Tension.  
Applied Force: 5.0 Newtons.  
Duration: 10 seconds.

4.4 MATERIALS AND FINISHES

The materials and finishes shall be as specified herein. Where a definite material is not specified, a material which will enable the transistors specified herein to meet the performance requirements of this specification shall be used. Acceptance or approval of any constituent material does not guarantee acceptance of the finished product.

4.4.1 Case

Metal case, hermetically sealed, similar to JEDEC TO-72.

4.4.2 Lead Material and Finish

The lead material shall be Type 'D' with Type '2' finish in accordance with the requirements of ESA/SCC Basic Specification No. 23500.



4.5 MARKING

4.5.1 General

The marking of all components delivered to this specification shall be in accordance with the requirements of ESA/SCC Basic Specification No. 21700. Each component shall be marked in respect of:-

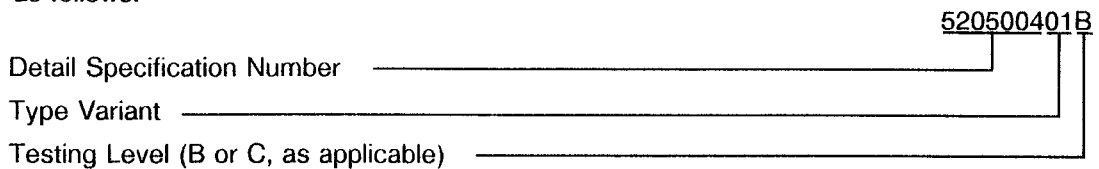
- (a) Lead Identification.
- (b) The SCC Component Number.
- (c) Traceability Information.

4.5.2 Lead Identification

Lead identification shall be as shown in Figures 2 and 3.

4.5.3 The SCC Component Number

Each component shall bear the SCC Component Number which shall be constituted and marked as follows:



4.5.4 Traceability Information


Each component shall be marked in respect of traceability information in accordance with the requirements of ESA/SCC Basic Specification No. 21700.

4.5.5 Marking of Small Components

When it is considered that the component is too small to accommodate the marking as specified above, as much as space permits shall be marked. The order of precedence shall be as follows:-

- (a) Lead Identification.
- (b) The SCC Component Number.
- (c) Traceability Information.

The marking information in full shall accompany each component in its primary package.

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#### 4.6 ELECTRICAL MEASUREMENTS

##### 4.6.1 Electrical Measurements at Room Temperature

The parameters to be measured at room temperature are scheduled in Table 2. The measurements shall be performed at  $T_{amb} = +22 \pm 3$  °C.

##### 4.6.2 Electrical Measurements at High and Low Temperatures

The parameters to be measured at high and low temperatures are scheduled in Table 3.

##### 4.6.3 Circuits for Electrical Measurements

Circuits for use in performing the electrical measurements listed in Tables 2 and 3 are shown in Figure 4.

#### 4.7 BURN-IN TESTS

##### 4.7.1 Parameter Drift Values

The parameter drift values applicable to burn-in are specified in Table 4 of this specification. Unless otherwise stated, measurements shall be performed at  $T_{amb} = +22 \pm 3$  °C. The parameter drift values ( $\Delta$ ) applicable to the parameters scheduled, shall not be exceeded. In addition to these drift value requirements, the appropriate limit value specified for a given parameter in Table 2 shall not be exceeded.

##### 4.7.2 Conditions for H.T.R.B. Burn-in

The requirements for burn-in are specified in Section 7 of ESA/SCC Generic Specification No. 5000. The conditions for burn-in shall be as specified in Table 5 of this specification.

##### 4.7.3 Electrical Circuits for H.T.R.B. Burn-in

Circuits for use in performing the burn-in tests are shown in Figure 5 of this specification.

**TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS**

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	LIMITS		UNIT
					MIN.	MAX.	
1	Total Gate Leakage Current	$I_{GSS}$	MIL-STD-750 Method 3411	$V_{DS} = 0V$ $V_{GS} = -20V$	-	-0.1	nA
2	Gate Source Breakdown Voltage - Variant 01 - Variant 02	$V_{(BR)GSS}$	MIL-STD-750 Method 3401	$V_{DS} = 0V$ $I_G = -1.0\mu A$	-30 -35	- -	V
3	Gate Source Voltage	$V_{GS}$	See Figure 4(b)	$V_{DS} = 0V$ $I_G = 1.0mA$	-	1.0	V
4	Gate Source Cut-off Voltage - Variant 01 - Variant 02	$V_{GSoff}$	MIL-STD-750 Method 3403	$V_{DS} = 15V$ $I_D = 1.0nA$	- -2.5	-6.0 -6.0	V
5	Drain Current	$I_{DSS}$	MIL-STD-750 Method 3413	$V_{DS} = 15V$ $V_{GS} = 0V$ Note 1	5.0	15	mA
6	Gate Source Voltage	$V_{GS}$	MIL-STD-750 Method 3403	$V_{DS} = 15V$ $I_D = 0.5mA$	-1.0	-5.5	V

**NOTES**

1. Pulse measurement: Pulse length  $\leq 300\mu s$ , Duty Cycle  $\leq 2\%$ .

**TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS**

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	LIMITS		UNIT
					MIN.	MAX.	
7	Input Capacitance	$C_{iss}$	MIL-STD-750 Method 3431	$V_{GS} = 15V$ $V_{DS} = 0V$ $f = 1.0MHz$	-	4.0	pF
8	Reverse Transfer Capacitance - Variant 01 - Variant 02	$C_{rss}$	MIL-STD-750 Method 3433	$V_{DS} = 15V$ $V_{GS} = 0V$ $f = 1.0MHz$	- -	0.9 0.8	pF
9	Modulus of Forward Transfer Admittance	$ Y_{21s} $	MIL-STD-750 Method 3455  or Method 3475	$V_{DS} = 15V, V_{GS} = 0V$ $f = 1.0kHz$  $V_{DS} = 15V, Pulse \leq 300\mu s$ $V_{GS} = 0V$ Duty Cycle $\leq 2\%$	4.5	7.5	ms
10	Modulus of Output Admittance	$ Y_{22s} $	MIL-STD-750 Method 3453  or Method 3475	$V_{DS} = 15V, V_{GS} = 0V$ $f = 1.0kHz$  $V_{DS} = 15V, Pulse \leq 300\mu s$ $V_{GS} = 0V$ Duty Cycle $\leq 2\%$	-	50	$\mu s$
11	Power Gain (Neutralised)	$G_p$	See Figure 4(a)	$V_{DS} = 15V$ $I_D = 5.0mA$ $f = 400MHz$	10	-	dB
12	Noise Factor	F	See Figure 4(a)	$V_{DS} = 15V$ $I_D = 5.0mA$ $R_G = 1.0$ $f = 400MHz$	-	4.0	dB

**NOTES**

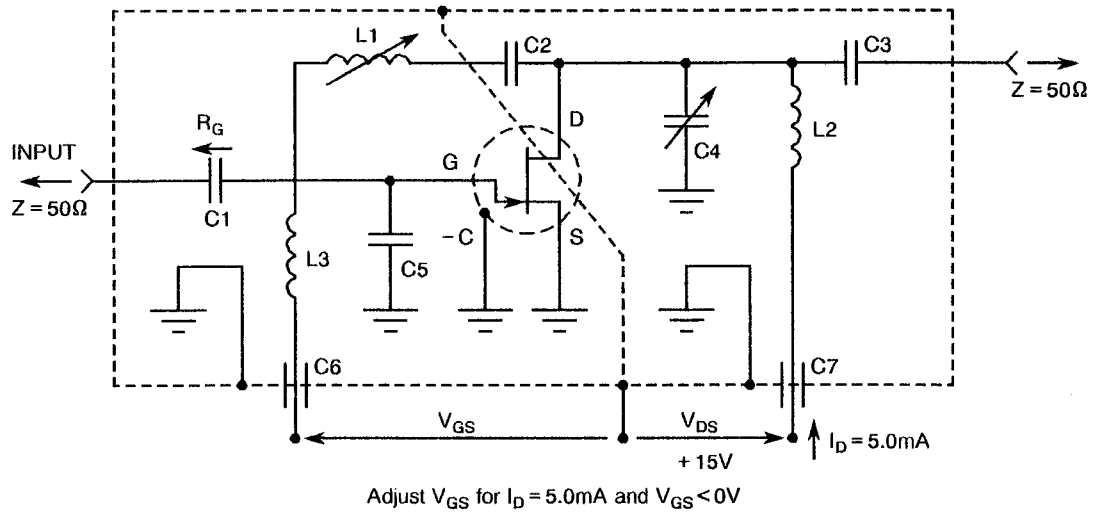
1. If more than 20 units have to be measured, the measurements shall be made on a sample basis in accordance with Para. 7.4.2 of ESA/SCC Generic Specification No. 5000. Inspection Level II with an AQL = 2.5%.





**FIGURE 4 - TEST CIRCUIT**

**FIGURE 4(a) - MEASUREMENT OF POWER GAIN AND NOISE FACTOR**

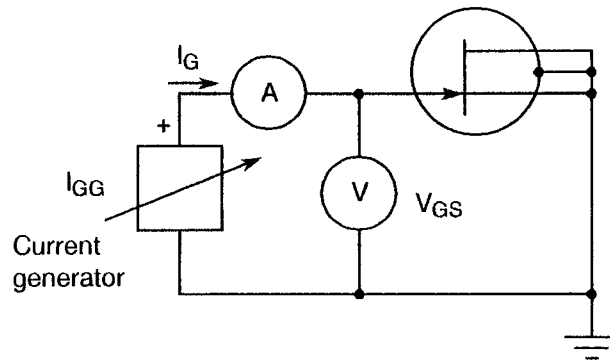


	$C_1$	$C_2$	$C_3$	$C_4$	$C_5$	$C_6$	$C_7$	$L_1$	$L_2$	$L_3$
400MHz	1.8pF	27pF	1.0pF	0.8 - 8 pF	0.8 - 8 pF	0.001μF	0.001μF	0.2μH	0.03μH	0.022μH

**400MHz power gain**

- $L_1$  - 6 turns = 24 enamelled copper wire, close wound on 7/32" ceramic coil form.
- $L_2$  - 1 turn = 16 enamelled copper wire, 3/8" I.D. (air core).
- $L_3$  - 1/2 turn = 16 enamelled copper wire, 1/4" I.D. (air core).

**FIGURE 4(b) - MEASUREMENT OF GATE SOURCE VOLTAGE**



**TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES**

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	LIMITS		UNIT
					MIN.	MAX.	
1	Total Gate Leakage Current	$I_{GSS}$	MIL-STD-750 Method 3411	$V_{DS} = 0V$ $V_{GS} = -20V$ $T_{amb} = +150^{\circ}C$	-	-0.2	$\mu A$

**TABLE 4 - PARAMETER DRIFT VALUES**

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	CHANGE LIMITS ( $\Delta$ )	UNIT
1	Total Gate Leakage Current	$I_{GSS}$	MIL-STD-750 Method 3411	$V_{DS} = 0V$ $V_{GS} = -20V$	$\pm 100$ or (2) $\pm 50$	% pA
2	Gate Source Cut-off Voltage	$V_{GS(off)}$	MIL-STD-750 Method 3403	$V_{DS} = 15V$ $I_D = 1.0nA$	$\pm 10$	%
3	Drain Current	$I_{DSS}$	MIL-STD-750 Method 3413	$V_{DS} = 15V$ $V_{GS} = 0V$ Note 1	$\pm 15$	%

**NOTES**

1. Pulse measurement: Pulse length  $\leq 300\mu s$ , Duty Cycle  $\leq 2\%$
2. Whichever is greater.



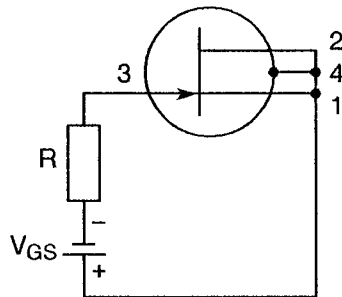
**TABLE 5 - CONDITIONS FOR H.T.R.B. BURN-IN AND OPERATING LIFE**



No.	CHARACTERISTICS	SYMBOL	CONDITION	UNIT
1	Ambient Temperature	$T_{amb}$	+ 150	°C
2	Drain Source Voltage	$V_{DS}$	0	V
3	Gate Source Voltage	$V_{GS}$	- 21	V
4	Test Method 1039 of MIL-STD-750	-	A	-

**NOTES**

1. H.T.R.B. burn-in shall be for 168 hours.

**FIGURE 5 - ELECTRICAL CIRCUITS FOR BURN-IN**



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4.8 ENVIRONMENTAL AND ENDURANCE TESTS (CHARTS IV AND V OF ESA/SCC GENERIC SPECIFICATION No. 5000)

4.8.1 Electrical Measurements on Completion of Environmental Tests

The parameters to be measured on completion of environmental tests are scheduled in Table 2. The measurements shall be performed at  $T_{amb} = +22 \pm 3$  °C.

4.8.2 Electrical Measurements at Intermediate Points and on Completion of Endurance Tests

The parameters to be measured at intermediate points and on completion of endurance tests are scheduled in Table 6.

4.8.3 Conditions for Operating Life Tests (Part of Endurance Testing)

The requirements for operating life testing are specified in Section 9 of ESA/SCC Generic Specification No. 5000. The conditions for operating life testing shall be as specified in Table 5 for the burn-in test.

4.8.4 Electrical Circuits for Operating Life Tests

The circuit to be used for performance of the operating life tests shall be as shown in Figure 5 for burn-in.

4.8.5 Conditions for High Temperature Storage Test (Part of Endurance Testing)

The requirements for the high temperature storage test are specified in ESA/SCC Generic Specification No. 5000. The temperature to be applied shall be the maximum storage temperature specified in Table 1(b) of this specification.

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**TABLE 6 - ELECTRICAL MEASUREMENTS AT INTERMEDIATE POINTS AND ON COMPLETION OF ENDURANCE TESTING**

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	LIMITS		UNIT
					MIN.	MAX.	
1	Total Gate Leakage Current	$I_{GSS}$	MIL-STD-750 Method 3411	$V_{DS} = 0V$ $V_{GS} = -20V$	-	-0.1	nA
2	Gate Source Cut-off Voltage - Variant 01 - Variant 02	$V_{GSoff}$	MIL-STD-750 Method 3403	$V_{DS} = 15V$ $I_D = 1.0nA$	- -2.5	-6.0 -6.0	V
3	Drain Current	$I_{DSS}$	MIL-STD-750 Method 3413	$V_{DS} = 15V$ $V_{GS} = 0V$ Note 1	5.0	15	mA

**NOTES**

1. Pulse measurement: Pulse length  $\leq 300\mu s$ , Duty Cycle  $\leq 2\%$