TRANSISTORS, MOSFET, P-CHANNEL, POWER,

BASED ON TYPES 2N6849 AND 2N6851

ESCC Detail Specification No. 5206/003

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Pages 1 to 29

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space components
coordination group

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Issue 1	December 1985	-	-
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DOCUMENTATION CHANGE NOTICE

Rev. Letter	Rev. Date	Reference	CHANGE Item	Approved DCR No.
'A'	Sept. 89	P1. Cover page		None
		P2. DCN		None
		P14. Para. 4.2.1	: Paragraph amended	22538
		P15. Para. 4.3.2	: Weight corrected	23367
		P19. Table 2	: No. 7, Min and Max Limits amended	22484
		P20. Table 2	: No. 13, Min and Max Limits amended	22484
'B'	Feb. '92	P1. Cover Page		None
		P2. DCN		None
		P5. Para. 1.2	: Paragraph amended	21021
		P13. Para. 2	: "ESA/SCC Basic Spec. No. 23500" added	21025
		P14. Para. 4.2.2	: Bond Strength and Die Shear Test deviations deleted	23499
			: PIND deviation deleted	21043
		Para. 4.2.3	: H.T.R.B. deviation deleted, subsequent deviations renumbered	23499
		P15. Para. 4.2.3	: Radiographic Inspection deviation deleted	21049
		Para. 4.2.4	: Bond Strength and Die Shear Test deviations deleted	23499
		P21. Table 3(b)	: Notes put under this table and renumbered	21047
'C'	March '93	P1. Cover page		None
		P2. DCN		None
		P20. Table 2	: Limits for item 13 amended	22970
'D'	Feb. '94	P1. Cover page		None
		P2. DCN		None
		P20. Table 2 a.c.	: Min. limit of item 15 for Variant 02 amended	221078
		This document has been transferred from hardcopy to electronic format. The content is unchanged but minor differences in presentation exist.		

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FIGURES

APPENDICES (Applicable to specific Manufacturers only)
None.

1. GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics, test and inspection data for Transistors, MOSFET, Power, P-Channel, based on Types 2N6849 and 2N6851.

It shall be read in conjunction with ESA/SCC Generic Specification No. 5000, the requirements of which are supplemented herein.

1.2 COMPONENT TYPE VARIANTS

See Table 1(a).

1.3 MAXIMUM RATINGS

The maximum ratings, which shall not be exceeded at any time during use or storage, applicable to the transistors specified herein, are as scheduled in Table 1(b).

1.4 PARAMETER DERATING INFORMATION

The parameter derating information applicable to the transistors specified herein is shown in Figure 1(a).

1.5 SAFE OPERATING AREA

The applicable safe operating area information for the transistors specified herein is shown in Figure 1(b).

1.6 PHYSICAL DIMENSIONS

The physical dimensions of the transistors specified herein are shown in Figure 2.

1.7 FUNCTIONAL DIAGRAM

The functional diagram, showing lead identification, of the transistors specified herein, is shown in Figure 3.

1.8 HANDLING PRECAUTIONS

These devices are susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be taken for protection during all phases of manufacture, testing, packaging, shipment and any handling.

TABLE 1(a) - TYPE VARIANTS

VARIANT	(1) LEAD MATERIAL AND FINISH	(2) JEDEC TYPE	(3) V_{DS} (MAX.) (V)	(4) I_D (MAX.) (NOTE 1) (A)	(5) I_D (MAX.) (NOTE 2) (A)	(6) I_S (NOTE 1) (A)	(7) V_{DD} (V)	(8) V_{DS} (80%) (V)	(9) I_{DM} (MAX.) (Apk)	(10) V_{DG} (V)
01	D2	2N6849	−100	−6.5	−4.1	−6.5	−42	−80	−25	−100
02	D2	2N6851	−200	−4.0	−2.4	−4.0	−95	−160	−20	−200

NOTES

1. At T_{case} = +25°C.
2. At T_{case} = +100°C.

TABLE 1(b) - MAXIMUM RATINGS

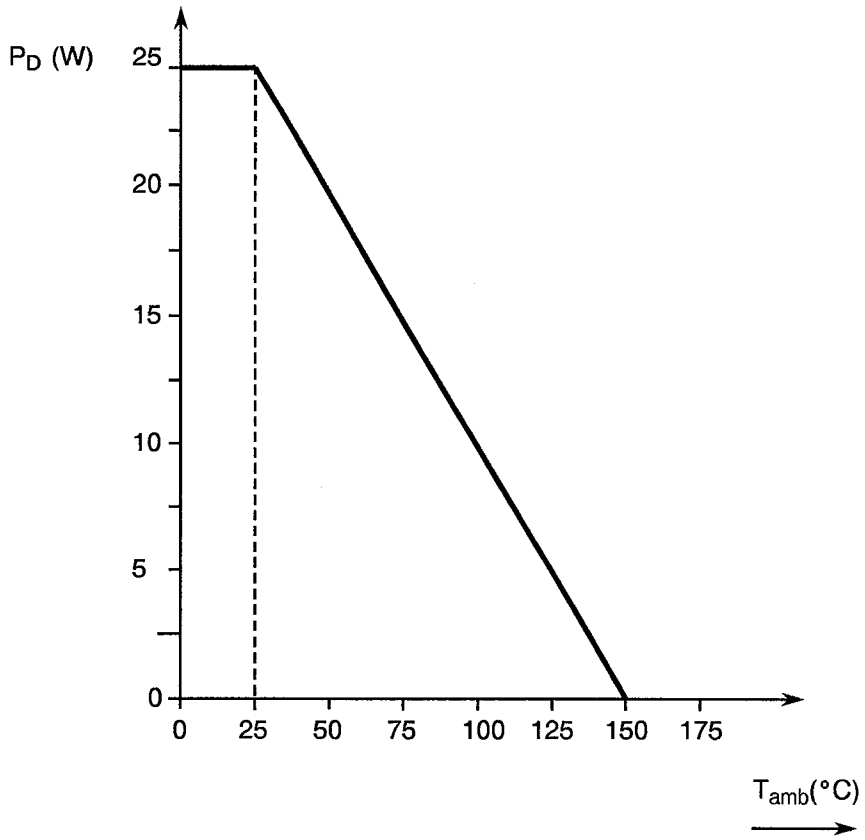
No.	CHARACTERISTICS	SYMBOL	MAXIMUM RATINGS	UNIT	REMARKS
1	Drain-Source Voltage	V_{DS}	Table 1(a) Column 3	Vdc	
2	Gate-Source Voltage	V_{GS}	±20	Vdc	
3	Drain-Gate Voltage	V_{DG}	Table 1(a) Column 10	Vdc	
4	Drain Current (Continuous)	I_D	Table 1(a) Column 4	Adc	At T_{case} = +25°C (2) (3)
5	Drain Current (Continuous)	I_D	Table 1(a) Column 5	Adc	At T_{case} = +100°C (2) (3)
6	Source Current (Continuous)	I_S	Table 1(a) Column 6	Adc	At T_{case} = +25°C (2) (3)
7	Drain Current Pulsed (Peak)	I_{DM}	Table 1(a) Column 9	Adc	Peak (2)
8	Total Power Dissipation	P_{tot}	25	W	At T_{case} = +25°C (1)
9	Operating Temperature Range	T_{op}	−55 to +150	°C	T_{amb}
10	Storage Temperature Range	T_{stg}	−55 to +150	°C	
11	Soldering Temperature	T_{sol}	+300	°C	Time: ≤10s Distance to case: ≥1.5mm
12	Thermal Resistance (Junction to Case)	$R_{TH(J-C)}$	5.0	°C/W	

NOTES

1. Derate linearly 0.20W/°C for T_{case} > +25°C (See Figure 1(a)).
2. These ratings apply at the case. Leads of TO-39 devices are not capable of carrying maximum drain currents beyond 2.0mm from the case without heatsink.
3. Derate for T_{case} > +25°C as follows:-

   $I_D = \sqrt{\frac{P(rated)}{K}}$ where: P(rated) = 25 − (T_{case} − 25) (0.20) watts.
   K = rated $r_{DS(ON)}$ at T_J = +150°C.

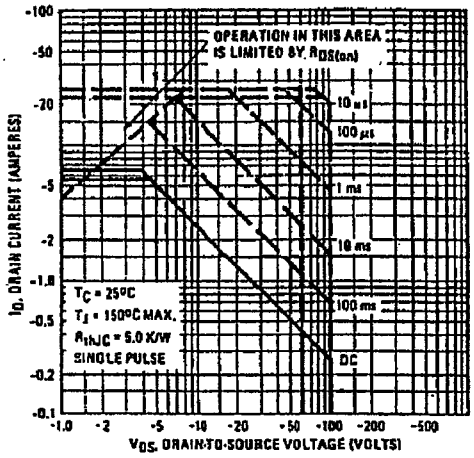
FIGURE 1(a) - PARAMETER DERATING INFORMATION (ALL VARIANTS)



Power Dissipation versus Temperature

FIGURE 1(b) - MAXIMUM SAFE OPERATING AREA

VARIANT 01



VARIANT 02

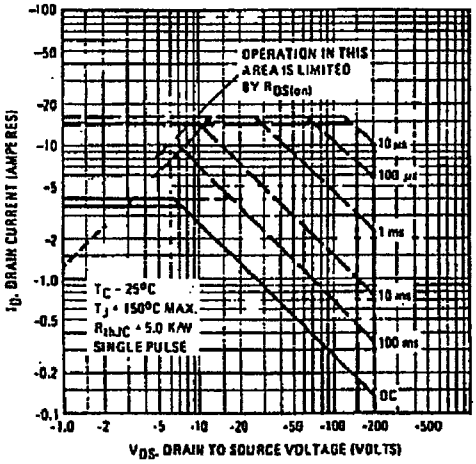
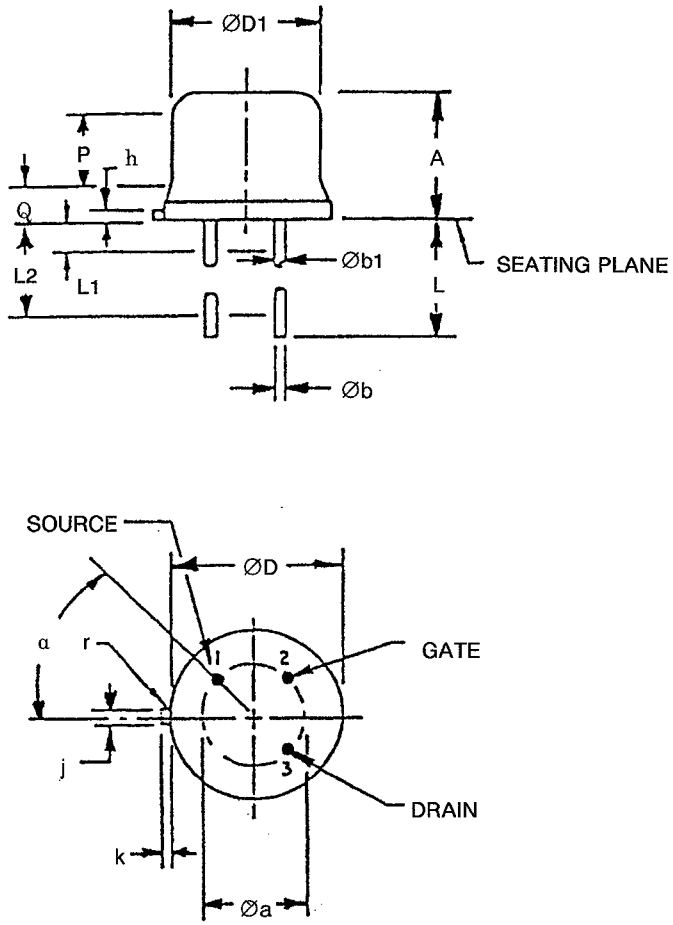


FIGURE 2 - PHYSICAL DIMENSIONS



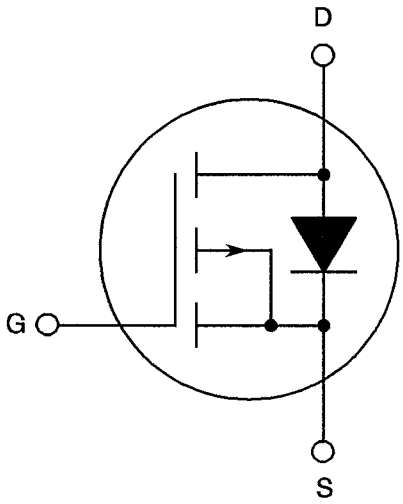
SYMBOL	MILLIMETRES		INCHES		NOTES (See Note 1)
	MIN.	MAX.	MIN.	MAX.	
A	4.074	4.57	0.160	0.180	
Øa	5.08 Typical		0.200 Typical		
Øb	0.41	0.53	0.016	0.021	7, 8
Øb1	0.41	0.48	0.016	0.019	7, 8
ØD	8.51	9.40	0.335	0.370	
ØD1	7.75	8.51	0.305	0.335	
h	0.23	1.04	0.009	0.041	
j	0.71	0.86	0.028	0.034	2
k	0.74	1.14	0.029	0.045	3
L	12.70	19.05	0.500	0.750	7, 8
L1	-	1.27	-	0.050	7, 8
L2	6.35	-	0.250	-	7, 8
P	2.54	-	0.100	-	5
Q	-	1.27	-	0.050	4
r	-	0.25	-	0.010	9
α	45° Typical		45° Typical		6

NOTES: See Page 11.

NOTES TO FIGURE 2 - PHYSICAL DIMENSIONS

1. Imperial equivalents are given for general information only and are based upon 25.4mm = 1inch.
2. Beyond r (radius) maximum, j shall be held for a minimum length of 0.28mm (0.11").
3. k measured from maximum ∅D.
4. Outline in this zone is not controlled.
5. ∅D1 shall not vary more than 0.25mm (0.010") in zone P. This zone is controlled for automatic handling.
6. Leads at gauge plane 1.37 + 0.03, -0.00 mm (0.054" + 0.001", -0.001", -0.000") below seating plane shall be within 0.18mm (0.007") radius of true position (TP) at maximum material condition (MMC) relative to tab at MMC. The device may be measured by direct methods or by gauge.
7. ∅b1 applies between L1 and L2. ∅b applies between L2 and L minimum. Diameter is uncontrolled in L1 and beyond L minimum.
8. All three leads.
9. r (radius) applies to both inside corners of tab.

FIGURE 3 - FUNCTIONAL DIAGRAM



NOTES

1. The drain is electrically connected to the case.

2. APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:-

(a) ESA/SCC Generic Specification No. 5000 for Discrete Semiconductor Components.

(b) MIL-STD-750, Test Methods and Procedures for Semiconductor Devices.

(c) ESA/SCC Basic Specification No. 23500, Requirements for Lead Materials and Finishes for Components for Space Application.

3. TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESA/SCC Basic Specification No. 21300 shall apply. In addition, the following abbreviations are used:-

I_{GSS} = Gate to Body Leakage Current.
B_{VGSS} = Gate to Source Breakdown Voltage.
$V_{GS(th)}$ = Gate Threshold Voltage.
V_{GS} = Gate to Source Voltage.
V_{DG} = Drain to Gate Voltage.
V_{DS} = Drain to Source Voltage.
gfs = Forward Transfer Conductance.
C_{iss} = Common Source Input Capacitance.
C_{oss} = Common Source Output Capacitance.
C_{rss} = Common Source Reverse Transfer Capacitance.
I_S = Source Current.
I_D = Drain Current.

4. REQUIREMENTS

4.1 GENERAL

The complete requirements for procurement of the transistors specified herein are stated in this specification and ESA/SCC Generic Specification No. 5000 for Discrete Semiconductor Components. Deviations from the Generic Specification applicable to this specification only, are listed in Para. 4.2.

Deviations from the applicable Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESA/SCC requirements and do not affect the components' reliability, are listed in the appendices attached to this specification.

4.2 DEVIATIONS FROM GENERIC SPECIFICATION

4.2.1 Deviations from Special In-process Controls

(a) For testing levels 'B' and 'C', a Scanning Electron Microscope (SEM) inspection shall be performed on samples from each metallisation lot in accordance with ESA/SCC Basic Specification No. 21400.

4.2.2 Deviations from Final Production Tests (Chart II)

None.

4.2.3 Deviations from Burn-in and Electrical Measurements (Chart III)

(a) Burn-in Test: The duration shall be 240 hours.

(b) The following test shall be added to the Electrical Measurements at Room Temperature; to be performed after the burn-in test only:-

Verification of Safe Operating Area (See Figure 4(a))

Test 'A' Condition (Variant 01)

T_{case} = +25 ± 10 °C; duration = 0.1sec.

V_{DS} = -80Vdc; I_D = -310mAdc

Test 'A' Condition (Variant 02)

T_{case} = +25 ± 10 °C; duration = 0.1sec.

V_{DS} = -160Vdc; I_D = -155mAdc

Test 'B' Condition (Variant 01)

T_{case} = +25 ± 10 °C; duration = 0.1sec.

V_{DS} = -3.85Vdc; I_D = -6.5Adc

Test 'B' Condition (Variant 02)

T_{case} = +25 ± 10 °C; duration = 0.1sec.

V_{DS} = -6.25Vdc; I_D = -4.0Adc

Test Method for Both Tests

Using a 0.1 second pulse width with a minimum of 1 minute between pulses, increase V_{GS} and the Drain Supply Voltage until the specified value of I_D and V_{DS} are obtained. A load resistor, R_L, shall be used and shall be selected such that $I_D.R_L = 2.5 \pm 1.0$ Vdc (All Variants).

Electrical Measurements

After performing both tests, the electrical measurements Nos. 1 to 7 inclusive of Table 2 shall be repeated.

4.2.4 Deviations from Qualification Tests (Chart IV)

None.

4.2.5 Deviations from Lot Acceptance Tests (Chart V)

None.

4.3 MECHANICAL REQUIREMENTS

4.3.1 Dimension Check

The dimensions of the transistors specified herein shall be checked. They shall conform to those shown in Figure 2.

4.3.2 Weight

The maximum weight of the transistors specified herein shall be 1.1 grammes.

4.3.3 Terminal Strength

The requirements for terminal strength testing are specified in Section 9 of ESA/SCC Generic Specification No. 5000. The test conditions shall be as follows:-

Test Condition : 'E', Lead Fatigue.
Applied Force : 2.2 Newtons.
Duration : 10 seconds.

4.4 MATERIALS AND FINISHES

The materials and finishes shall be as specified herein. Where a definite material is not specified, a material which will enable the transistors specified herein to meet the performance requirements of this specification shall be used. Acceptance or approval of any constituent material does not guarantee acceptance of the finished product.

4.4.1 Case

Metal case, hermetically sealed, similar to JEDEC TO-39.

4.4.2 Lead Material and Finish

The lead material shall be Type 'D' with Type '2' finish in accordance with the requirements of ESA/SCC Basic Specification No. 23500.

4.5 MARKING

4.5.1 General

The marking of components delivered to this specification shall be in accordance with the requirements of ESA/SCC Basic Specification No. 21700. Each component shall be marked in respect of:-

(a) Lead Identification.

(b) The SCC Component Number.

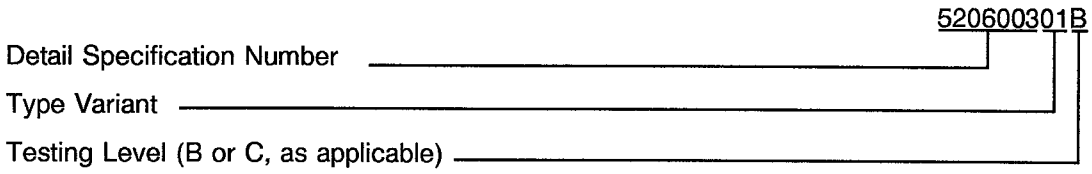
(c) Traceability Information.

4.5.2 Lead Identification

Lead identification shall be as shown in Figures 2 and 3.

4.5.3 The SCC Component Number

Each component shall bear the SCC Component Number which shall be constituted and marked as follows:



4.5.4 Traceability Information

Each component shall be marked in respect of traceability information in accordance with the requirements of ESA/SCC Basic Specification No. 21700.

4.5.5 Marking of Small Components

When it is considered that the component is too small to accommodate the marking as specified above, as much as space permits shall be marked. The order of precedence shall be as follows:-

(a) The SCC Component Number.

(b) Date Code.

(c) Serial Number

(d) Manufacturers Identification or Symbol.

The marking information in full shall accompany each component in its primary package.

4.6 ELECTRICAL MEASUREMENTS

4.6.1 Electrical Measurements at Room Temperature

The parameters to be measured at room temperature are scheduled in Table 2. The measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.6.2 Electrical Measurements at High and Low Temperatures

The parameters to be measured at high and low temperatures are scheduled in Table 3. The measurements shall be performed at $T_{amb} = +125(+0-5)$ and $-55(+5-0)$ °C respectively.

4.6.3 Circuits for Electrical Measurements

Circuits for use in performing the electrical measurements listed in Tables 2 and 3 of this specification are shown in Figure 4.

4.7 BURN-IN TESTS

4.7.1 Parameter Drift Values

The parameter drift values applicable to burn-in are specified in Table 4 of this specification. Unless otherwise stated, measurements shall be performed at $T_{amb} = +22 \pm 3$ °C. The parameter drift values (Δ) applicable to the parameters scheduled, shall not be exceeded. In addition to these drift value requirements, the appropriate limit value specified for a given parameter in Table 2 shall not be exceeded.

4.7.2 Conditions for H.T.R.B and Power Burn-in

The requirements for H.T.R.B. and Power burn-in are specified in Section 7 of ESA/SCC Generic Specification No. 5000. The conditions for H.T.R.B. and Power Burn-in shall be as specified in Tables 5(a) and 5(b) of this specification.

4.7.3 Electrical Circuits for H.T.R.B. and Power Burn-in

Circuits for use in performing the H.T.R.B. and Power Burn-in tests are shown in Figures 5(a) and 5(b) of this specification.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS

No.	CHARACTERISTICS	SYMBOL	MIL-STD 750 TEST METHOD	TEST CONDITIONS	LIMITS		UNIT
					MIN	MAX	
1	Breakdown Voltage Drain-Source Variant 01 Variant 02	B_{VDSS}	3407 Bias Cond. 'C'	I_D = −0.25mAdc V_{GS} = 0Vdc	 −100 −200	 - -	Vdc
2	Gate Threshold Voltage	$V_{GS(th)}$	3403	$V_{DS} \geq V_{GS}$ I_D = −0.25mAdc	−2.0	−4.0	Vdc
3	Gate-Body Leakage Current	I_{GSS}	3411 Bias Cond. 'C'	V_{GS} = −20V, V_{DS} = 0Vdc	-	−100	nAdc
4	Drain Current	I_{DSS}	3413 Bias Cond. 'C'	V_{DS} = Note 2 Vdc V_{GS} = 0Vdc	-	−0.25	mAdc
5	Drain-Source ON Resistance Variant 01 Variant 02	$r_{DS(ON)}$	3421	V_{GS} = −10Vdc I_D = −4.1Adc I_D = −2.4Adc Notes 1 and 6	 - -	 0.30 0.80	Ω
6	Drain-Source ON Voltage Variant 01 Variant 02	$V_{DS(ON)}$	3405	V_{GS} = −10Vdc I_D = −6.5Adc I_D = −4.0Adc Notes 1 and 6	 - -	 −2.0 −3.3	Vdc
7	Body Drain Diode Forward Voltage Variant 01 Variant 02	V_{SD}	4011	 I_S = −6.5Adc I_S = −4.0Adc Note 1	 −2.0 −2.6	 −4.3 −5.6	Vdc

NOTES

1. Pulsed Measurement: Pulse Width ≤ 300μs, Duty Cycle ≤ 2.0%.
2. See Column 3 of Table 1(a).
3. See Column 5 of Table 1(a).
4. See Column 7 of Table 1(a).
5. See Column 8 of Table 1(a).
6. Measured within 2.0mm of case.
7. Measurements to be performed on a sample basis, LTPD7.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS

No.	CHARACTERISTICS	SYMBOL	MIL-STD 750 TEST METHOD	TEST FIG.	TEST CONDITIONS (NOTE 7)	LIMITS		UNIT
						MIN	MAX	
8	Forward Transconductance Variant 01 Variant 02	gfs	3455	-	V_{DS} = −5.0Vdc I_D = −4.1Adc I_D = −2.4Adc Note 1	 2.5 2.2	 7.5 6.6	S
9	Turn-on Delay Time Variant 01 Variant 02	$t_{d(ON)}$	3459	4(b)	I_D = (3) Adc V_{DD} = (4) Vdc	 - -	 60 50	ns
10	Rise Time Variant 01 Variant 02	t_r	3251	4(b)	I_D = (3) Adc V_{DD} = (4) Vdc	 - -	 140 100	ns
11	Turn-off Delay Time Variant 01 Variant 02	$t_{d(OFF)}$	3251	4(b)	I_D = (3) Adc V_{DD} = (4) Vdc	 - -	 140 80	ns
12	Fall Time Variant 01 Variant 02	t_f	3251	4(b)	I_D = (3) Adc V_{DD} = (4) Vdc	 - -	 140 80	ns
13	Common Source Input Capacitance Variant 01 Variant 02	C_{iss}	3431	-	V_{DS} = −25Vdc V_{GS} = 0Vdc, f = 1.0MHz	 500 500	 950 950	pF
14	Common Source Output Capacitance Variant 01 Variant 02	C_{oss}	3453	4(c)	V_{DS} = −25Vdc V_{GS} = 0Vdc, f = 1.0MHz	 150 100	 450 300	pF
15	Common Source Reverse Transfer Capacitance Variant 01 Variant 02	C_{rss}	3433	-	V_{DS} = −25Vdc V_{GS} = 0Vdc, f = 1.0MHz	 50 30	 200 90	pF

NOTES: See Page 19.

TABLE 3(a) - ELECTRICAL MEASUREMENTS AT HIGH TEMPERATURE, +125(+0-5) °C

No.	CHARACTERISTICS	SYMBOL	MIL-STD 750 TEST METHOD	TEST CONDITIONS	LIMITS		UNIT
					MIN	MAX	
2	Gate Threshold Voltage	$V_{GS(th)}$	3403	$V_{DS} \geq V_{GS}$ $I_D = -0.25$mAdc	−1.0	-	Vdc
3	Gate-Body Leakage Current	I_{GSS}	3411 Bias Cond. 'C'	$V_{GS} = -20$Vdc $V_{DS} = 0$Vdc	-	−200	nAdc
4	Drain Current	I_{DSS}	3413 Bias Cond. 'C'	$V_{DS} = (2)$ Vdc $V_{GS} = 0$Vdc	-	−1.0	mAdc
5	Drain-Source ON Resistance Variant 01 Variant 02	$r_{DS(ON)}$	3421	$V_{GS} = -10$V $I_D = -4.1$Adc $I_D = -2.4$Adc Notes 1 and 3	 - -	 0.54 1.6	Ω

TABLE 3(b) - ELECTRICAL MEASUREMENTS AT LOW TEMPERATURE, -55 (+5-0) °C

No.	CHARACTERISTICS	SYMBOL	MIL-STD 750 TEST METHOD	TEST CONDITIONS	LIMITS		UNIT
					MIN	MAX	
2	Gate Threshold Voltage	$V_{GS(th)}$	3403	$V_{DS} \geq V_{GS}$ $I_D = -0.25$mAdc	-	−5.0	Vdc

NOTES

1. Pulsed: Pulse Width ≤300μs, Duty Cycle ≤2.0%.
2. See Column 8 of Table 1(a).
3. Measured within 2.0mm of case.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS

FIGURE 4(a) - SAFE OPERATING AREA TEST CIRCUIT

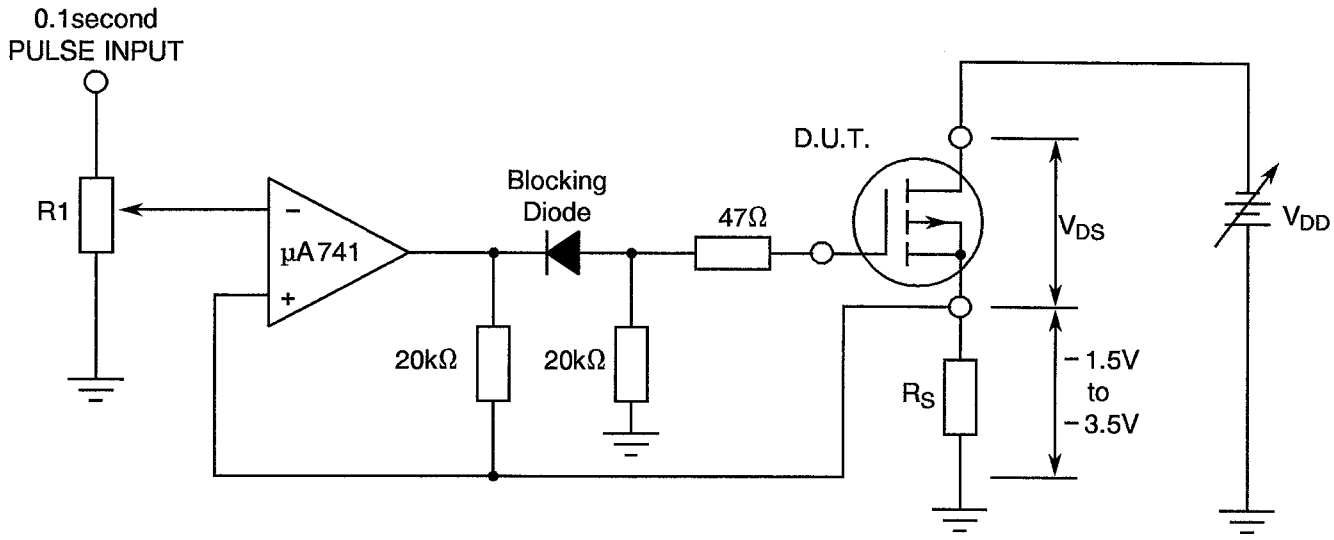
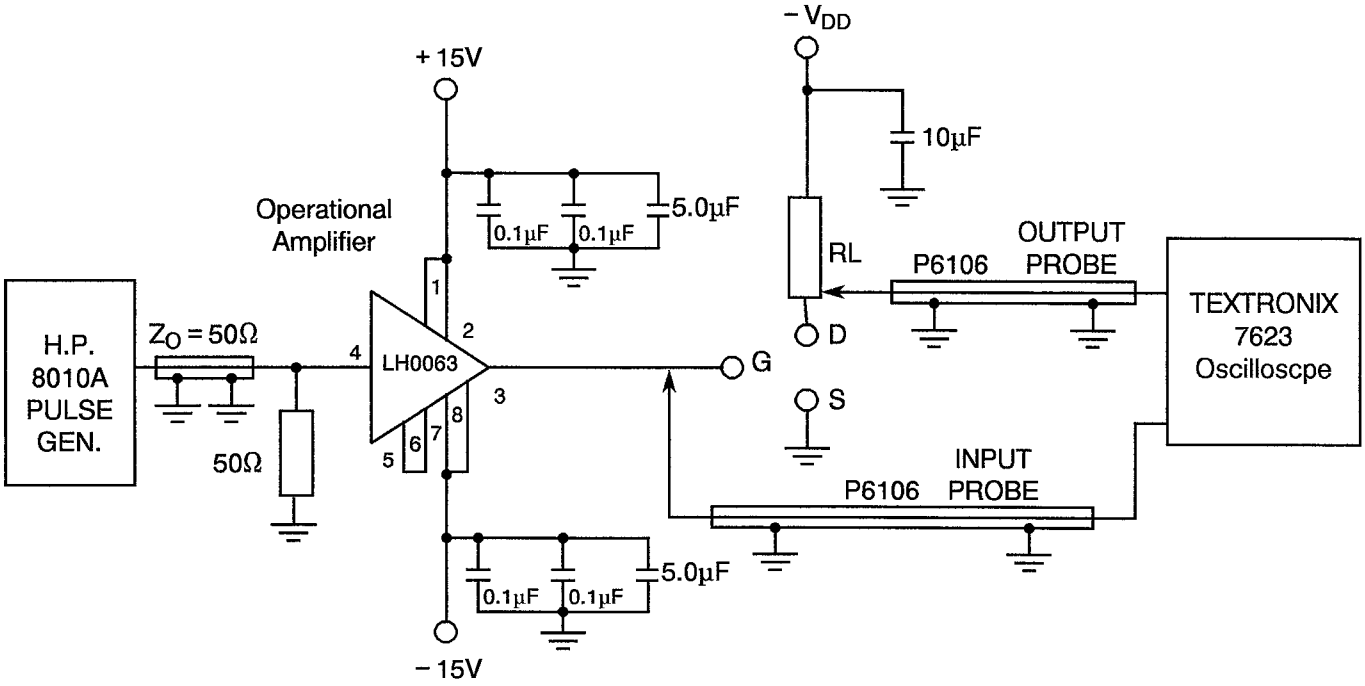


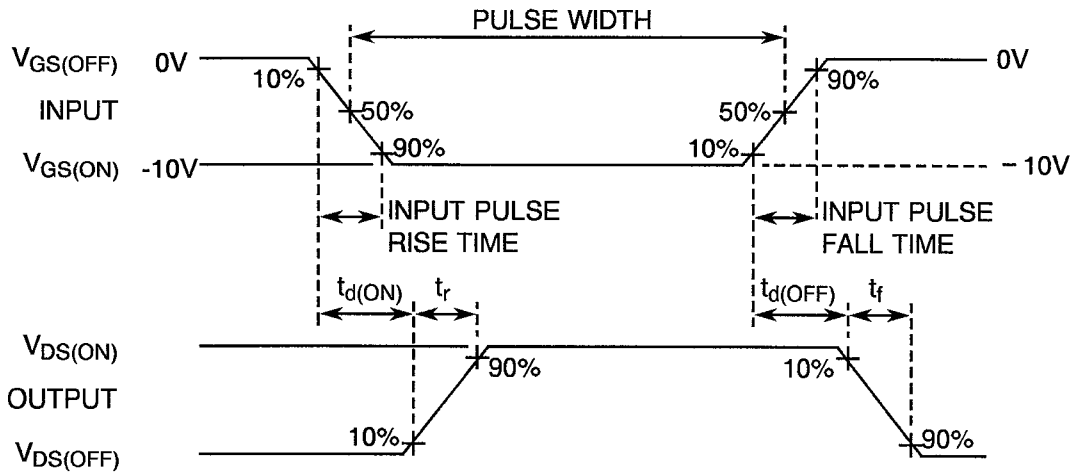
FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(b) - SWITCHING TIMES TEST CIRCUIT



NOTES

1. LH0063 case grounded.
2. Grounded connections common to ground plane on board.
3. Pulse width ≤3.0s, Period ≤1.0ms, Amplitude = +0V to −10V.

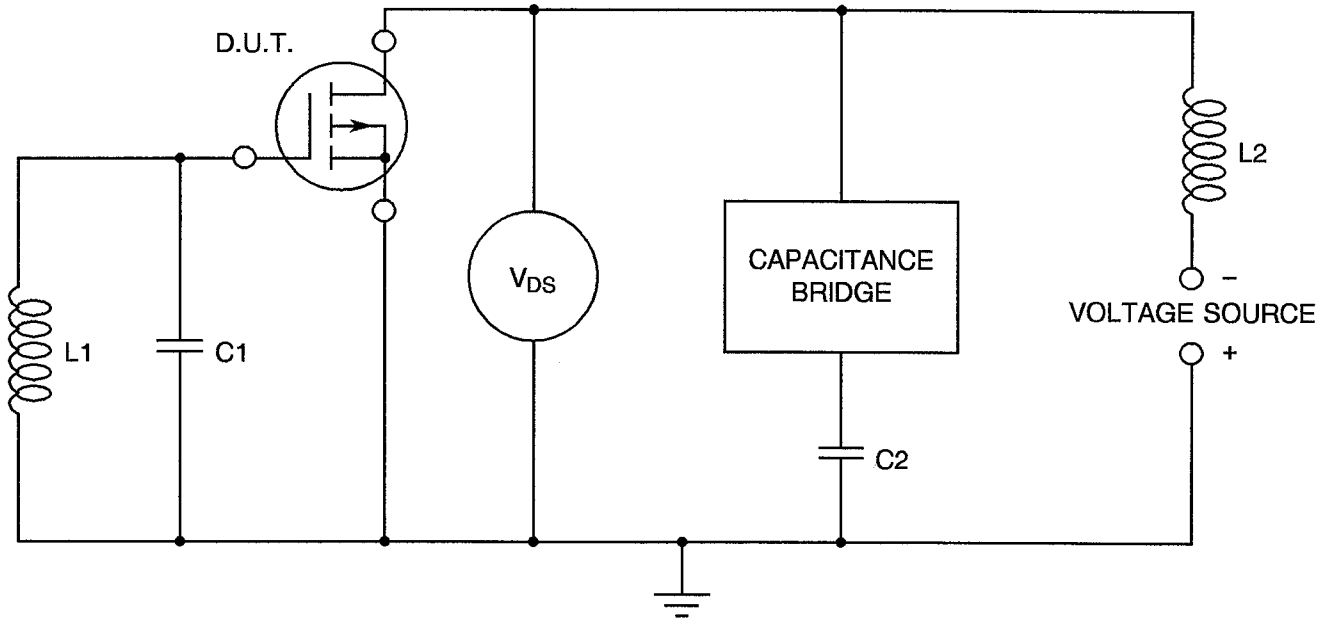


NOTES

1. When measuring rise time, $V_{GS(ON)}$ shall be as specified on the input waveform.
2. When measuring fall time, $V_{GS(OFF)}$ shall be as specified on the input waveform.
3. The input transition and drain voltage response detector shall have rise and fall response times such that doubling these responses will not affect the results greater than the precision of measurement.
4. The current shall be sufficiently small so that doubling it does not affect test results greater than the precision of measurement.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(c) - COMMON SOURCE OUTPUT CAPACITANCE



PROCEDURE

The capacitors C1 and C2 shall present apparent short circuits at the test frequency. L1 and L2 shall present a high a.c. impedance at the test frequency for isolation. The bridge shall have low d.c. resistance between its output terminals and should be capable of carrying the test current without affecting the desired accuracy of measurement.

TABLE 4 - PARAMETER DRIFT VALUES

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	CHANGE LIMITS (Δ)	UNIT
2	Gate Threshold Voltage	$V_{GS(th)}$	As per Table 2	As per Table 2	±20	%
3	Gate-Body Leakage Current	I_{GSS}	As per Table 2	As per Table 2	±20 or (1) ±100	nAdc %
4	Drain Current	I_{DSS}	As per Table 2	As per Table 2	±25 or (1) ±100	µAdc %
5	Drain-Source ON Resistance	$r_{DS(ON)}$	As per Table 2	As per Table 2	±20	%

NOTES

1. Whichever is greater referred to the initial value.

TABLE 5(a) - CONDITIONS FOR HTRB (PRE-CONDITIONING STRESS)

No.	CHARACTERISTICS	SYMBOL	CONDITION	UNIT
1	Ambient Temperature	T_{amb}	+150(+0−5)	°C
2	Drain-Source Voltage Variant 01 Variant 02	V_{DS}	 −80 −160	Vdc
3	Gate-Source Voltage	V_{GS}	0	Vdc
4	Duration	t	72	Hrs

TABLE 5(b) - CONDITIONS FOR POWER BURN-IN AND OPERATING LIFE TESTS

No.	CHARACTERISTICS	SYMBOL	CONDITION	UNIT
1	Junction Temperature	T_J	+140 ± 10 (1)	°C
2	Drain-Source Voltage	V_{DS}	−10	Vdc
3	Gate-Source Voltage	V_{GS}	−1.0 to −16	Vdc
4	Duration	t	240	Hrs

NOTES

1. Using the circuit shown in Figure 5(b), power shall be applied to the device to achieve the specified junction temperature. The junction temperature (T_J) should be determined as follows:-

   $T_J = (P_T) \times (R_{TH(J-C)}) + T_{case}$.

   $P_T = (V_{DS}) \times (I_D)$.

   $R_{TH(J-C)}$ = 5.0°C/W

   T_{case} = Measured value at the hottest point on the case.

FIGURE 5(a) - ELECTRICAL CIRCUIT FOR HIGH TEMPERATURE REVERSE BIAS BURN-IN

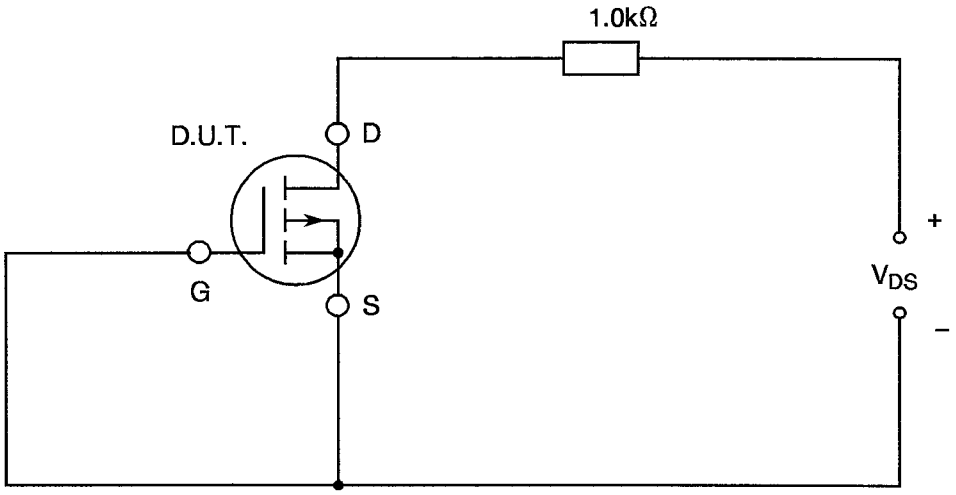
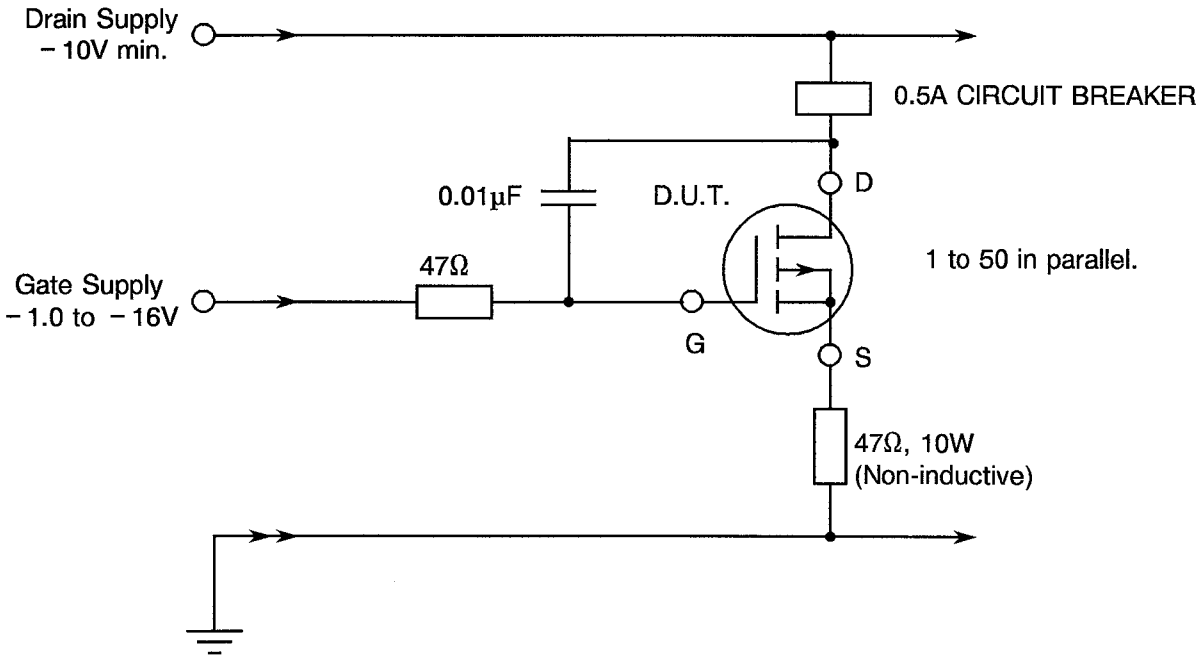


FIGURE 5(b) - ELECTRICAL CIRCUIT FOR BURN-IN AND OPERATING LIFE TESTS



4.8 ENVIRONMENTAL AND ENDURANCE TESTS (CHARTS IV AND V OF ESA/SCC GENERIC SPECIFICATION NO. 5000)

4.8.1 Electrical Measurements on Completion of Environmental Tests

The parameters to be measured on completion of environmental tests are scheduled in Table 2. The measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.8.2 Electrical Measurements at Intermediate Points and on Completion of Endurance Tests

The parameters to be measured at intermediate points and on completion of endurance tests are scheduled in Table 6. The measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.8.3 Conditions for Operation Life Tests (Part of Endurance Testing)

The requirements for operating life testing are specified in Section 9 of ESA/SCC Generic Specification No. 5000. The conditions for operating life testing shall be the same as specified in Table 5(b) for the burn-in test.

4.8.4 Electrical Circuits for Operating Life Tests

The circuit to be used for performance of the operating life tests shall be the same as shown in Figure 5(b) for the burn-in test.

4.8.5 Conditions for High Temperature Storage Test (Part of Endurance Testing)

The requirements for the high temperature storage test are specified in ESA/SCC Generic Specification No. 5000. The conditions for high temperature storage shall be $T_{amb} = 150(+0\text{-}5)$ °C.

TABLE 6 - ELECTRICAL MEASUREMENTS AT INTERMEDIATE POINTS AND ON COMPLETION OF ENDURANCE TESTING

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	LIMITS		UNIT
					MIN.	MAX.	
2	Gate Threshold Voltage	$V_{GS(th)}$	As per Table 2	As per Table 2	− 2.0	− 4.0	Vdc
3	Gate-Body Leakage Current	I_{GSS}	As per Table 2	As per Table 2	- -	− 100	nAdc
4	Drain Current	I_{DSS}	As per Table 2	As per Table 2	-	− 0.25	mAdc