INTEGRATED CIRCUITS, SILICON MONOLITHIC,

CMOS DUAL 4-INPUT NAND GATES,

BASED ON TYPE 4012B

ESCC Detail Specification No. 9201/044

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SCC

space components
coordination group

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Issue 3	June 2001	[signature]	[signature]

DOCUMENTATION CHANGE NOTICE

Rev. Letter	Rev. Date	CHANGE Reference	CHANGE Item	Approved DCR No.
		This Issue supersedes Issue 2 and incorporates all modifications defined in Revisions 'A', 'B' and 'C' to Issue 2 and the changes agreed in the following DCRs:-		
		Cover page		None
		DCN		None
		Para. 1.3	: New sentence added	221602
		Table 1(b)	: No. 8, Maximum temperature amended	221602
		Para. 4.8.6	: Last sentence deleted, new text added	221602
		Appendix 'A'	: Appendix added	221602

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TABLES

FIGURES

APPENDICES (Applicable to specific Manufacturers only)

1. GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics, test and inspection data for a silicon, monolithic, CMOS DUAL 4-Input NAND Gate, having fully buffered outputs, based on Type 4012B. It shall be read in conjunction with ESA/SCC Generic Specification No. 9000, the requirements of which are supplemented herein.

1.2 COMPONENT TYPE VARIANTS

Variants of the basic type integrated circuits specified herein, which are also covered by this specification, are given in Table 1(a).

1.3 MAXIMUM RATINGS

The maximum ratings, which shall not be exceeded at any time during use or storage, applicable to the integrated circuits specified herein, are as scheduled in Table 1(b).

Maximum ratings shall only be exceeded during testing to the extent specified in this specification and when stipulated in Test Methods and Procedures of the applicable ESA/SCC Generic Specification.

1.4 PARAMETER DERATING INFORMATION (FIGURE 1)

Not applicable.

1.5 PHYSICAL DIMENSIONS

As per Figure 2.

1.6 PIN ASSIGNMENT

As per Figure 3(a).

1.7 TRUTH TABLE

As per Figure 3(b).

1.8 CIRCUIT SCHEMATIC

As per Figure 3(c).

1.9 FUNCTIONAL DIAGRAM

As per Figure 3(d).

1.10 HANDLING PRECAUTIONS

These devices are susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacture, test, packaging, shipping and any handling. These components are catagorised as Class 1 with a Minimum Critical Path Failure Voltage of 400Volts.

1.11 INPUT PROTECTION NETWORK

Double diode protection shall be incorporated into each input as shown in Figure 3(e).

TABLE 1(a) - TYPE VARIANTS

VARIANT	CASE	FIGURE	LEAD MATERIAL AND/OR FINISH
01	FLAT	2(a)	G2 or G8
02	FLAT	2(a)	G4
03	D.I.L.	2(b)	G2 or G8
04	D.I.L.	2(b)	G4
07	CHIP CARRIER	2(c)	2
08	SO CERAMIC	2(d)	G2
09	SO CERAMIC	2(d)	G4

TABLE 1(b) - MAXIMUM RATINGS

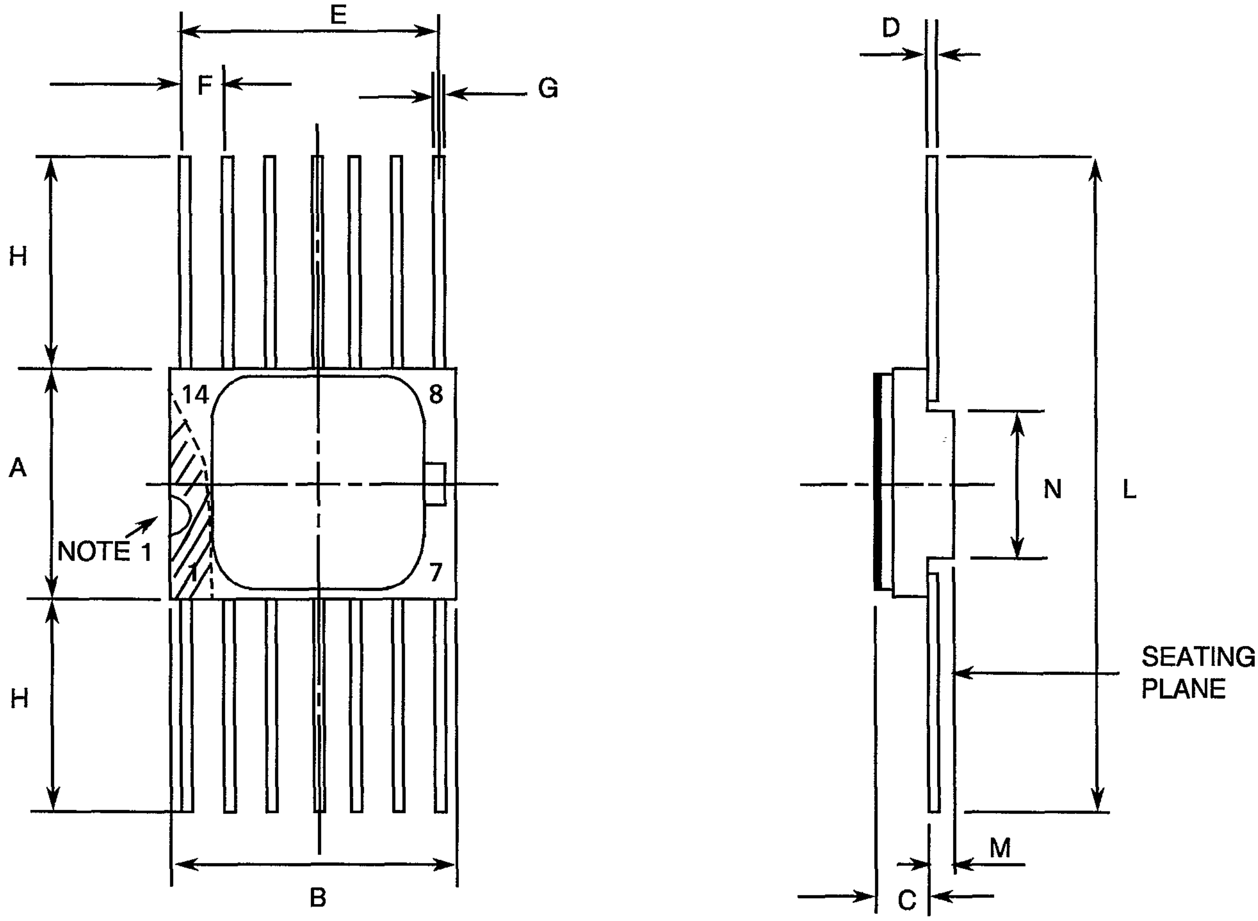
NO.	CHARACTERISTICS	SYMBOL	MAXIMUM RATINGS	UNITS	REMARKS
1	Supply Voltage	V_{DD}	-0.5 to +18	V	Note 1
2	Input Voltage	V_{IN}	-0.5 to V_{DD} + 0.5	V	Note 2 Power on
3	D.C. Input Current	$\pm I_{IN}$	10	mA	-
4	D.C. Output Current	$\pm I_{O}$	10	mA	Note 3
5	Device Dissipation	P_D	200	mWdc	Per Package
6	Output Dissipation	P_{DSO}	100	mWdc	Note 4
7	Operating Temperature Range	T_{op}	-55 to +125	°C	-
8	Storage Temperature Range	T_{stg}	-65 to +150	°C	-
9	Soldering Temperature for FP and DIP for CCP	T_{sol}	 +300 +245	°C	 Note 5 Note 6

NOTES

1. Device is functional from +3V to +15V with reference to V_{SS}.
2. V_{DD} + 0.5V should not exceed +18V.
3. The maximum output current of any single output.
4. The maximum power dissipation of any single output.
5. Duration 10 seconds maximum at a distance of not less than 1.5mm from the device body and the same lead shall not be resoldered until 3 minutes have elapsed.
6. Duration 30 seconds maximum and the same terminals shall not be resoldered until 3 minutes have elapsed.

FIGURE 2 - PHYSICAL DIMENSIONS

FIGURE 2(a) - FLAT PACKAGE, 14-Pin

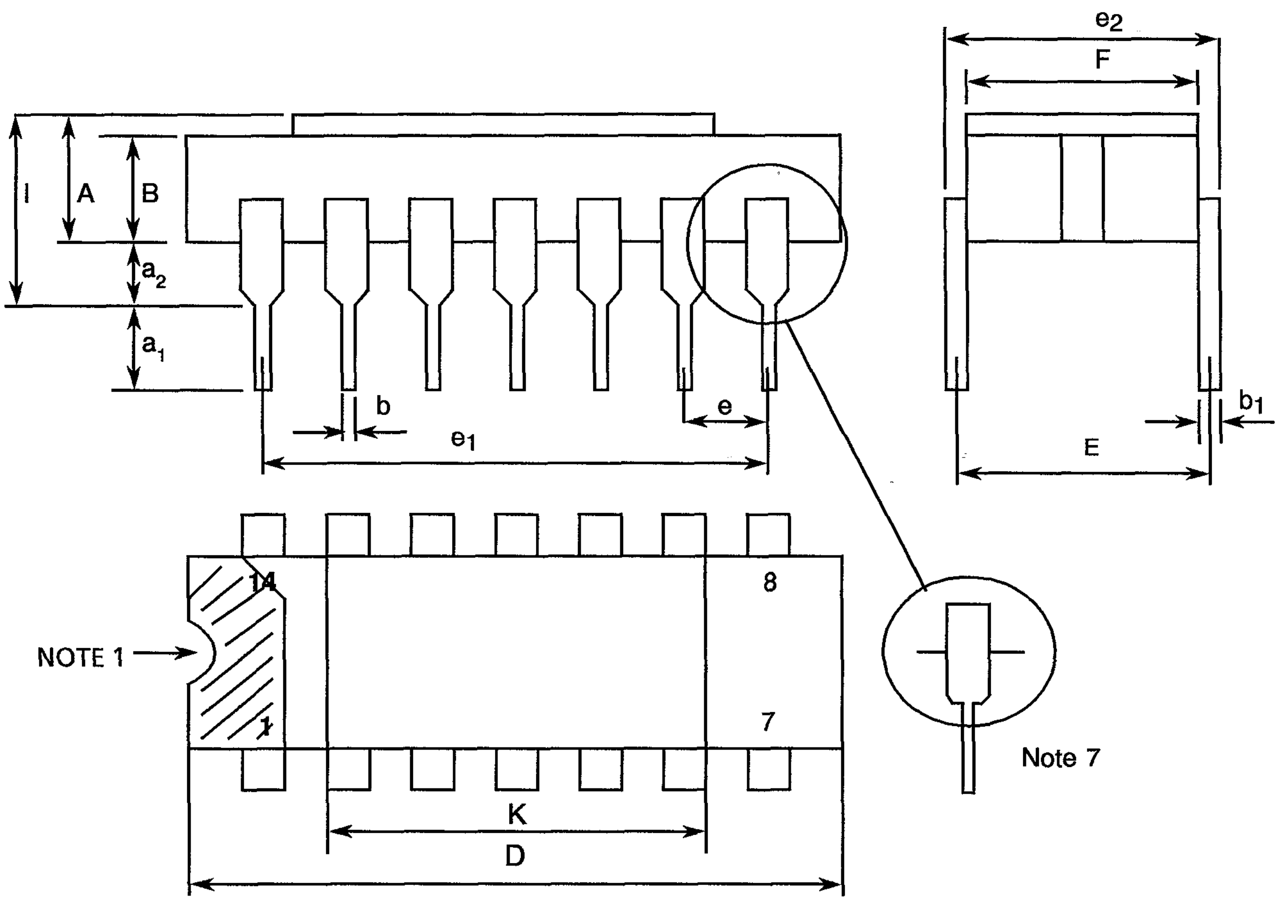


SYMBOL	MILLIMETRES		NOTES
	MIN	MAX	
A	6.75	7.06	
B	9.76	10.14	
C	1.49	1.95	
D	0.102	0.152	3
E	7.50	7.75	
F	1.27 TYPICAL		4
G	0.38	0.48	3
H	6.0	-	3
L	18.75	22.0	
M	0.33	0.43	
N	4.31 TYPICAL		

NOTES: See Page 11.

FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)

FIGURE 2(b) - DUAL-IN-LINE PACKAGE, 14-PIN

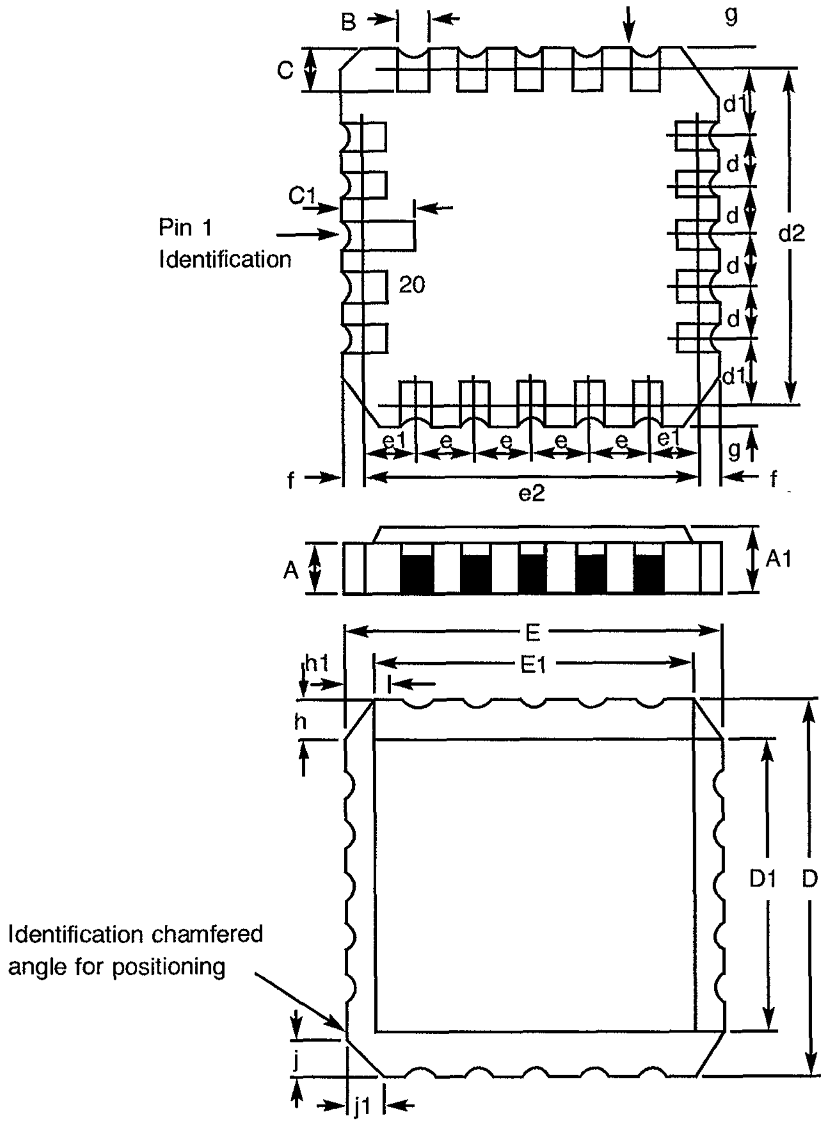


SYMBOL	MILLIMETRES		NOTES
	MIN	MAX	
A	2.10	2.54	
a_1	3.0	3.7	
a_2	0.63	1.14	2
B	1.82	2.23	
b	0.40	0.50	3
b_1	0.20	0.30	3
D	18.79	19.20	
E	7.36	7.87	
e	2.29	2.79	4
e_1	15.11	15.37	
e_2	7.62	8.12	
F	7.11	7.75	
I	-	3.70	
K	10.90	12.10	

NOTES: See Page 11.

FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)

FIGURE 2(c) - CHIP CARRIER - 20-TERMINAL

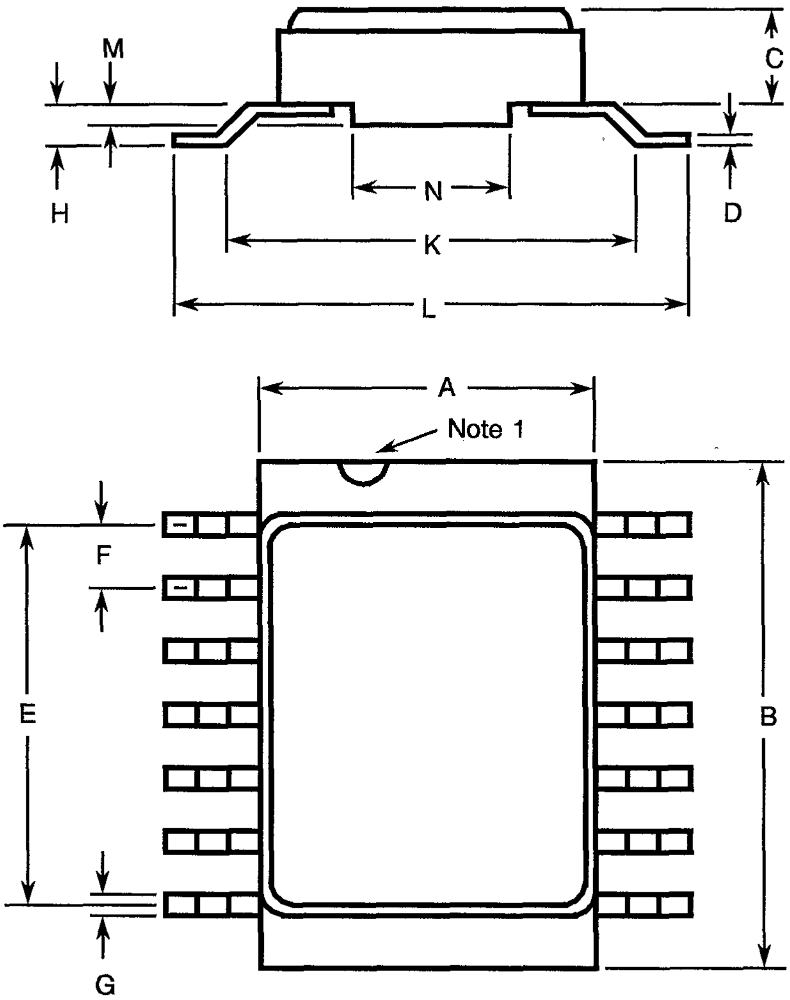


DIMENSIONS	MILLIMETRES		NOTES
	MIN	MAX	
A	1.14	1.95	
A1	1.63	2.36	
B	0.55	0.72	3
C	1.06	1.47	3
C_1	1.91	2.41	
D	8.67	9.09	
D1	7.21	7.52	
d, d1	1.27	TYPICAL	4
d2	7.62	TYPICAL	
E	8.67	9.09	
E1	7.21	7.52	
e, e1	1.27	TYPICAL	4
e2	7.62	TYPICAL	
f, g	-	0.76	
h,h1	1.01	TYPICAL	6
j, j1	0.51	TYPICAL	5

NOTES: See Page 11.

FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)

FIGURE 2(d) - SMALL OUTLINE CERAMIC PACKAGE, 14-PIN



SYMBOL	MILLIMETRES		NOTES
	MIN.	MAX.	
A	6.75	7.06	
B	9.76	10.14	
C	1.49	1.95	
D	0.102	0.152	3
E	7.50	7.75	
F	1.27 TYPICAL		4
G	0.38	0.48	3
H	0.60	0.90	3
K	9.00 TYPICAL		
L	10	10.65	
M	0.33	0.43	
N	4.31 TYPICAL		

NOTES: See Page 11.

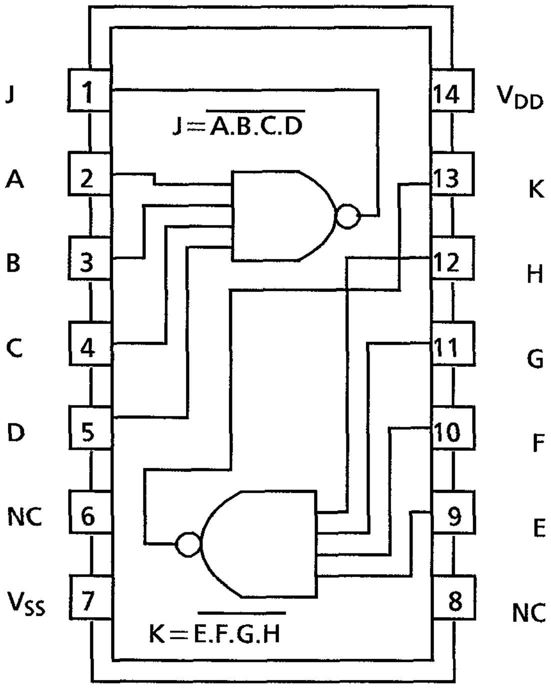
FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)

NOTES TO FIGURES 2(a) TO 2(d) INCLUSIVE

1. Index area: a notch, letter or dot shall be located adjacent to Pin 1 and shall be within the shaded area shown. For chip carrier packages the index shall be as defined in Figure 2(c).
2. The dimension shall be measured from the seating plane to the base plane.
3. All leads or terminals.
4. Twelve spaces.
5. Index corner only.
6. Three non-index corners.
7. For all pins, either pin shape may be supplied.

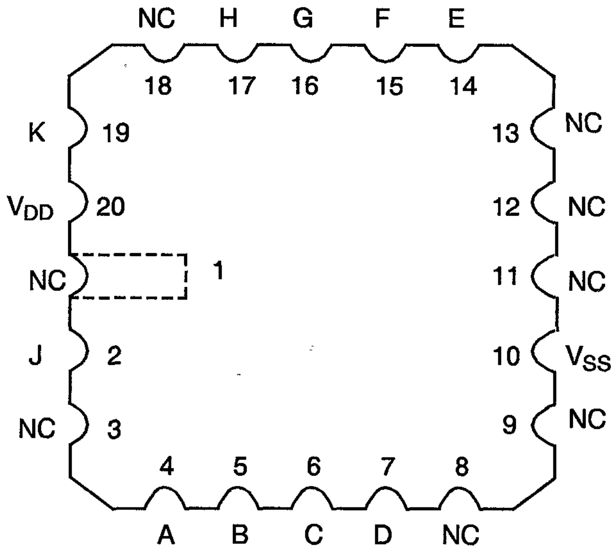
FIGURE 3(a) - PIN ASSIGNMENT

DUAL-IN-LINE, SO AND FLAT PACKAGES



TOP VIEW

CHIP CARRIER PACKAGE



TOP VIEW

FLAT PACKAGE, SO AND DUAL-IN-LINE TO CHIP CARRIER PIN ASSIGNMENT

FLAT PACKAGE, SO AND DUAL-IN-LINE PIN OUTS	1	2	3	4	5	6	7	8	9	10	11	12	13	14
CHIP CARRIER PIN OUTS	2	4	5	6	7	9	10	12	14	15	16	17	19	20

FIGURE 3(b) - TRUTH TABLE

TRUTH TABLE EACH GATE				
INPUT				OUTPUTS
A	B	C	D	J
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

NOTES

1. Logic Level Definitions: L = Low Level, H = High Level, X = Don't Care.

FIGURE 3(c) - CIRCUIT SCHEMATIC (EACH GATE)

V_{DD}
14
p
2 (12)
n
p
p
3 (11)
n
p
p
p
4 (10)
n
p
p
5 (9)
n
p
n
n
n
n
n
1 (13)
V_{SS}
7

FIGURE 3(d) - FUNCTIONAL DIAGRAM (EACH GATE)

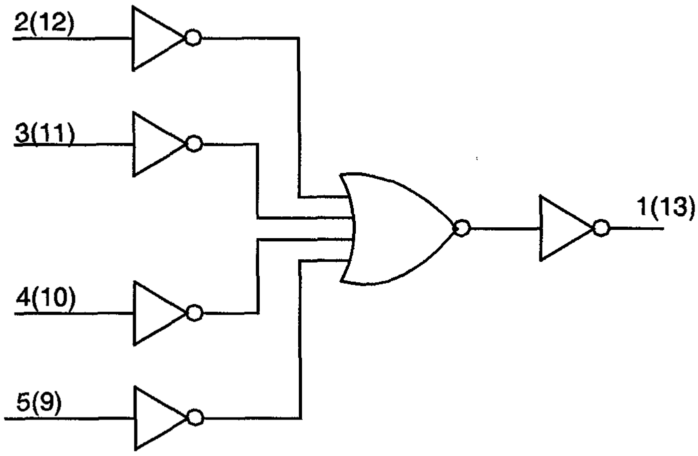
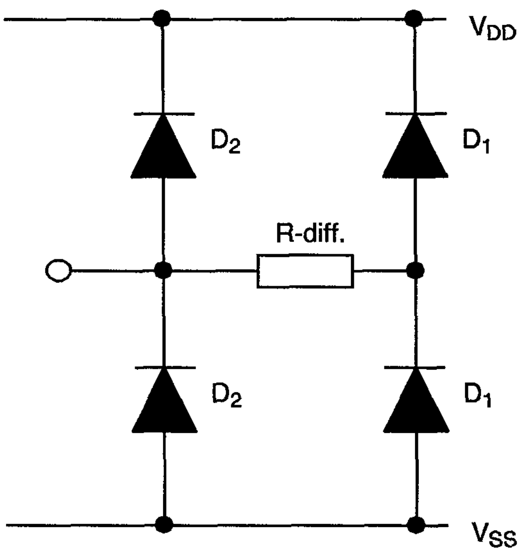


FIGURE 3(e) - INPUT PROTECTION NETWORK



2. APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:-

(a) ESA/SCC Generic Specification No. 9000 for Integrated Circuits.

(b) MIL-STD-883, Test Methods and Procedures for Micro-electronics.

3. TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESA/SCC Basic Specification No. 21300 shall apply. In addition, the following abbreviations are used:

V_{IC} = Input Clamp Voltage
P_{DSO} = Single Output Power Dissipation
CKT = Circuit

4. REQUIREMENTS

4.1 GENERAL

The complete requirements for procurement of the integrated circuits specified herein are stated in this specification and ESA/SCC Generic Specification No. 9000 for Integrated Circuits. Deviations from the Generic Specification, applicable to this Specification only, are listed in Para. 4.2.

Deviations from the applicable Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalant to the ESA/SCC requirements and do not affect the components' reliability, are listed in the appendices attached to this specification.

4.2 DEVIATIONS FROM GENERIC SPECIFICATION

4.2.1 Deviations from Special In-process Controls

None.

4.2.2 Deviations from Final Production Tests (Chart II)

None.

4.2.3 Deviations from Burn-in Tests (Chart III)

4.2.3.1 Deviations from High Temperature Reverse Bias (H.T.R.B.)

Prior to operating power burn-in, a high temperature reverse bias (H.T.R.B.) screen at +125°C shall be added for the N-Channel and then for the P-Channel in accordance with Tables 5(a) and 5(b) of this specification. Each exposure to H.T.R.B. shall be 72 hours and Table 4 Parameter Drift Values shall be applied at 0 and 144 hours.

4.2.4 Deviations from Qualification Tests (Chart IV)

None.

4.2.5 Deviations from Lot Acceptance Tests (Chart V)

None.

4.3 MECHANICAL REQUIREMENTS

4.3.1 Dimension Check

The dimensions of the integrated circuits specified herein shall be checked. They shall conform to those shown in Figure 2.

4.3.2 Weight

The maximum weight of the integrated circuits specified herein shall be 1.34 grammes for the dual-in-line package, 0.58 grammes for the flat and SO packages and 0.52 grammes for the chip carrier package.

4.4 MATERIALS AND FINISHES

The materials shall be as specified herein. Where a definite material is not specified, a material which will enable the integrated circuits specified herein to meet the performance requirements of this specification shall be used. Acceptance or approval of any constituent material does not guarantee acceptance of the finished product.

4.4.1 Case

The case shall be hermetically sealed and have a metal body with hard glass seals or a ceramic body and the lids shall be welded, brazed or preform-soldered.

4.4.2 Lead Material and Finish

For dual-in-line and flat packages, the material shall be Type 'G' with either Type '4' or Type '2 or 8' finish in accordance with ESA/SCC Basic Specification No. 23500. For chip carrier packages the finish shall be Type '2' in accordance with ESA/SCC Basic Specification No. 23500. For SO ceramic packages, the material shall be Type 'G' with either Type '2' or Type '4' finish in accordance with ESA/SCC Basic Specification No. 23500. (See Table 1(a) for Type Variants).

4.5 MARKING

4.5.1 General

The marking of all components delivered to this specification shall be in accordance with the requirements of ESA/SCC Basic Specification No. 21700. Each component shall be marked in respect of:-

(a) Lead Identification.

(b) The SCC Component Number.

(c) Traceability Information.

4.5.2 Lead Identification

For dual-in-line, flat and SO packages, an index shall be located at the top of the package in the position defined in Note 1 to Figure 2 or, alternatively, a tab may be used to identify Pin No. 1. The pin numbering must be read with the index or tab on the left-hand side. For chip carrier packages, the index shall be as defined by Figure 2(c).

4.5.3 The SCC Component Number

Each component shall bear the SCC Component Number which shall be constituted and marked as follows:

920104401B

- Detail Specification Number — 9201044
- Type Variant, as applicable — 01
- Testing Level (B or C, as appropriate) — B

4.5.4 Traceability Information

Each component shall be marked in respect of traceability information in accordance with the requirements of ESA/SCC Basic Specification No. 21700.

4.6 ELECTRICAL MEASUREMENTS

4.6.1 Electrical Measurements at Room Temperature

The parameters to be measured in respect of electrical characteristics are scheduled in Table 2. Unless otherwise specified, the measurements shall be performed at T_{amb} = +22±3 °C.

4.6.2 Electrical Measurements at High and Low Temperatures

The parameters to be measured at high and low temperatures are scheduled in Table 3. The measurements shall be performed at T_{amb} = +125(+0-5) °C and -55(+5-0) °C respectively.

4.6.3 Circuits for Electrical Measurements

Circuits and functional test sequence for use in performing electrical measurements listed in Tables 2 and 3 of this specification are shown in Figure 4.

4.7 BURN-IN TESTS

4.7.1 Parameter Drift Values

The parameter drift values applicable to burn-in are specified in Table 4 of this specification. Unless otherwise stated, measurements shall be performed at +22±3 °C. The parameter drift values (Δ) applicable to the parameters scheduled, shall not be exceeded. In addition to these drift value requirements, the appropriate limit value specified for a given parameter in Table 2 shall not be exceeded.

4.7.2 Conditions for H.T.R.B. and Burn-in

The requirements for H.T.R.B. and Burn-in are specified in Section 7 of ESA/SCC Generic Specification No. 9000. The conditions for H.T.R.B. and Burn-in shall be as specified in Tables 5(a), 5(b) and 5(c) of this specification.

4.7.3 Electrical Circuits for H.T.R.B and Burn-in

Circuits for use in performing the H.T.R.B. and Burn-in tests are shown in Figures 5(a), 5(b) and 5(c) of this specification.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS

NO.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
1	Functional Test	-	-	4(a)	Verify Truth Table without Load. V_{DD} = 3Vdc, V_{SS} = 0Vdc Notes 1 and 2	-	-	-
2	Functional Test	-	-	4(a)	Verify Truth Table without Load. V_{DD} = 15Vdc, V_{SS} = 0Vdc Notes 1 and 2	-	-	-
3 to 4	Quiescent Current	I_{DD}	3005	4(b)	V_{IL} = 0Vdc, V_{IH} = 15Vdc V_{DD} = 15Vdc, V_{SS} = 0Vdc Note 3 (Pin D/F 14) (Pin C 20)	-	100	nA
5 to 12	Input Current Low Level	I_{IL}	3009	4(c)	V_{IN} (Under Test) = 0Vdc V_{IN} (Remaining Inputs) = 15Vdc V_{DD} = 15Vdc, V_{SS} = 0Vdc (Pins D/F 2-3-4-5-9-10-11-12) (Pins C 4-5-6-7-14-15-16-17)	-	-50	nA
13 to 20	Input Current High Level	I_{IH}	3010	4(d)	V_{IN} (Under Test) = 15Vdc V_{IN} (Remaining Inputs) = 0Vdc V_{DD} = 15Vdc, V_{SS} = 0Vdc (Pins D/F 2-3-4-5-9-10-11-12) (Pins C 4-5-6-7-14-15-16-17)	-	50	nA
21 to 22	Output Voltage Low Level	V_{OL}	3007	4(e)	Gate Under Test: V_{IN} (All Inputs) = 15Vdc V_{OUT} = Open Other Gate: V_{IN} = 0Vdc V_{DD} = 15Vdc, V_{SS} = 0Vdc (Pins D/F 1-13) (Pins C 2-19)	-	0.05	V

NOTES: See Page 23.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS (CONT'D)

NO.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
23 to 30	Output Voltage High Level	V_{OH}	3006	4(f)	Gate Under Test: V_{IN1} = 0Vdc, $V_{IN2} = V_{IN3} = V_{IN4}$ = 15Vdc (V_{IN2} = 0Vdc, $V_{IN1} = V_{IN3} = V_{IN4}$ = 15Vdc) (V_{IN3} = 0Vdc, $V_{IN1} = V_{IN2} = V_{IN4}$ = 15Vdc) (V_{IN4} = 0Vdc, $V_{IN1} = V_{IN2} = V_{IN3}$ = 15Vdc) Other Gate: V_{IN} = 0Vdc V_{DD} = 15Vdc, V_{SS} = 0Vdc (Pins D/F 1-13) (Pins C 2-19)	14.95	-	V
31 to 32	Output Drive Current N-Channel	I_{OL1}	-	4(g)	Gate Under Test: V_{IN} (All Inputs) = 5Vdc V_{OUT} = 0.4Vdc Other Gate: V_{IN} = 0Vdc V_{DD} = 5Vdc, V_{SS} = 0Vdc Note 4 (Pins D/F 1-13) (Pins C 2-19)	0.51	-	mA
33 to 34	Output Drive Current N-Channel	I_{OL2}	-	4(g)	Gate Under Test: V_{IN} (All Inputs) = 15Vdc V_{OUT} = 1.5Vdc Other Gate: V_{IN} = 0Vdc V_{DD} = 15Vdc, V_{SS} = 0Vdc Note 4 (Pins D/F 1-13) (Pins C 2-19)	3.4	-	mA
35 to 42	Output Drive Current P-Channel	I_{OH1}	-	4(h)	Gate Under Test: $V_{IN1} = V_{IN2} = V_{IN3} =$ V_{IN4} = 0Vdc (V_{IN1} = 5Vdc, $V_{IN2} = V_{IN3} = V_{IN4}$ = 0Vdc) ($V_{IN1} = V_{IN2}$ = 5Vdc, $V_{IN3} = V_{IN4}$ = 0Vdc) ($V_{IN1} = V_{IN2} = V_{IN3}$ = 5Vdc, V_{IN4} = 0Vdc) V_{OUT} = 4.6Vdc Other Gate: V_{IN} = 0Vdc V_{DD} = 5Vdc, V_{SS} = 0Vdc Note 4 (Pins D/F 1-13) (Pins C 2-19)	-0.51	-	mA

NOTES: See Page 23.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS (CONT'D)

NO.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
43 to 50	Output Drive Current P-Channel	I_{OH2}	-	4(h)	Gate Under Test: V_{IN1} = V_{IN2} = V_{IN3} = V_{IN4} = 0Vdc (V_{IN1} = 15Vdc, V_{IN2} = V_{IN3} = V_{IN4} = 0Vdc) (V_{IN1} = V_{IN2} = 15Vdc, V_{IN3} = V_{IN4} = 0Vdc) (V_{IN1} = V_{IN2} = V_{IN3} = 15Vdc, V_{IN4} = 0Vdc) V_{OUT} = 13.5Vdc Other Gate: V_{IN} = 0Vdc V_{DD} = 15Vdc, V_{SS} = 0Vdc Note 4 (Pins D/F 1-13) (Pins C 2-19)	-3.4	-	mA
51 to 58	Input Voltage Low Level (Noise Immunity)	V_{IL1}	-	4(i)	Gate Under Test: V_{IN1} = 1.5Vdc, V_{IN2} = V_{IN3} = V_{IN4} = 3.5Vdc (V_{IN2} = 1.5Vdc, V_{IN1} = V_{IN3} = V_{IN4} = 3.5Vdc) (V_{IN3} = 1.5Vdc, V_{IN1} = V_{IN2} = V_{IN4} = 3.5Vdc) (V_{IN4} = 1.5Vdc, V_{IN1} = V_{IN2} = V_{IN3} = 3.5Vdc) Other Gate: V_{IN} = 5Vdc V_{DD} = 5 Vdc, V_{SS} = 0Vdc (Pins D/F 1-13) (Pins C 2-19)	4.5	-	V
59 to 66	Input Voltage Low Level (Noise Immunity)	V_{IL2}	--	4(i)	Gate Under Test: V_{IN1} = 4Vdc, V_{IN2} = V_{IN3} = V_{IN4} = 11Vdc (V_{IN2} = 4Vdc, V_{IN1} = V_{IN3} = V_{IN4} = 11Vdc) (V_{IN3} = 4Vdc V_{IN1} = V_{IN2} = V_{IN4} = 11Vdc) (V_{IN4} = 4Vdc, V_{IN1} = V_{IN2} = V_{IN3} = 11Vdc) Other Gate: V_{IN} = 15Vdc V_{DD} = 15 Vdc, V_{SS} = 0Vdc (Pins D/F 1-13) (Pins C 2-19)	13.5	-	V

NOTES: See Page 23.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS (CONT'D)

NO.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
67 to 68	Input Voltage High Level (Noise Immunity)	V_{IH1}	-	4(j)	Gate Under Test: V_{IN} (All Inputs) = 3.5Vdc Other Gate: V_{IN} = 0Vdc V_{DD} = 5Vdc, V_{SS} = 0Vdc (Pins D/F 1-13) (Pins C 2-19)	-	0.5	V
69 to 70	Input Voltage High Level (Noise Immunity)	V_{IH2}	-	4(j)	Gate Under Test: V_{IN} (All Inputs) = 11Vdc Other Gate: V_{IN} = 0Vdc V_{DD} = 15Vdc, V_{SS} = 0Vdc (Pins D/F 1-13) (Pins C 2-19)	-	1.5	V
71	Threshold Voltage N-Channel	V_{THN}	-	4(k)	A Input at Ground All Other Inputs: V_{IN} = 5Vdc V_{DD} = 5Vdc, I_{SS} = -10µA (Pin D/F 7) (Pin C 10)	-0.7	-3.0	V
72	Threshold Voltage P-Channel	V_{THP}	-	4(l)	A Input at Ground All Other Inputs: V_{IN} = -5Vdc V_{SS} = -5Vdc, I_{DD} = 10µA (Pin D/F 14) (Pin C 20)	0.7	3.0	V
73 to 80	Input Clamp Voltage (to V_{SS})	V_{IC1}	-	4(m)	I_{IN} (Under Test) = -100µA V_{DD} = Open, V_{SS} = 0Vdc All Other Pins Open (Pins D/F 2-3-4-5-9-10-11-12) (Pins C 4-5-6-7-14-15-16-17)	-	-2.0	V
81 to 88	Input ClampVoltage (to V_{DD})	V_{IC2}	-	4(n)	V_{IN} (Under Test) = 6Vdc V_{SS} = Open, R = 30KΩ; (Pins D/F 2-3-4-5-9-10-11-12) (Pins C 4-5-6-7-14-15-16-17)	3.0	-	V

NOTES: See Page 23.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS

NO.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
89 to 96	Input Capacitance	C_{IN}	3012	4(o)	V_{IN} (Not Under Test) = 0Vdc V_{DD} = V_{SS} = 0Vdc Note 5 (Pins D/F 2-3-4-5-9-10-11-12) (Pins C 4-5-6-7-14-15-16-17)	-	7.5	pF
97	Propagation Delay Low to High	t_{PLH}	3003	4(p)	V_{IN} (Under Test) = Pulse Generator V_{IN} (All Other Inputs) = 5Vdc V_{DD} = 5Vdc, V_{SS} = 0Vdc Note 6 Pins D/F: 2 to 1; Pins C: 4 to 2	-	200	ns
98	Propagation Delay High to Low	t_{PHL}	3003	4(p)	V_{IN} (Under Test) = Pulse Generator V_{IN} (All Other Inputs) = 5Vdc V_{DD} = 5Vdc, V_{SS} = 0Vdc Note 6 Pins D/F: 2 to 1; Pins C: 4 to 2	-	200	ns
99	Transition Time Low to High	t_{TLH}	3004	4(p)	V_{IN} (Under Test) = Pulse Generator V_{IN} (All Other Inputs) = 5Vdc V_{DD} = 5Vdc, V_{SS} = 0Vdc Note 6 (Pin D/F 1) (Pin C 2)	-	150	ns
100	Transition Time High to Low	t_{THL}	3004	4(p)	V_{IN} (Under Test) = Pulse Generator V_{IN} (All Other Inputs) = 5Vdc V_{DD} = 5Vdc, V_{SS} = 0Vdc Note 6 (Pin D/F 1) (Pins C 2)	-	150	ns

NOTES: See Page 23.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE (CONT'D)

NOTES

1. GO-NO-GO Test, each pattern of Test Table 4(a).
   $V_{OH} \geq V_{DD}$ - 0.5Vdc $V_{OL} \leq$ 0.5Vdc.
2. Maximum time to output comparator strobe 300μsec.
3. Test I_{DD} for the two input conditions given in Figure 4(b).
4. Interchange of forcing and measuring function is permitted.
5. Measurement performed on a sample basis LTPD 7, or less, with a Capacitance Bridge connected between each input under test and V_{SS}, only for Lots where LAT Level 2 is to be performed. (For LTPD sampling plan, see Annexe I of ESA/SCC 9000).
6. Measurement performed on a sample basis LTPD 7, or less (see Annexe I of ESA/SCC 9000).

TABLE 3(a) - ELECTRICAL MEASUREMENTS AT HIGH TEMPERATURE, +125(+0-5) °C

NO.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
1	Functional Test	-	-	4(a)	Verify Truth Table without Load. V_{DD} = 3Vdc, V_{SS} = 0Vdc Notes 1 and 2	-	-	-
2	Functional Test	-	-	4(a)	Verify Truth Table without Load. V_{DD} = 15Vdc, V_{SS} = 0Vdc Notes 1 and 2	-	-	-
3 to 4	Quiescent Current	I_{DD}	3005	4(b)	V_{IL} = 0Vdc, V_{IH} = 15Vdc V_{DD} = 15Vdc, V_{SS} = 0Vdc (Pin D/F 14) (Pin C 20)	-	1.0	µA
5 to 12	Input Current Low Level	I_{IL}	3009	4(c)	V_{IN} (Under Test) = 0Vdc V_{IN} (Remaining Inputs) = 15Vdc V_{DD} = 15Vdc, V_{SS} = 0Vdc (Pins D/F 2-3-4-5-9-10-11-12) (Pins C 4-5-6-7-14-15-16-17)	-	-100	nA
13 to 20	Input Current High Level	I_{IH}	3010	4(d)	V_{IN} (Under Test) = 15Vdc V_{IN} (Remaining Inputs) = 0Vdc V_{DD} = 15Vdc, V_{SS} = 0Vdc (Pins D/F 2-3-4-5-9-10-11-12) (Pins C 4-5-6-7-14-15-16-17)	-	100	nA
21 to 22	Output Voltage Low Level	V_{OL}	3007	4(e)	Gate Under Test: V_{IN} (All Inputs) = 15Vdc V_{OUT} = Open Other Gate: V_{IN} = 0Vdc V_{DD} = 15Vdc, V_{SS} = 0Vdc (Pins D/F 1-13) (Pins C 2-19)	-	0.05	V

NOTES: See Page 23.

TABLE 3(a) - ELECTRICAL MEASUREMENTS AT HIGH TEMPERATURE, +125(+0-5) °C (CONT'D)

NO.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
23 to 30	Output Voltage High Level	V_{OH}	3006	4(f)	Gate Under Test: V_{IN1} = 0Vdc, $V_{IN2} = V_{IN3} = V_{IN4}$ = 15Vdc (V_{IN2} = 0Vdc, $V_{IN1} = V_{IN3} = V_{IN4}$ = 15Vdc) (V_{IN3} = 0Vdc, $V_{IN1} = V_{IN2} = V_{IN4}$ = 15Vdc) (V_{IN4} = 0Vdc, $V_{IN1} = V_{IN2} = V_{IN3}$ = 15Vdc) Other Gate: V_{IN} = 0Vdc V_{DD} = 15Vdc, V_{SS} = 0Vdc (Pins D/F 1-13) (Pins C 2-19)	14.95	-	V
31 to 32	Output Drive Current N-Channel	I_{OL1}	-	4(g)	Gate Under Test: V_{IN} (All Inputs) = 5Vdc V_{OUT} = 0.4Vdc Other Gate: V_{IN} = 0Vdc V_{DD} = 5Vdc, V_{SS} = 0Vdc Note 4 (Pins D/F 1-13) (Pins C 2-19)	0.36	-	mA
33 to 34	Output Drive Current N-Channel	I_{OL2}	-	4(g)	Gate Under Test: V_{IN} (All Inputs) = 15Vdc V_{OUT} = 1.5Vdc Other Gate: V_{IN} = 0Vdc V_{DD} = 15Vdc, V_{SS} = 0Vdc Note 4 (Pins D/F 1-13) (Pins C 2-19)	2.4	-	mA
35 to 42	Output Drive Current P-Channel	I_{OH1}	-	4(h)	Gate Under Test: $V_{IN1} = V_{IN2} = V_{IN3} = V_{IN4}$ = 0Vdc (V_{IN1} = 5Vdc, $V_{IN2} = V_{IN3} = V_{IN4}$ = 0Vdc) ($V_{IN1} = V_{IN2}$ = 5Vdc, $V_{IN3} = V_{IN4}$ = 0Vdc) ($V_{IN1} = V_{IN2} = V_{IN3}$ = 5Vdc, V_{IN4} = 0Vdc) V_{OUT} = 4.6Vdc Other Gate: V_{IN} = 0Vdc V_{DD} = 5Vdc, V_{SS} = 0Vdc Note 4 (Pins D/F 1-13) (Pins C 2-19)	-0.36	-	mA

NOTES: See Page 23.

TABLE 3(a) - ELECTRICAL MEASUREMENTS AT HIGH TEMPERATURE, +125(+0-5) °C (CONT'D)

NO.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
43 to 50	Output Drive Current P-Channel	I_{OH2}	-	4(h)	Gate Under Test: $V_{IN1} = V_{IN2} = V_{IN3} = V_{IN4} = 0Vdc$ (V_{IN1} = 15Vdc, $V_{IN2} = V_{IN3} = V_{IN4} = 0Vdc$) ($V_{IN1} = V_{IN2} = 15Vdc$, $V_{IN3} = V_{IN4} = 0Vdc$) ($V_{IN1} = V_{IN2} = V_{IN3} = 15Vdc$, V_{IN4} = 0Vdc) V_{OUT} = 13.5Vdc Other Gate: V_{IN} = 0Vdc V_{DD} = 15Vdc, V_{SS} = 0Vdc Note 4 (Pins D/F 1-13) (Pins C 2-19)	-2.4	-	mA
51 to 58	Input Voltage Low Level (Noise Immunity)	V_{IL1}	-	4(i)	Gate Under Test: V_{IN1} = 1.5Vdc, $V_{IN2} = V_{IN3} = V_{IN4} = 3.5Vdc$ (V_{IN2} = 1.5Vdc, $V_{IN1} = V_{IN3} = V_{IN4} = 3.5Vdc$) ($V_{IN3}$ = 1.5Vdc, $V_{IN1} = V_{IN2} = V_{IN4} = 3.5Vdc$) ($V_{IN4}$ = 1.5Vdc, $V_{IN1} = V_{IN2} = V_{IN3} = 3.5Vdc$) Other Gate: V_{IN} = 5Vdc V_{DD} = 5Vdc, V_{SS} = 0Vdc (Pins D/F 1-13) (Pins C 2-19)	4.5	-	V
59 to 66	Input Voltage Low Level (Noise Immunity)	V_{IL2}	-	4(i)	Gate Under Test: V_{IN1} = 4Vdc, $V_{IN2} = V_{IN3} = V_{IN4} = 11Vdc$ (V_{IN2} = 4Vdc, $V_{IN1} = V_{IN3} = V_{IN4} = 11Vdc$) ($V_{IN3}$ = 4Vdc, $V_{IN1} = V_{IN2} = V_{IN4} = 11Vdc$) ($V_{IN4}$ = 4Vdc, $V_{IN1} = V_{IN2} = V_{IN3} = 11Vdc$) Other Gate: V_{IN} = 15Vdc V_{DD} = 15Vdc, V_{SS} = 0Vdc (Pins D/F 1-13) (Pins C 2-19)	13.5	-	V

NOTES: See Page 23.

TABLE 3(a) - ELECTRICAL MEASUREMENTS AT HIGH TEMPERATURE, +125(+0-5) °C (CONT'D)

NO.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
67 to 68	Input Voltage High Level (Noise Immunity)	V_{IH1}	-	4(j)	Gate Under Test: V_{IN} (All Inputs) = 3.5Vdc Other Gate: V_{IN} = 0Vdc V_{DD} = 5Vdc, V_{SS} = 0Vdc (Pins D/F 1-13) (Pins C 2-19)	-	0.5	V
69 to 70	Input Voltage High Level (Noise Immunity)	V_{IH2}	-	4(j)	Gate Under Test: V_{IN} (All Inputs) = 11Vdc Other Gate: V_{IN} = 0Vdc V_{DD} = 15Vdc, V_{SS} = 0Vdc (Pins D/F 1-13) (Pins C 2-19)	-	1.5	V
71	Threshold Voltage N-Channel	V_{THN}	-	4(k)	A input at Ground All other Inputs: V_{IN} = 5Vdc V_{DD} = 5Vdc, I_{SS} = -10μA (Pin D/F 7) (Pin C 10)	-0.3	-3.5	V
72	Threshold Voltage P-Channel	V_{THP}	-	4(l)	A input at Ground All other Inputs: V_{IN} = -5Vdc V_{SS} = -5Vdc, I_{DD} = 10μA (Pin D/F 14) (Pin C 20)	0.3	3.5	V

NOTES: See Page 23.

TABLE 3(b) - ELECTRICAL MEASUREMENTS AT LOW TEMPERATURE, -55(+5-0) °C

NO.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
1	Functional Test	-	-	4(a)	Verify Truth Table without Load. V_{DD} = 3V, V_{SS} = 0V Notes 1 and 2	-	-	-
2	Functional Test	-	-	4(a)	Verify Truth Table without Load. V_{DD} = 15V, V_{SS} = 0V Notes 1 and 2	-	-	-
3 to 4	Quiescent Current	I_{DD}	3005	4(b)	V_{IL} = 0Vdc, V_{IH} = 15Vdc V_{DD} = 15Vdc, V_{SS} = 0Vdc Note 3 (Pin D/F 14) (Pin C 20)	-	100	nA
5 to 12	Input Current Low Level	I_{IL}	3009	4(c)	V_{IN} (Under Test) = 0Vdc V_{IN} (Remaining Inputs) = 15Vdc V_{DD} = 15Vdc, V_{SS} = 0Vdc (Pins D/F 2-3-4-5-9-10-11-12) (Pins C 4-5-6-7-14-15-16-17)	-	-50	nA
13 to 20	Input Current High Level	I_{IH}	3010	4(d)	V_{IN} (Under Test) = 15Vdc V_{IN} (Remaining Inputs) = 0Vdc V_{DD} = 15Vdc, V_{SS} = 0Vdc (Pins D/F 2-3-4-5-9-10-11-12) (Pins C 4-5-6-7-14-15-16-17)	-	50	nA
21 to 22	Output Voltage Low Level	V_{OL}	3007	4(e)	Gate Under Test: V_{IN} (All Inputs) = 15Vdc V_{OUT} = Open Other Gate: V_{IN} = 0Vdc V_{DD} = 15Vdc, V_{SS} = 0Vdc (Pins D/F 1-13) (Pins C 2-19)	-	0.05	V

NOTES: See Page 23.

TABLE 3(b) - ELECTRICAL MEASUREMENTS AT LOW TEMPERATURE, -55(+5-0) °C (CONT'D)

NO.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
23 to 30	Output Voltage High Level	V_{OH}	3006	4(f)	Gate Under Test: V_{IN1} = 0Vdc, $V_{IN2} = V_{IN3} = V_{IN4}$ = 15Vdc (V_{IN2} = 0Vdc, $V_{IN1} = V_{IN3} = V_{IN4}$ = 15Vdc) (V_{IN3} = 0Vdc, $V_{IN1} = V_{IN2} = V_{IN4}$ = 15Vdc) (V_{IN4} = 0Vdc, $V_{IN1} = V_{IN2} = V_{IN3}$ = 15Vdc) Other Gate: V_{IN} = 0Vdc V_{DD} = 15Vdc, V_{SS} = 0Vdc (Pins D/F 1-13) (Pins C 2-19)	14.95	-	V
31 to 32	Output Drive Current N-Channel	I_{OL1}	-	4(g)	Gate Under Test: V_{IN} (All Inputs) = 5Vdc V_{OUT} = 0.4Vdc Other Gate: V_{IN} = 0Vdc V_{DD} = 5Vdc, V_{SS} = 0Vdc Note 4 (Pins D/F 1-13) (Pins C 2-19)	0.64	-	mA
33 to 34	Output Drive Current N-Channel	I_{OL2}	-	4(g)	Gate Under Test: V_{IN} (All Inputs) = 15Vdc V_{OUT} = 1.5Vdc Other Gate: V_{IN} = 0Vdc V_{DD} = 15Vdc, V_{SS} = 0Vdc Note 4 (Pins D/F 1-13) (Pins C 2-19)	4.2	-	mA
35 to 42	Output Drive Current P-Channel	I_{OH1}	-	4(h)	Gate Under Test: $V_{IN1} = V_{IN2} = V_{IN3} =$ V_{IN4} = 0Vdc (V_{IN1} = 5Vdc, $V_{IN2} = V_{IN3} = V_{IN4}$ = 0Vdc) ($V_{IN1} = V_{IN2}$ = 5Vdc, $V_{IN3} = V_{IN4}$ = 0Vdc) ($V_{IN1} = V_{IN2} = V_{IN3}$ = 5Vdc, V_{IN4} = 0Vdc) V_{OUT} = 4.6Vdc Other Gate: V_{IN} = 0Vdc V_{DD} = 5Vdc, V_{SS} = 0Vdc Note 4 (Pins D/F 1-13) (Pins C 2-19)	-0.64	-	mA

NOTES: See Page 23.

TABLE 3(b) - ELECTRICAL MEASUREMENTS AT LOW TEMPERATURE, -55(+5-0) °C (CONT'D)

NO.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
43 to 50	Output Drive Current P-Channel	I_{OH2}	-	4(h)	Gate Under Test: $V_{IN1} = V_{IN2} = V_{IN3} = V_{IN4} = 0Vdc$ (V_{IN1} = 15Vdc, $V_{IN2} = V_{IN3} = V_{IN4} = 0Vdc$) ($V_{IN1} = V_{IN2} = 15Vdc$, $V_{IN3} = V_{IN4} = 0Vdc$) ($V_{IN1} = V_{IN2} = V_{IN3} = 15Vdc$, V_{IN4} = 0Vdc) V_{OUT} = 13.5Vdc Other Gate: V_{IN} = 0Vdc V_{DD} = 15Vdc, V_{SS} = 0Vdc Note 4 (Pins D/F 1-13) (Pins C 2-19)	-4.2	-	mA
51 to 58	Input Voltage Low Level (Noise Immunity)	V_{IL1}	-	4(i)	Gate Under Test: V_{IN1} = 1.5Vdc, $V_{IN2} = V_{IN3} = V_{IN4} = 3.5Vdc$ (V_{IN2} = 1.5Vdc, $V_{IN1} = V_{IN3} = V_{IN4} = 3.5Vdc$) ($V_{IN3}$ = 1.5Vdc, $V_{IN1} = V_{IN2} = V_{IN4} = 3.5Vdc$) ($V_{IN4}$ = 1.5Vdc, $V_{IN1} = V_{IN2} = V_{IN3} = 3.5Vdc$) Other Gate: V_{IN} = 5Vdc V_{DD} = 5Vdc, V_{SS} = 0Vdc (Pins D/F 1-13) (Pins C 2-19)	4.5	-	V
59 to 66	Input Voltage Low Level (Noise Immunity)	V_{IL2}	-	4(i)	Gate Under Test: V_{IN1} = 4Vdc, $V_{IN2} = V_{IN3} = V_{IN4} = 11Vdc$ (V_{IN2} = 4Vdc, $V_{IN1} = V_{IN3} = V_{IN4} = 11Vdc$) ($V_{IN3}$ = 4Vdc, $V_{IN1} = V_{IN2} = V_{IN4} = 11Vdc$) ($V_{IN4}$ = 4Vdc, $V_{IN1} = V_{IN2} = V_{IN3} = 11Vdc$) Other Gate: V_{IN} = 15Vdc V_{DD} = 15Vdc, V_{SS} = 0Vdc (Pins D/F 1-13) (Pins C 2-19)	13.5	-	V

NOTES: See Page 23.

TABLE 3(b) - ELECTRICAL MEASUREMENTS AT LOW TEMPERATURE, -55(+5-0) °C (CONT'D)

NO.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS MIN	LIMITS MAX	UNIT
67 to 68	Input Voltage High Level (Noise Immunity)	V_{IH1}	-	4(j)	Gate Under Test: V_{IN} (All Inputs) = 3.5Vdc Other Gate: V_{IN} = 0Vdc V_{DD} = 5Vdc, V_{SS} = 0Vdc (Pins D/F 1-13) (Pins C 2-19)	-	0.5	V
69 to 70	Input Voltage High Level (Noise Immunity)	V_{IH2}	-	4(j)	Gate Under Test: V_{IN} (All Inputs) = 11Vdc Other Gate: V_{IN} = 0Vdc V_{DD} = 15Vdc, V_{SS} = 0Vdc (Pins D/F 1-13) (Pins C 2-19)	-	1.5	V
71	Threshold Voltage N-Channel	V_{THN}	-	4(k)	A input at Ground All other Inputs: V_{IN} = 5Vdc V_{DD} = 5Vdc, I_{SS} = -10μA (Pin D/F 7) (Pin C 10)	-0.7	-3.5	V
72	Threshold Voltage P-Channel	V_{THP}	-	4(l)	A input at Ground All other Inputs: V_{IN} = -5Vdc V_{SS} = -5Vdc, I_{SS} = 10μA (Pin D/F 14) (Pin C 20)	0.7	3.5	V

NOTES: See Page 23.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS

FIGURE 4(a) - FUNCTIONAL TEST TABLE

PATTERN NO.	PIN NUMBERS												D.C. SUPPLY	
	1	2	3	4	5	6	8	9	10	11	12	13	7	14
1	1	0	0	0	0	0	0	0	0	0	0	1	0	V_{DD}
2	0	1	1	1	1	0	0	0	0	0	0	1	↓	↓
3	1	0	1	1	1	0	0	1	1	1	1	0		
4	0	1	1	1	1	0	0	0	1	1	1	1		
5	1	1	0	1	1	0	0	1	1	1	1	0		
6	0	1	1	1	1	0	0	1	0	1	1	1		
7	1	1	1	0	1	0	0	1	1	1	1	0		
8	0	1	1	1	1	0	0	1	1	0	1	1		
9	1	1	1	1	0	0	0	1	1	1	1	0		
10	0	1	1	1	1	0	0	1	1	1	0	1		
11	1	0	0	0	0	0	0	1	1	1	1	0		

NOTES

1. Figure 4(a) illustrates one series of test patterns. Any other pattern series shall be agreed with the Qualifying Space Agency and shall be included as an Appendix.
2. Logic Level Definitions: $1 = V_{IH} = V_{DD}$, $0 = V_{IL} = V_{SS}$.

FIGURE 4(b) - QUIESCENT CURRENT

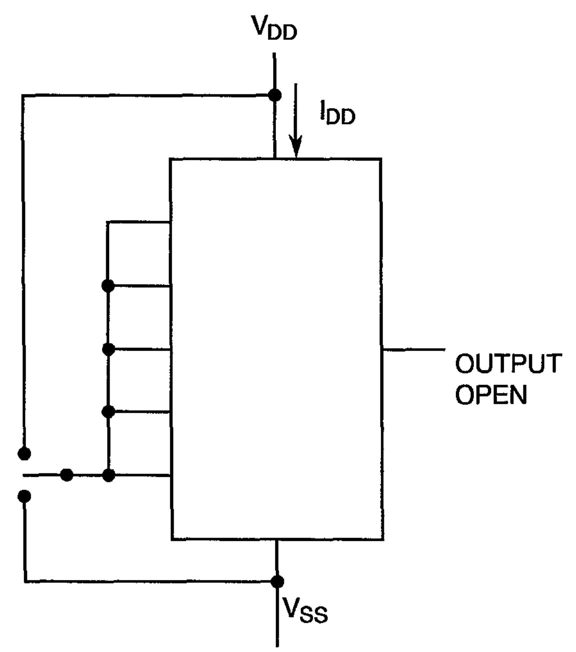
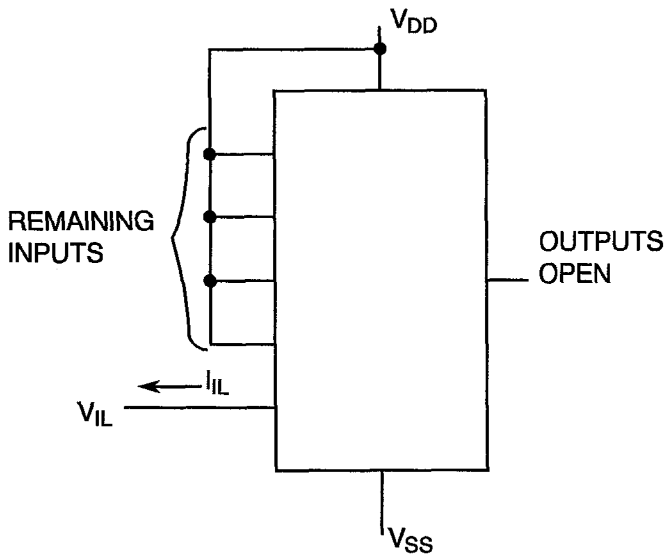


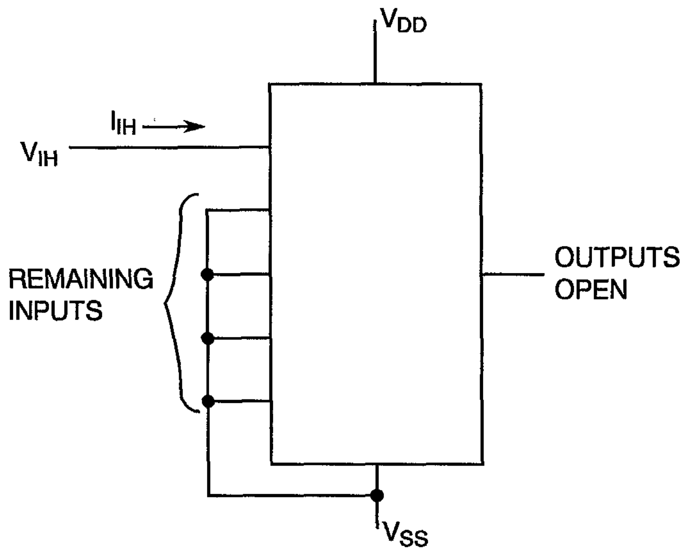
FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(c) - LOW LEVEL INPUT CURRENT



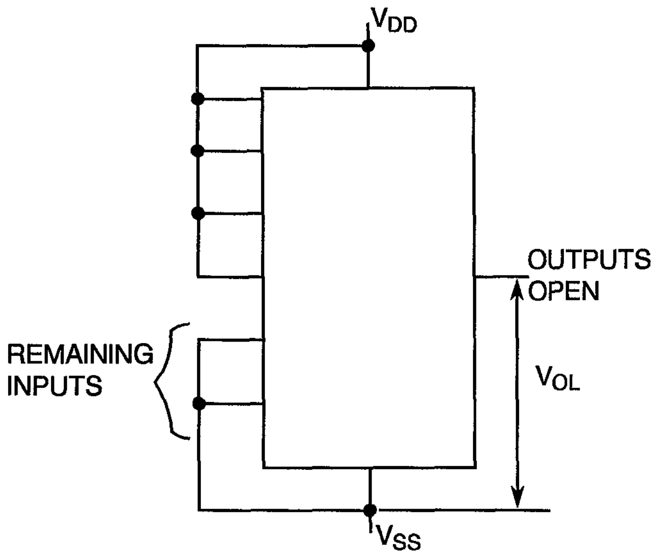
NOTES
1. Each input to be tested separately.

FIGURE 4(d) - HIGH LEVEL INPUT CURRENT



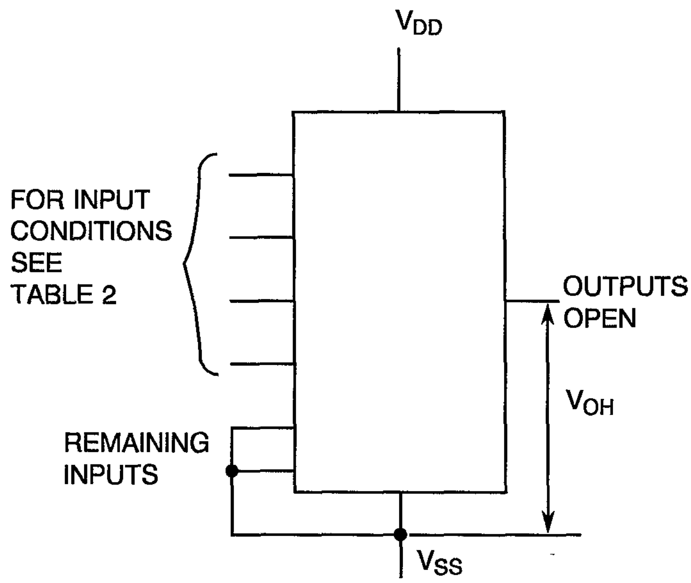
NOTES
1. Each input to be tested separately.

FIGURE 4(e) - LOW LEVEL OUTPUT VOLTAGE



NOTES
1. Each output to be tested separately.

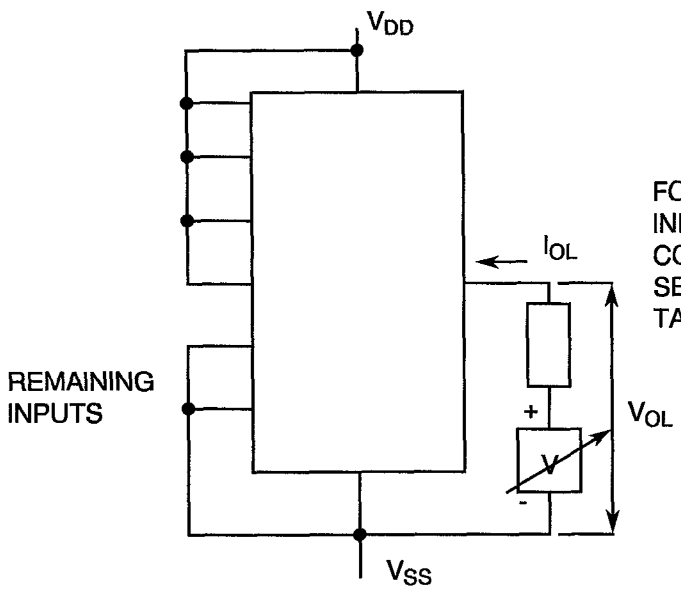
FIGURE 4(f) - HIGH LEVEL OUTPUT VOLTAGE



NOTES
1. Each output to be tested separately.

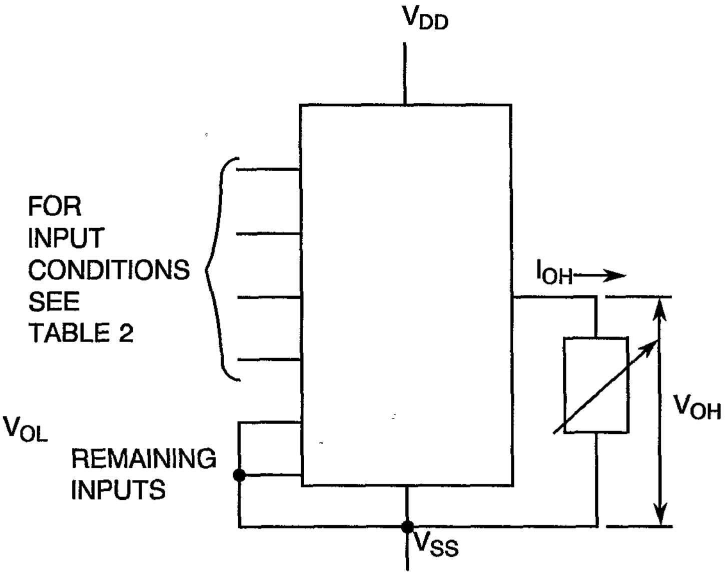
FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(g) - LOW LEVEL OUTPUT CURRENT



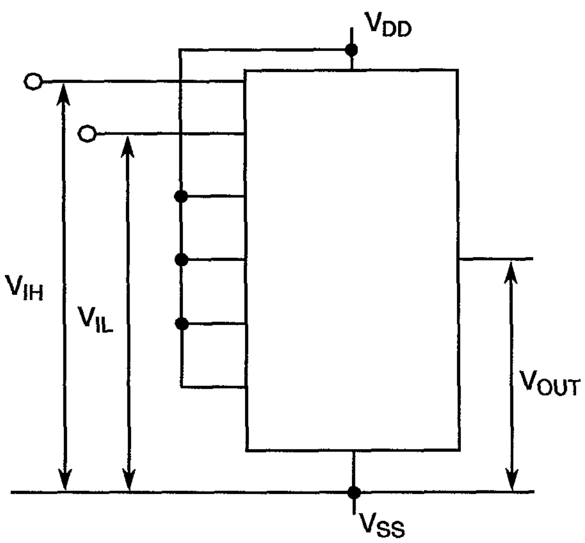
NOTES
1. Each output to be tested separately.

FIGURE 4(h) - HIGH LEVEL OUTPUT CURRENT



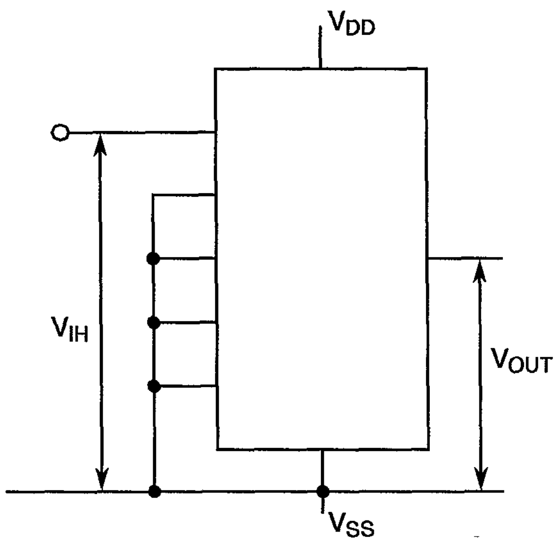
NOTES
1. Each output to be tested separately.

FIGURE 4(i) - LOW LEVEL INPUT VOLTAGE



NOTES
1. Each output to be tested separately.

FIGURE 4(j) - HIGH LEVEL INPUT VOLTAGE



NOTES
1. Each output to be tested separately.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(k) - THRESHOLD VOLTAGE N-CHANNEL

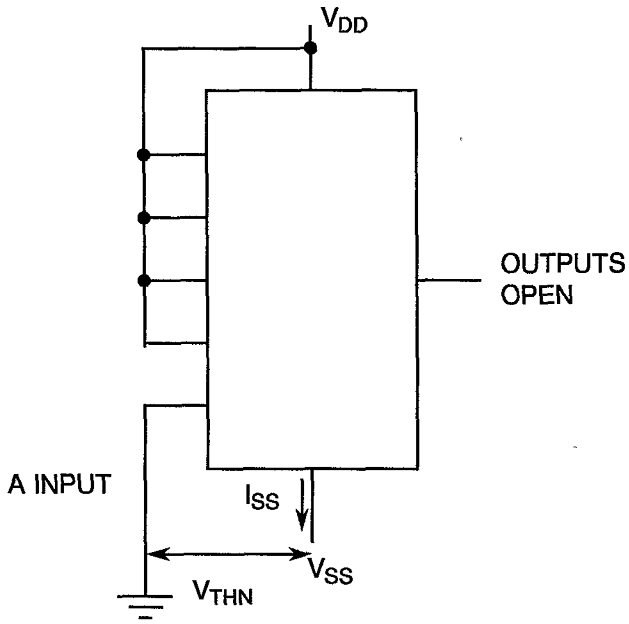


FIGURE 4(l) - THRESHOLD VOLTAGE P-CHANNEL

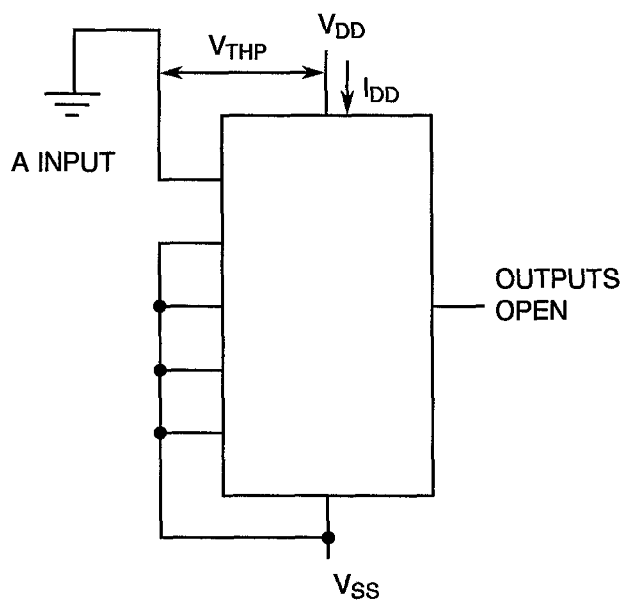
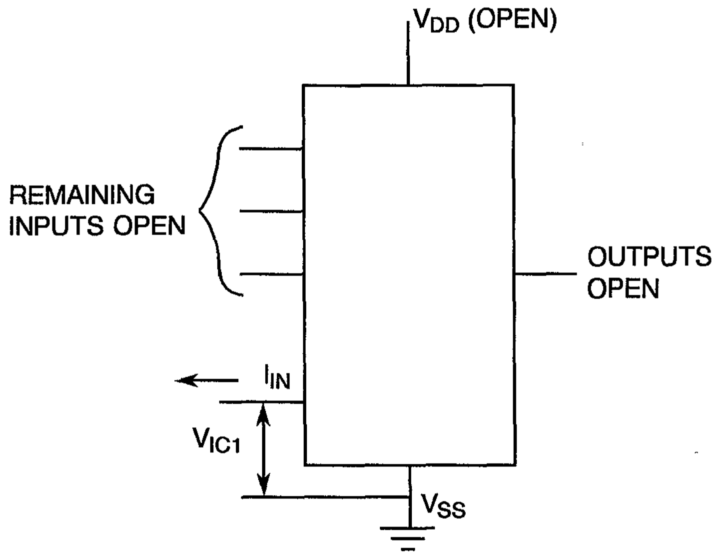


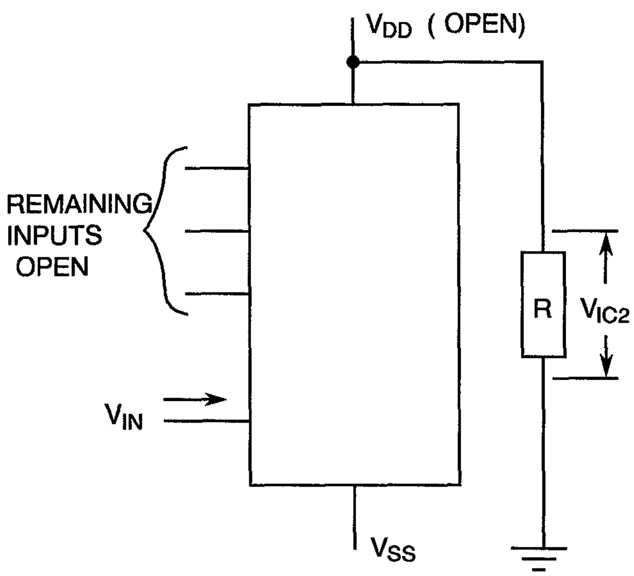
FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(m) - INPUT CLAMP VOLTAGE (V_{SS})



NOTES 1. Each input to be tested separately.

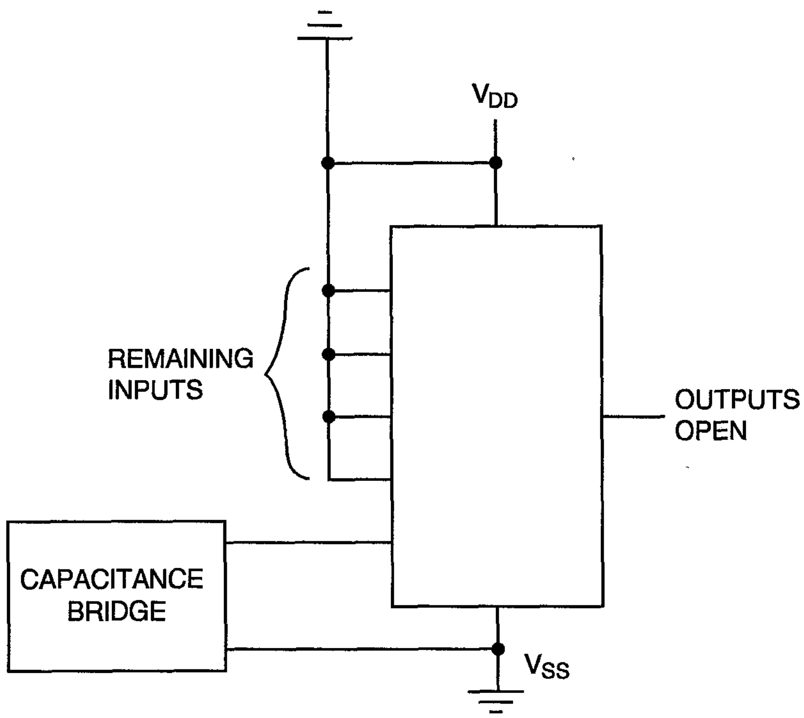
FIGURE 4(n) - INPUT CLAMP VOLTAGE (V_{DD})



NOTES 1. Each input to be tested separately.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

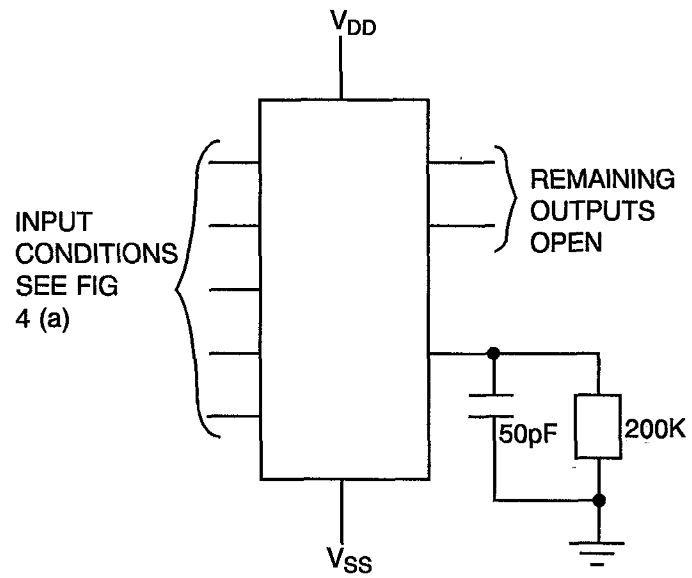
FIGURE 4(o) - INPUT CAPACITANCE



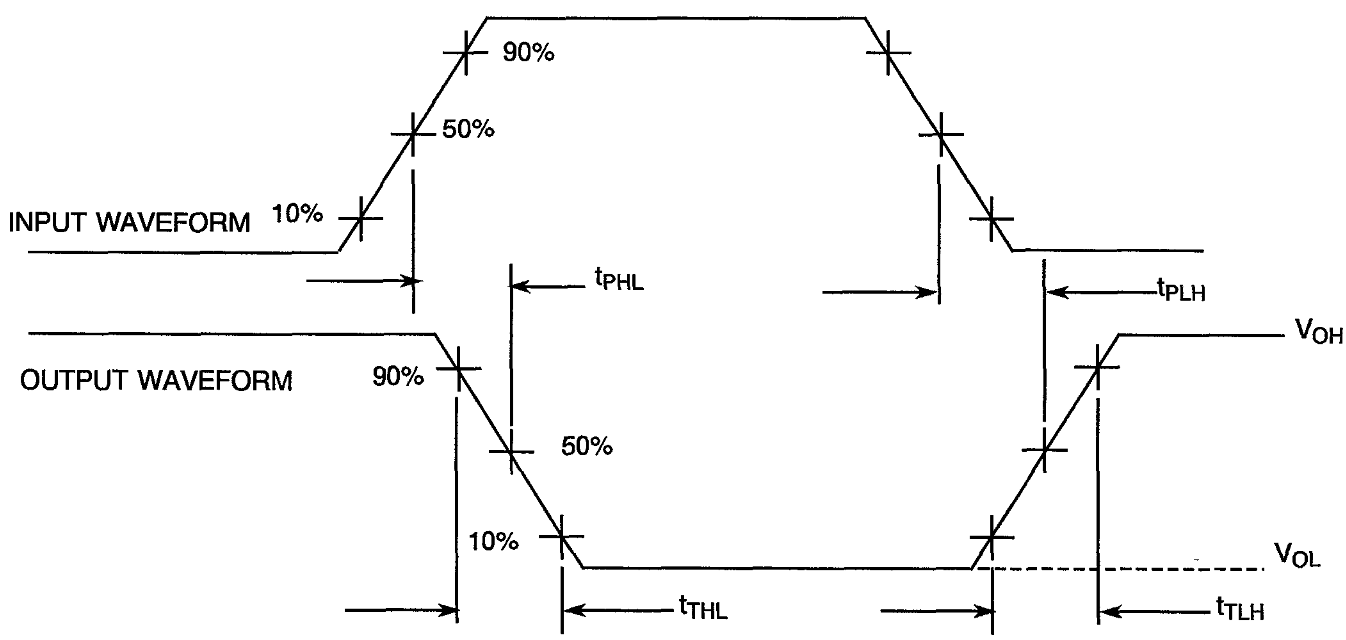
NOTES
1. Each input to be tested separately.
2. f = 100KHz to 1MHz

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(p) - PROPAGATION DELAY AND TRANSITION TIME



VOLTAGE WAVEFORMS



NOTES 1. Pulse Generator - V_P = 0 to V_{DD} , t_r and t_f $\leq$ 15ns, f = 500KHz.

TABLE 4 - PARAMETER DRIFT VALUES

NO.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	CHANGE LIMITS (Δ)	UNIT
3 to 4	Quiescent Current	I_{DD}	As per Table 2	As per Table 2	±50	nA
31 to 32	Output Drive Current N-Channel	I_{OL1}	As per Table 2	As per Table 2	±15 (1)	%
35 to 42	Output Drive Current P-Channel	I_{OH1}	As per Table 2	As per Table 2	±15 (1)	%
71	Threshold Voltage N-Channel	V_{THN}	As per Table 2	As per Table 2	±0.3	V
72	Threshold Voltage P-Channel	V_{THP}	As per Table 2	As per Table 2	±0.3	V

NOTES 1. Percentage of limit value if voltage is the measurement function.

TABLE 5(a) - CONDITIONS FOR BURN-IN HIGH TEMPERATURE REVERSE BIAS, N-CHANNELS

NO.	CHARACTERISTICS	SYMBOL	CONDITION	UNIT
1	Ambient Temperature	T_{amb}	+125(+0-5)	°C
2	Outputs - (Pins D/F 1-13) (Pins C 2-19)	V_{OUT}	Open	-
3	Inputs - (Pins D/F 2-3-4-5-9-10-11-12) (Pins C 4-5-6-7-14-15-16-17)	V_{IN}	Ground	Vdc
4	Positive Supply Voltage (Pin D/F 14) (Pin C 20)	V_{DD}	15	Vdc
5	Negative Supply Voltage (Pin D/F 7) (Pin C 10)	V_{SS}	Ground	Vdc

NOTES 1. Input Load = Protection Resistor = 2KΩ minimum to 47KΩ maximum.

TABLE 5(b) - CONDITIONS FOR BURN-IN HIGH TEMPERATURE REVERSE BIAS, P-CHANNELS

NO.	CHARACTERISTICS	SYMBOL	CONDITION	UNIT
1	Ambient Temperature	T_{amb}	+125(+0-5)	°C
2	Outputs - (Pins D/F 1-13) (Pins C 2-19)	V_{OUT}	Open	-
3	Inputs - (Pins D/F 2-3-4-5-9-10-11-12) (Pins C 4-5-6-7-14-15-16-17)	V_{IN}	V_{DD}	Vdc
4	Positive Supply Voltage (Pin D/F 14) (Pin C 20)	V_{DD}	15	Vdc
5	Negative Supply Voltage (Pin D/F 7) (Pin C 10)	V_{SS}	Ground	Vdc

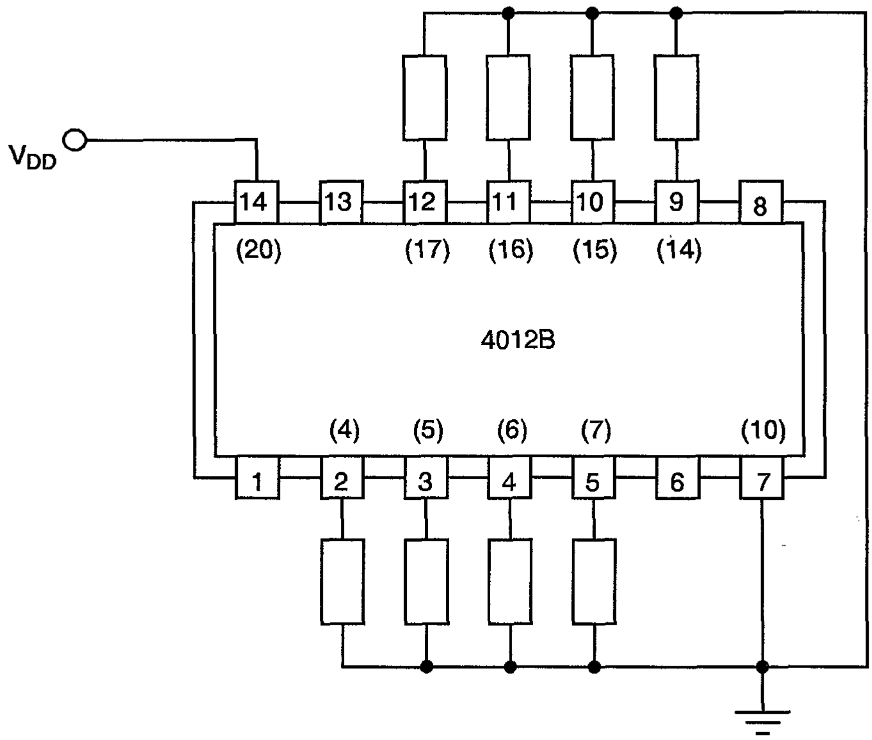
NOTES 1. Input Load = Protection Resistor = 2KΩ minimum to 47KΩ maximum.

TABLE 5(c) - CONDITIONS FOR BURN-IN DYNAMIC

NO.	CHARACTERISTICS	SYMBOL	CONDITIONS	UNIT
1	Ambient Temperature	T_{amb}	+125(+0-5)	°C
2	Outputs - (Pins D/F 1-13) (Pins C 2-19)	V_{OUT}	$V_{DD/2}$	Vdc
3	Inputs - (Pins D/F 2-3-4-5-9-10-11-12) (Pins C 4-5-6-7-14-15-16-17)	V_{IN}	V_{GEN}	Vac
4	Pulse Voltage	V_{GEN}	0V to V_{DD}	Vac
5	Pulse Frequency Square Wave	f	$50K \leq f < 1M$ 50% Duty Cycle	Hz
6	Positive Supply Voltage (Pin D/F 14) (Pin C 20)	V_{DD}	15	Vdc
7	Negative Supply Voltage (Pin D/F 7) (Pin C 10)	V_{SS}	Ground	Vdc

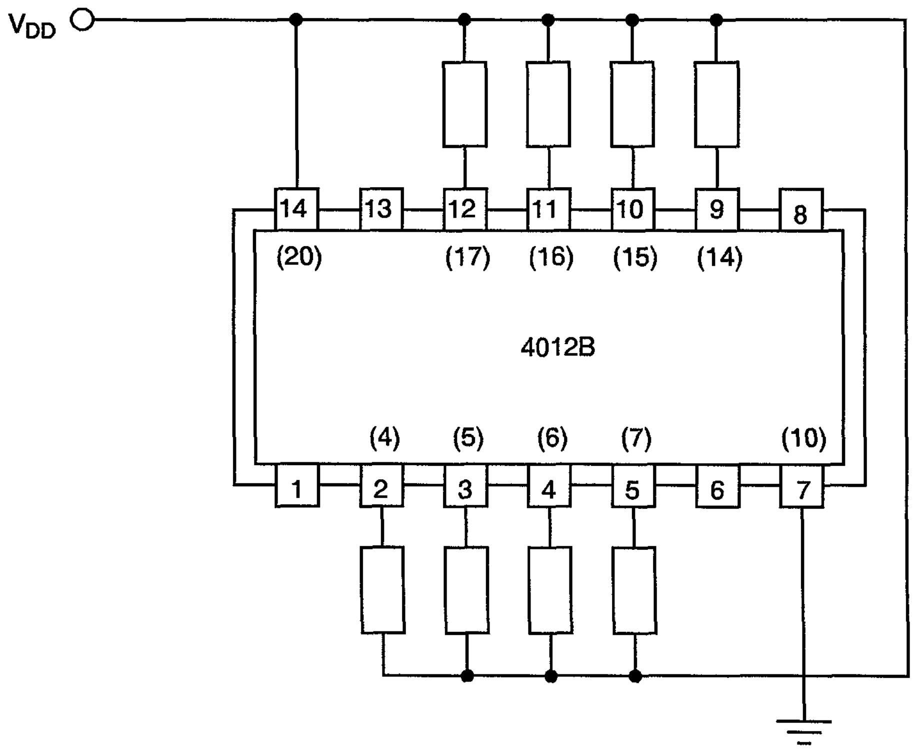
NOTES 1. Input Load = Output Load = 2KΩ minimum to 47KΩ maximum.

FIGURE 5(a) - ELECTRICAL CIRCUIT FOR BURN-IN HIGH TEMPERATURE REVERSE BIAS, N-CHANNELS



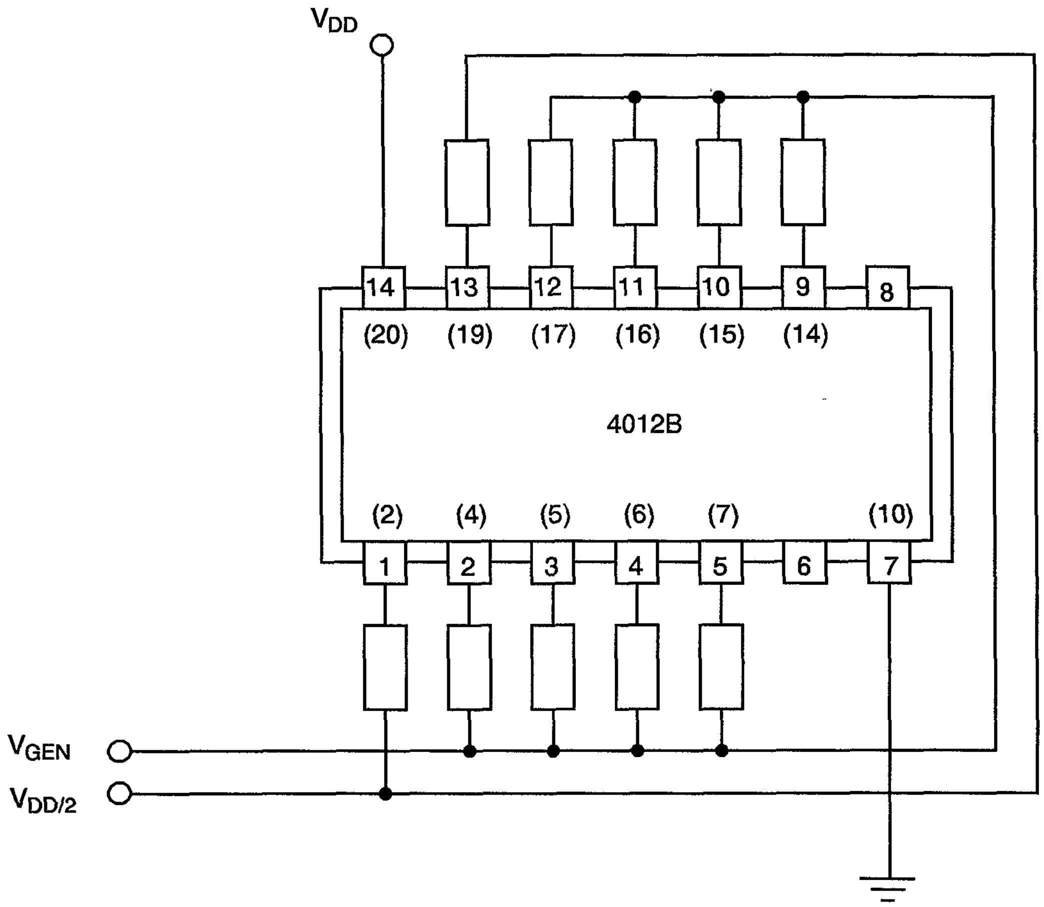
NOTES 1. Pin numbers in parenthesis are for the Chip Carrier Package.

FIGURE 5(b) - ELECTRICAL CIRCUIT FOR BURN-IN HIGH TEMPERATURE REVERSE BIAS, P-CHANNELS



NOTES 1. Pin numbers in parenthesis are for the Chip Carrier Package.

FIGURE 5(c) - ELECTRICAL CIRCUIT FOR BURN-IN DYNAMIC



NOTES 1. Pin numbers in parenthesis are for the Chip Carrier Package.

4.8 ENVIRONMENTAL AND ENDURANCE TESTS (CHARTS IV AND V OF ESA/SCC GENERIC SPECIFICATION NO. 9000)

4.8.1 Electrical Measurements on Completion of Environmental Tests

The parameters to be measured on completion of environmental tests are scheduled in Table 6. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.8.2 Electrical Measurements at Intermediate Points during Endurance Tests

The parameters to be measured at intermediate points during endurance tests are as scheduled in Table 6 of this specification.

4.8.3 Electrical Measurements on Completion of Endurance Tests

The parameters to be measured on completion of endurance testing are as scheduled in Table 6 of this specification. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +22 \pm 3$°C.

4.8.4 Conditions for Operating Life Test

The requirements for operating life testing are specified in Section 9 of ESA/SCC Generic Specification No. 9000. The conditions for operating life testing shall be as specified in Table 5(c) of this specification.

4.8.5 Electrical Circuits for Operating Life Tests

Circuits for use in performing the operating life tests are shown in Figure 5(c) of this specification.

4.8.6 Conditions for High Temperature Storage Test

The requirements for the high temperature storage test are specified in ESA/SCC Generic Specification No. 9000. The temperature to be applied shall be the maximum storage temperature specified in Table 1(b) of this specification.

TABLE 6 - ELECTRICAL MEASUREMENTS ON COMPLETION OF ENVIRONMENTAL TESTS AND AT INTERMEDIATE POINTS AND ON COMPLETION OF ENDURANCE TESTING

NO.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	CHANGE LIMITS (Δ)	MIN	MAX	UNIT
1	Functional Test	-	As per Table 2	As per Table 2	-	-	-	-
3 to 4	Quiescent Current	I_{DD}	As per Table 2	As per Table 2	±50	-	-	nA
5 to 12	Input Current Low Level	I_{IL}	As per Table 2	As per Table 2	-	-	-50	nA
13 to 20	Input Current High Level	I_{IH}	As per Table 2	As per Table 2	-	-	50	nA
21 to 22	Output Voltage Low Level	V_{OL}	As per Table 2	As per Table 2	-	-	0.05	V
23 to 30	Output Voltage High Level	V_{OH}	As per Table 2	As per Table 2	-	14.95	-	V
31 to 32	Output Drive Current N-Channel	I_{OL1}	As per Table 2	As per Table 2	±15 (1)	-	-	%
33 to 34	Output Drive Current N-Channel	I_{OL2}	As per Table 2	As per Table 2	±15 (1)	-	-	%
35 to 42	Output Drive Current P-Channel	I_{OH1}	As per Table 2	As per Table 2	±15 (1)	-	-	%
43 to 50	Output Drive Current P-Channel	I_{OH2}	As per Table 2	As per Table 2	±15 (1)	-	-	%
51 to 58	Input Voltage Low Level (Noise Immunity)	V_{IL1}	As per Table 2	As per Table 2	-	4.5	-	V
67 to 68	Input Voltage High Level (Noise Immunity)	V_{IH1}	As per Table 2	As per Table 2	-	-	0.5	V
71	Threshold Voltage N-Channel	V_{THN}	As per Table 2	As per Table 2	±0.3	-	-	V
72	Threshold Voltage P-Channel	V_{THP}	As per Table 2	As per Table 2	±0.3	-	-	V

NOTES 1. Percentage of limit value if voltage is the measurement.

APPENDIX 'A'

AGREED DEVIATIONS FOR STMICROELECTRONICS (F)

ITEMS AFFECTED	DESCRIPTION OF DEVIATION
Para. 4.2.3	Para. 9.23, High Temperature Reverse Bias Burn-in: The temperature limits of MIL-STD-883, Para. 4.5.8(c) may be used. Para. 9.24, Power Burn-in: The temperature limits of MIL-STD-883, Para. 4.5.8(c) may be used.
Para. 4.2.4	Para. 9.21.1, Operating Life during Qualification Testing: The temperature limits of MIL-STD-883, Para. 4.5.8(c) may be used.
Para. 4.2.5	Para. 9.21.2, Operating Life during Lot Acceptance Testing: The temperature limits of MIL-STD-883, Para. 4.5.8(c) may be used.