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INTEGRATED CIRCUITS, SILICON MONOLITHIC, CMOS

MICROPOWER PHASE-LOCKED LOOP

BASED ON TYPE 4046B

ESCC Detail Specification No. 9202/044

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DOCUMENTATION CHANGE NOTICE

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DCR No.	CHANGE DESCRIPTION
90	Specification up issued to incorporate editorial and technical changes per DCR.

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1. GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics and test and inspection data for the component type variants and/or the range of components specified below. It supplements the requirements of, and shall be read in conjunction with, the ESCC Generic Specification listed under Applicable Documents.

1.2 APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:

(a) ESCC Generic Specification No. 9000
(b) MIL-STD-883, Test Methods and Procedures for Microelectronics

1.3 TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESCC Basic Specification No. 21300 shall apply.

1.4 THE ESCC COMPONENT NUMBER AND COMPONENT TYPE VARIANTS

1.4.1 The ESCC Component Number

The ESCC Component Number shall be constituted as follows:

Example: 920204401

- Detail Specification Reference: 9202044
- Component Type Variant Number: 01 (as required)

1.4.2 Component Type Variants

The component type variants applicable to this specification are as follows:

Variant Number	Based on Type	Case	Terminal Material and /or Finish	Weight max g
01	4046B	FP	G2	0.7
02	4046B	FP	G4	0.7
07	4046B	CCP	2	0.6
08	4046B	DIP	G2	2.2
09	4046B	DIP	G4	2.2
10	4046B	SO	G2	0.7
11	4046B	SO	G4	0.7

The terminal material and/or finish shall be in accordance with the requirements of ESCC Basic Specification No. 23500.

1.5 MAXIMUM RATINGS

The maximum ratings shall not be exceeded at any time during use or storage.

Maximum ratings shall only be exceeded during testing to the extent specified in this specification and when stipulated in Test Methods and Procedures of the ESCC Generic Specification.

Characteristics	Symbols	Maximum Ratings	Units	Remarks
Supply Voltage	V_{DD}	-0.5 to 18	V	Note 1
Input Voltage	V_{IN}	-0.5 to V_{DD} +0.5	V	Note 1 Power on
Input Current	I_{IN}	±10	mA	-
Device Power Dissipation (Continuous)	P_D	200	mW	-
Power Dissipation per Output	P_{DSO}	100	mW	-
Operating Temperature Range	T_{op}	-55 to +125	°C	T_{amb}
Storage Temperature Range	T_{stg}	-65 to +150	°C	-
Soldering Temperature For FP, DIP and SO For CCP	T_{sol}	 +265 +245	°C	 Note 2 Note 3

NOTES:

1. Device is functional for $3V \leq V_{DD} \leq 15V$.
2. Duration 10 seconds maximum at a distance of not less than 1.5mm from the device body and the same terminal shall not be resoldered until 3 minutes have elapsed.
3. Duration 5 seconds maximum and the same terminal shall not be resoldered until 3 minutes have elapsed.

1.6 HANDLING PRECAUTIONS

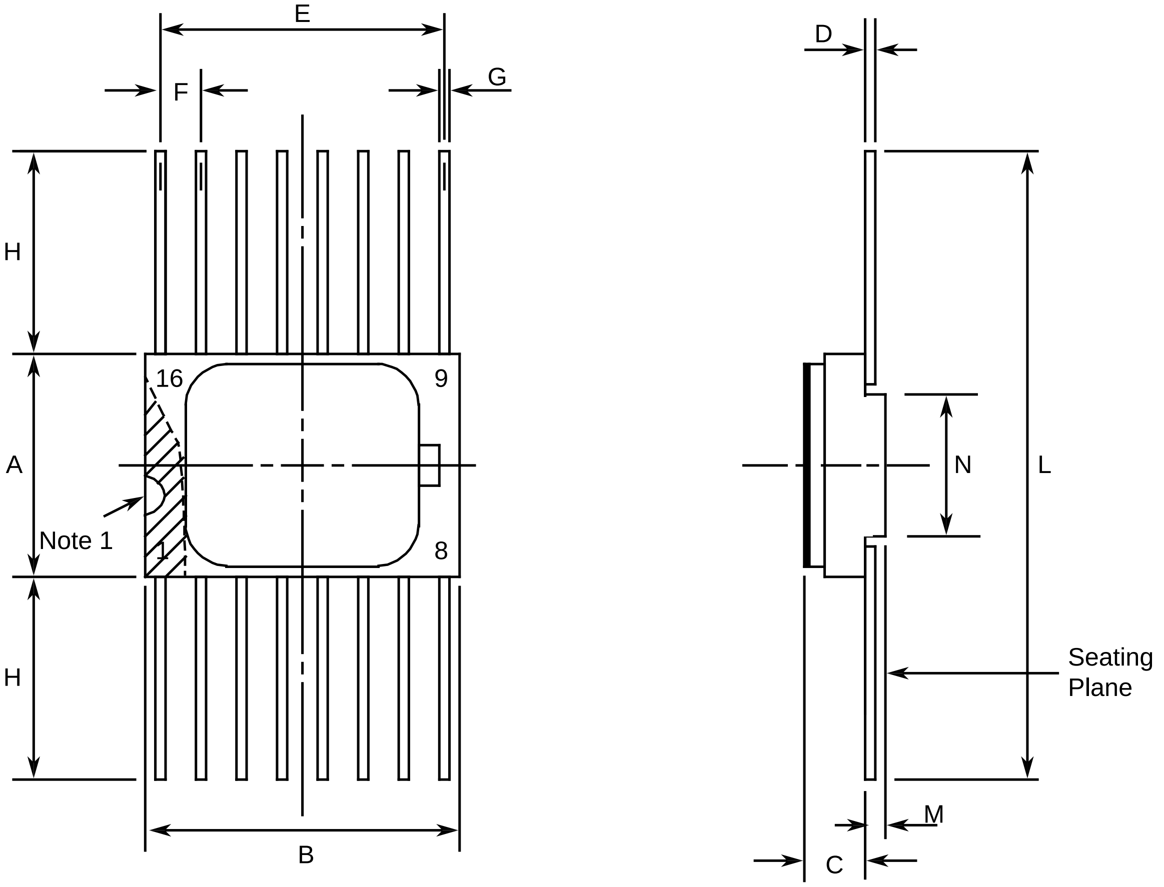
These devices are susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacture, testing, packaging, shipment and any handling.

These components are categorised as Class 1 per ESCC Basic Specification No. 23800 with a minimum Critical Path Failure Voltage of 400 Volts.

1.7 PHYSICAL DIMENSIONS AND TERMINAL IDENTIFICATION

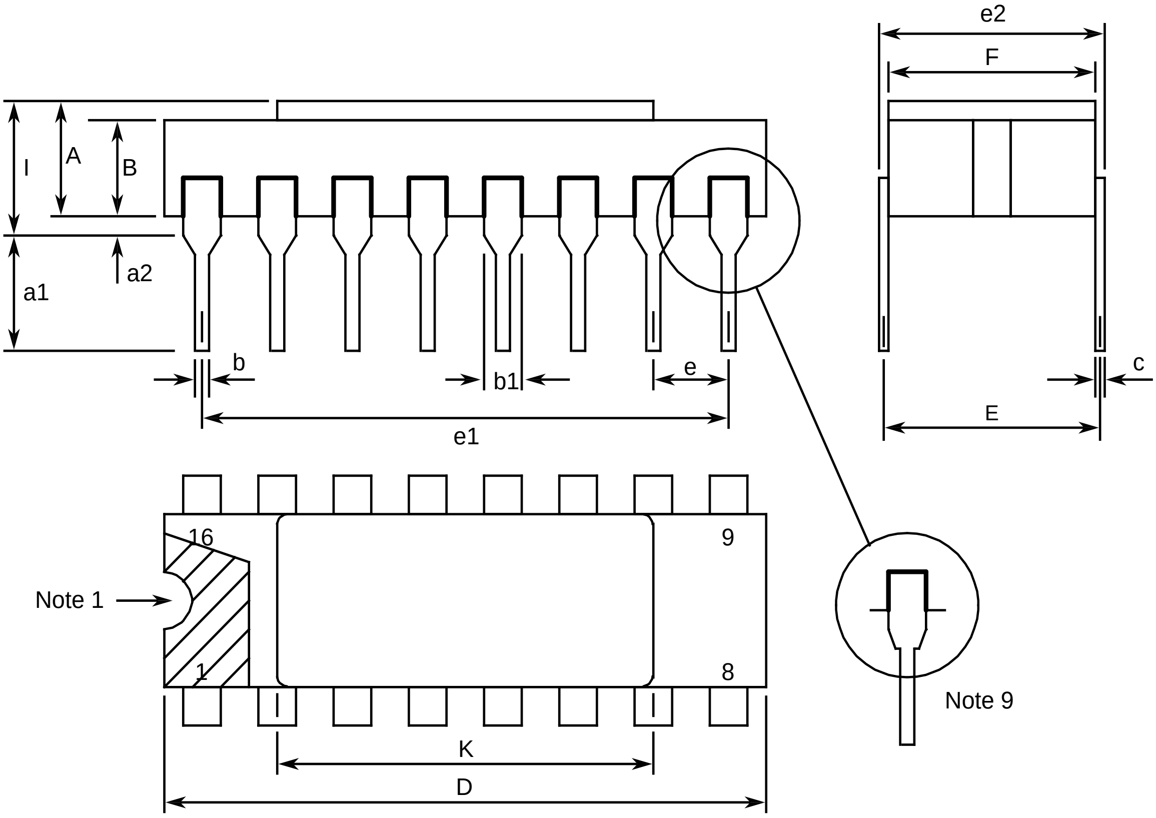
Consolidated Notes are given following the case drawings and dimensions.

1.7.1 Flat Package (FP) - 16 Pin



Symbols	Dimensions mm		Notes
	Min	Max	
A	6.75	7.06	
B	9.76	10.14	
C	1.49	1.95	
D	0.1	0.15	5
E	8.76	9.01	
F	1.27 TYPICAL		3, 6
G	0.38	0.48	5
H	6	-	5
L	18.75	22	
M	0.33	0.43	
N	4.32 TYPICAL		

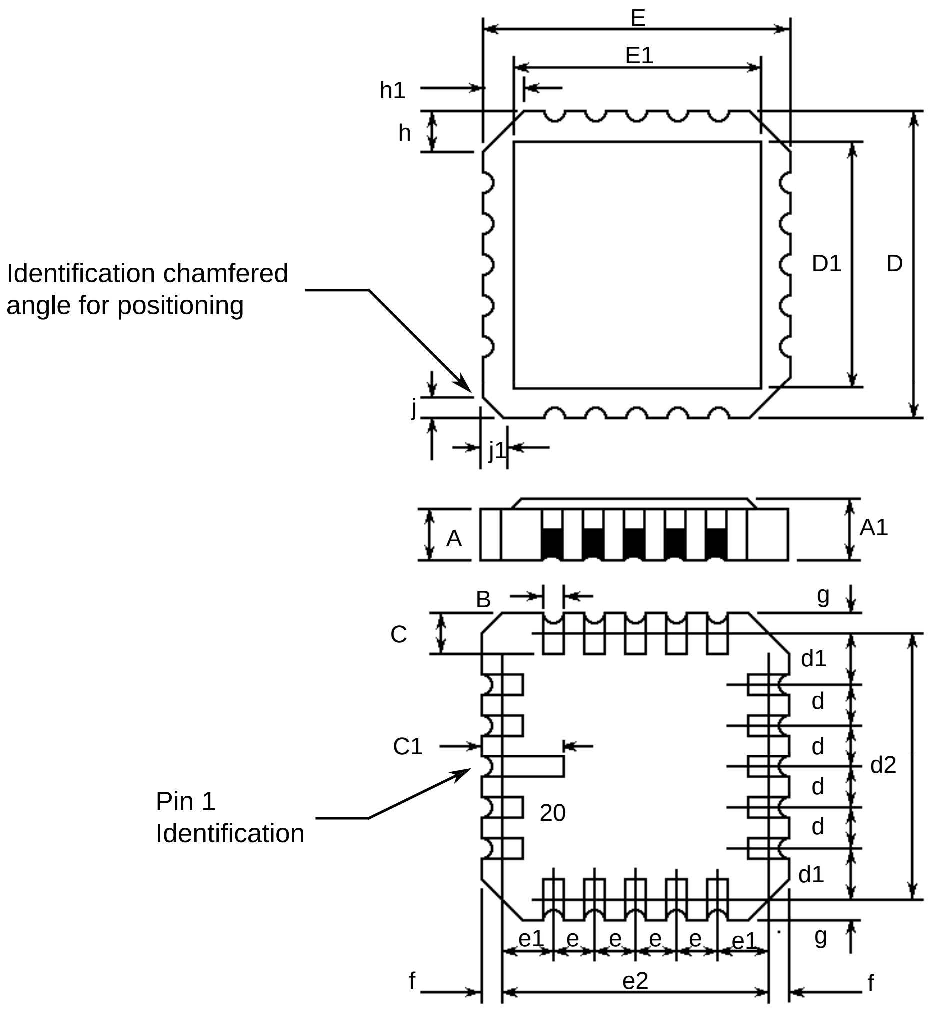
1.7.2 Dual-in-line Package (DIP) - 16 Pin



Symbols	Dimensions mm		Notes
	Min	Max	
A	2.1	2.71	
a1	3	3.7	
a2	0.63	1.14	2
B	1.82	2.39	
b	0.4	0.5	5
b1	1.14	1.5	5
c	0.2	0.3	5
D	20.06	20.58	
E	7.36	7.87	
e	2.54 TYPICAL		4, 6
e1	17.65	17.9	
e2	7.62	8.12	
F	7.29	7.7	
I	-	3.83	

Symbols	Dimensions mm		Notes
	Min	Max	
K	10.9	12.1	

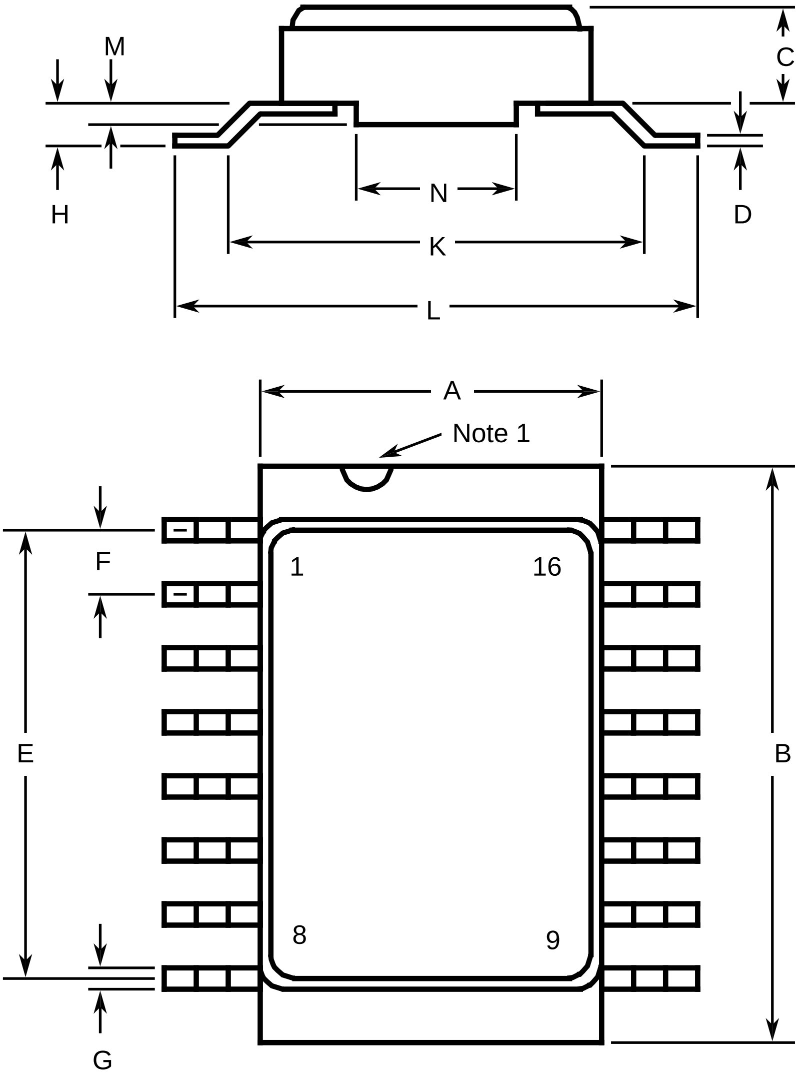
1.7.3 Chip Carrier Package (CCP) - 20 Terminal



Symbols	Dimensions mm		Notes
	Min	Max	
A	1.14	1.95	
A1	1.63	2.36	
B	0.55	0.72	5
C	1.06	1.47	5
C1	1.91	2.41	

Symbols	Dimensions mm		Notes
	Min	Max	
D	8.67	9.09	
D1	7.21	7.52	
d, d1	1.27 TYPICAL		3, 6
d2	7.62 TYPICAL		
E	8.67	9.09	
E1	7.21	7.52	
e, e1	1.27 TYPICAL		3, 6
e2	7.62 TYPICAL		
f, g	-	0.76	
h, h1	1.01 TYPICAL		8
j, j1	0.51 TYPICAL		7

1.7.4 Small Outline Ceramic Package (SO) - 16 Pin



Symbols	Dimensions mm		Notes
	Min	Max	
A	6.75	7.06	
B	9.76	10.14	
C	1.49	1.95	
D	0.1	0.15	5
E	8.76	9.01	
F	1.27 TYPICAL		3, 6
G	0.38	0.48	5
H	0.6	0.9	5

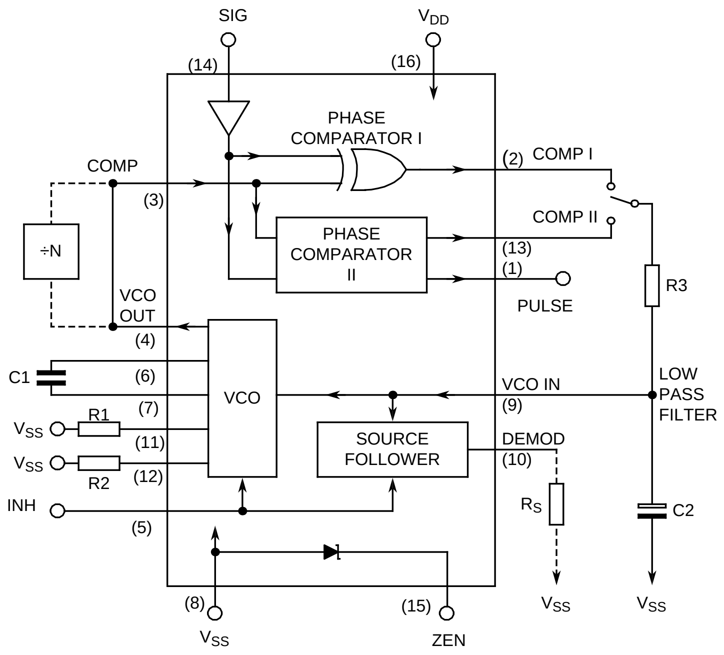
Symbols	Dimensions mm		Notes
	Min	Max	
K	9 TYPICAL		
L	10	10.65	
M	0.33	0.43	
N	4.31 TYPICAL		

1.7.5 Consolidated Notes

1. Index area; a notch or a dot shall be located adjacent to Pin 1 and shall be within the shaded area shown. For chip carrier packages, the index shall be as shown.
2. The dimension shall be measured from the seating plane to the base plane.
3. The true position pin spacing is 1.27mm between centrelines. Each pin centreline shall be located within ±0.13mm of its true longitudinal position relative to Pin 1 and the highest pin number.
4. The true position pin spacing is 2.54mm between centrelines. Each pin centreline shall be located within ±0.25mm of its true longitudinal position relative to Pin 1 and the highest pin number.
5. All terminals.
6. 14 spaces for flat, dual-in-line and small outline packages.
   16 spaces for chip carrier packages.
7. Index corner only - 2 dimensions.
8. 3 non-index corners - 6 dimensions.
9. For all pins, either pin shape may be supplied.

1.8 FUNCTIONAL DIAGRAM

Pin numbers relate to FP, DIP and SO packages only

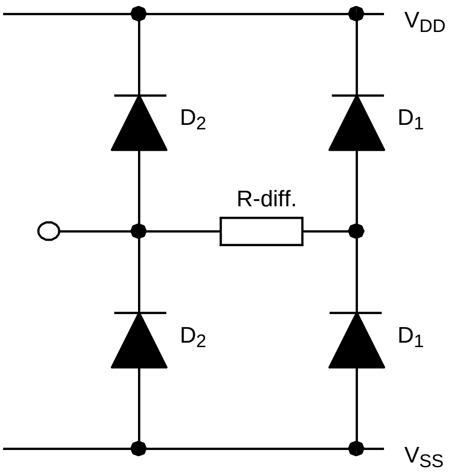


1.9 PIN ASSIGNMENT

Pin	Function		Pin	Function	
	FP, DIP and SO	CCP		FP, DIP and SO	CCP
1	PULSE Output (Phase Pulses)	PULSE Output (Phase Pulses)	11	R1 Input (Resistance to V_{SS})	VCO IN Input (Voltage-Controlled Oscillator)
2	COMP I Output (Phase Comparator I)	COMP I Output (Phase Comparator I)	12	R2 Input (Resistance to V_{SS})	DEMOD Output (Demodulator)
3	COMP Input (Phase Comparator)	-	13	COMP II Output (Phase Comparator II)	-
4	VCO OUT Output (Voltage-Controlled Oscillator)	COMP Input (Phase Comparator)	14	SIG Input (Signal)	R1 Input (Resistance to V_{SS})
5	INH Input (Inhibit)	VCO OUT Output (Voltage-Controlled Oscillator)	15	ZEN Output (Zener Diode)	R2 Input (Resistance to V_{SS})
6	1C1 Input/Output (Capacitor)	INH Input (Inhibit)	16	V_{DD}	COMP II Output (Phase Comparator II)
7	2C1 Input/Ouput (Capacitor)	1C1 Input/Output (Capacitor)	17	-	SIG Input (Signal)
8	V_{SS}	-	18	-	-
9	VCO IN Input (Voltage-Controlled Oscillator)	2C1 Input/Output (Capacitor)	19	-	ZEN Output (Zener Diode)
10	DEMOD Output (Demodulator)	V_{SS}	20	-	V_{DD}

1.10 INPUT PROTECTION NETWORK

Inputs COMP, VCO IN, INH and SIG shall incorporate double diode input protection as shown.



2. REQUIREMENTS

2.1 GENERAL

The complete requirements for procurement of the components specified herein are as stated in this specification and the ESCC Generic Specification. Permitted deviations from the Generic Specification, applicable to this specification only, are listed below.

Permitted deviations from the Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESCC requirement and do not affect the component's reliability, are listed in the appendices attached to this specification.

2.1.1 Deviations from the Generic Specification

None.

2.2 MARKING

The marking shall be in accordance with the requirements of ESCC Basic Specification No. 21700 and as follows.

The information to be marked on the component shall be:

(a) Terminal identification.
(b) The ESCC qualified components symbol (for ESCC qualified components only).
(c) The ESCC Component Number.
(d) Traceability information.

2.3 ELECTRICAL MEASUREMENTS AT ROOM, HIGH AND LOW TEMPERATURES

Electrical measurements shall be performed at room, high and low temperatures. Consolidated Notes are given after the tables.

2.3.1 Room Temperature Electrical Measurements

The measurements shall be performed at T_{amb}=+22 ±3°C.

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Functional Test 1	-	3014	V_{IL}=0V,V_{IH}=3V V_{DD}=3V,V_{SS}=0V Note 2	-	-	-
Functional Test 2	-	3014	V_{IL}=0V,V_{IH}=15V V_{DD}=15V,V_{SS}=0V Note 2	-	-	-
Quiescent Current	I_{DD}, I_{SS}	3005	V_{IL}=0V,V_{IH}=15V V_{DD}=15V,V_{SS}=0V Note 3	-	±80	µA
Low Level Input Current, COMP, INH, VCO IN, R2	I_{IL}	3009	V_{IN} (Under Test)=V_{IN}(SIG and 2C1)=0V V_{IN}(all other Inputs)=15V V_{DD}=15V,V_{SS}=0V	-	-100	nA
High Level Input Current, PULSE, INH, VCO IN, R2	I_{IH}	3010	V_{IN} (Under Test)=15V V_{IN}(all other Inputs)=0V V_{DD}=15V,V_{SS}=0V	-	100	nA
Low Level Output Voltage 1, PULSE, COMP I, VCO OUT, 1C1, 2C1, COMP II	V_{OL1}	3007	Input conditions per Note 4 V_{IN}(INH and R2)=15V V_{IN}(VCO IN and R1)=0V V_{DD}=15V, V_{SS}=0V	-	50	mV
Low Level Output Voltage 2 (Noise Immunity), PULSE, COMP I, VCO OUT, 1C1, 2C1, COMP II	V_{OL2}	3007	Input conditions per Note 4 V_{IL}=1.5V, V_{IH}=3.5V, I_{OL}=0A V_{DD}=5V, V_{SS}=0V	-	500	mV
Low Level Output Voltage 3 (Noise Immunity), PULSE, COMP I, VCO OUT, 1C1, 2C1, COMP II	V_{OL3}	3007	Input conditions per Note 4 V_{IL}=4V, V_{IH}=11V, I_{OL}=0A V_{DD}=15V, V_{SS}=0V	-	1.5	V
High Level Output Voltage 1, PULSE, COMP I, VCO OUT, COMP II	V_{OH1}	3006	Input Conditions per Note 5 V_{IN}(R2)=15V V_{IN}(VCO IN, INH, R1, 1C1 and 2C1)=0V V_{DD}=15V, V_{SS}=0V	14.95	-	V

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
High Level Output Voltage 2 (Noise Immunity), PULSE, COMP I, VCO OUT, 1C1, 2C1, COMP II	V_{OH2}	3006	Input Conditions per Note 5 V_{IL}=1.5V, V_{IH}=3.5V, I_{OH}=0A V_{DD}=5V, V_{SS}=0V	4.5	-	V
High Level Output Voltage 3 (Noise Immunity), PULSE, COMP I, VCO OUT, 1C1, 2C1, COMP II	V_{OH3}	3006	Input Conditions per Note 5 V_{IL}=4V, V_{IH}=11V, I_{OH}=0A V_{DD}=15V, V_{SS}=0V	13.5	-	V
Low Level Output Current 1, PULSE, COMP I, VCO OUT, 1C1, 2C1, COMP II	I_{OL1}	-	Input conditions per Note 4 V_{IN}(INH and R2)=5V V_{IN}(VCO IN and R1)=0V V_{OL}=0.4V V_{DD}=5V, V_{SS}=0V Note 7	510	-	µA
Low Level Output Current 2, PULSE, COMP I, VCO OUT, 1C1, 2C1, COMP II	I_{OL2}	-	Input conditions per Note 4 V_{IN}(INH and R2)=15V V_{IN}(VCO IN and R1)=0V V_{OL}=1.5V V_{DD}=15V, V_{SS}=0V Note 7	3.4	-	mA
High Level Output Current 1, PULSE, COMP I, VCO OUT, COMP II	I_{OH1}	-	Input conditions per Note 5 V_{IN}(R2)=5V V_{IN}(VCO IN, INH, R1, 1C1 and 2C1)=0V V_{OH}=4.6V V_{DD}=5V, V_{SS}=0V Note 7	-510	-	µA
High Level Output Current 2, PULSE, COMP I, VCO OUT, COMP II	I_{OH2}	-	Input conditions per Note 5 V_{IN}(R2)=15V V_{IN}(VCO IN, INH, R1, 1C1 and 2C1)=0V V_{OH}=13.5V V_{DD}=15V, V_{SS}=0V Note 7	-3.4	-	mA
Bias Leakage Current 1, V_{SS}	I_{LB1}	-	V_{IN}(COMP and VCO IN)=0V V_{IN}(INH and R2)=15V SIG=Open V_{DD}=15V, V_{SS}=0V	-	-1.5	mA

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Bias Leakage Current 2, SIG	I_{LB2}	-	V_{IN}(SIG, COMP and VCO IN)=0V V_{IN}(INH and R2)=15V V_{DD}=15V, V_{SS}=0V	-	-150	µA
Bias Leakage Current 3, SIG	I_{LB3}	-	V_{IN}(SIG, INH and R2)=15V V_{IN}(COMP and VCO IN)=0V V_{DD}=15V, V_{SS}=0V	-	150	µA
Threshold Voltage N-Channel, DEMOD	V_{THN}	-	V_{IN}(COMP, INH, 1C1, 2C1 and SIG)= V_{SS}=-5V I(DEMOD)=-10µA All Other Inputs: V_{IN}=V_{DD}=Ground	-0.7	-3	V
Threshold Voltage P-Channel, R2	V_{THP}	-	V_{DD} at Ground I(R2)=-10µA All Other Inputs: V_{IN}=V_{SS}=-5V	-0.7	-3	V
Output Leakage Current Third State, Low Level Applied, COMP II	I_{OZL}	3020	Input conditions per Note 6 V_{IN}(INH and R2)=15V V_{IN}(VCO IN)=0V V_{OL}=0V V_{DD}=15V, V_{SS}=0V	-	-400	nA
Output Leakage Current Third State, High Level Applied, COMP II	I_{OZH}	3021	Input conditions per Note 6 V_{IN}(INH and R2)=15V V_{IN}(VCO IN)=0V V_{OH}=15V V_{DD}=15V, V_{SS}=0V	-	400	nA
Zener Voltage	V_Z	-	I_Z=50µA	4.45	7.5	V
Input Clamp Voltage 1 (to V_{SS}), COMP, INH, 1C1, 2C1, VCO IN, R2, SIG	V_{IC1}	-	I_{IN} (Under Test)= -100µA V_{DD}=Open, V_{SS}=0V All Other Pins Open	-	-2	V
Input Clamp Voltage 2 (to V_{DD}), COMP, INH, 1C1, 2C1, VCO IN, R2, SIG	V_{IC2}	-	V_{IN} (Under Test)=6V R=30kΩ, V_{SS}=Open All Other Pins Open Note 8	3	-	V
Input Capacitance, COMP and INH	C_{IN1}	3012	V_{IN} (Not Under Test)=0V V_{DD}= V_{SS}=0V f = 100 kHz to 1 MHz Note 9	-	7.5	pF

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Input Capacitance, VCO IN	C_{IN2}	3012	V_{IN} (Not Under Test)=0V V_{DD}= V_{SS}=0V f = 100 kHz to 1 MHz Note 9	-	35	pF
Propagation Delay Low to High, COMP to COMP I	t_{PLH}	3003	V_{IN}(Under Test)=Pulse Generator V_{IN}(Remaining Inputs)=0V V_{IL}=0V, V_{IH}=5V V_{DD}=5V, V_{SS}=0V Note 10	-	650	ns
Propagation Delay High to Low, SIG to COMP I	t_{PHL}	3003	V_{IN}(Under Test)=Pulse Generator V_{IN} (Remaining Inputs)=0V V_{IL}=0V, V_{IH}=5V, V_{DD}=5V, V_{SS}=0V Note 10	-	400	ns
Output Enable Time High Impedance to Low Output, COMP to COMP II	t_{PZL}	3003	V_{IN}(Under Test)=Pulse Generator V_{IN} (Remaining Inputs)=0V V_{IL}=0V, V_{IH}=5V, V_{DD}=5V, V_{SS}=0V Note 10	-	550	ns
Output Disable Time Low Output to High Impedance, SIG to COMP II	t_{PLZ}	3003	V_{IN}(Under Test)=Pulse Generator V_{IN} (Remaining Inputs)=0V V_{IL}=0V, V_{IH}=5V, V_{DD}=5V, V_{SS}=0V Note 10	-	550	ns
Output Enable Time High Impedance to High Output, SIG to COMP II	t_{PZH}	3003	V_{IN}(Under Test)=Pulse Generator V_{IN} (Remaining Inputs)=0V V_{IL}=0V, V_{IH}=5V, V_{DD}=5V, V_{SS}=0V Note 10	-	420	ns
Output Disable Time High Output to High Impedance, COMP to COMP II	t_{PHZ}	3003	V_{IN}(Under Test)=Pulse Generator V_{IN} (Remaining Inputs)=0V V_{IL}=0V, V_{IH}=5V, V_{DD}=5V, V_{SS}=0V Note 10	-	420	ns

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Transition Time Low to High, COMP I	t_{TLH}	3004	V_{IN}(Under Test)=Pulse Generator V_{IN} (Remaining Inputs)=0V V_{IL}=0V, V_{IH}=5V, V_{DD}=5V, V_{SS}=0V Note 10	-	150	ns
Transition Time High to Low, COMP I	t_{THL}	3004	V_{IN}(Under Test)=Pulse Generator V_{IN} (Remaining Inputs)=0V V_{IL}=0V, V_{IH}=5V, V_{DD}=5V, V_{SS}=0V Note 10	-	150	ns
Maximum Output Frequency of VCO	f_{VCO}	-	R1=10kΩ, R2=OPEN, C1=50pF V_{IL}=0V, V_{IH}=5V, V_{DD}=5V, V_{SS}=0V Note 11	300	-	kHz

2.3.2 High and Low Temperatures Electrical Measurements

The measurements shall be performed at T_{amb}=+125 (+0 -5) ^{o}C and T_{amb}=- 55(+5-0)^{o}C.

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Functional Test 1	-	3014	V_{IL}=0V,V_{IH}=3V V_{DD}=3V,V_{SS}=0V Note 2	-	-	-
Functional Test 2	-	3014	V_{IL}=0V,V_{IH}=15V V_{DD}=15V,V_{SS}=0V Note 2	-	-	-
Quiescent Current	I_{DD}, I_{SS}	3005	V_{IL}=0V,V_{IH}=15V V_{DD}=15V,V_{SS}=0V Note 3 T_{amb}=+125^{o}C T_{amb}=- 55^{o}C	 - -	 ±2400 ±80	µA
Low Level Input Current, COMP, INH, VCO IN, R2	I_{IL}	3009	V_{IN} (Under Test)=V_{IN}(SIG and 2C1)=0V V_{IN}(all other Inputs)=15V V_{DD}=15V,V_{SS}=0V T_{amb}=+125^{o}C T_{amb}=- 55^{o}C	 - -	 -1000 -100	nA

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
High Level Input Current, COMP, INH, VCO IN, R2	I_{IH}	3010	V_{IN} (Under Test)=15V V_{IN}(all other Inputs)=0V V_{DD}=15V,V_{SS}=0V T_{amb}=+125°C T_{amb}=- 55°C	- -	1000 100	nA
Low Level Output Voltage 1, PULSE, COMP I, VCO OUT, 1C1, 2C1, COMP II	V_{OL1}	3007	Input conditions per Note 4 V_{IN}(INH and R2)=15V V_{IN}(VCO IN and R1)=0V V_{DD}=15V, V_{SS}=0V	-	50	mV
Low Level Output Voltage 2 (Noise Immunity), PULSE, COMP I, VCO OUT, 1C1, 2C1, COMP II	V_{OL2}	3007	Input conditions per Note 4 V_{IL}=1.5V, V_{IH}=3.5V, I_{OL}=0A V_{DD}=5V, V_{SS}=0V	-	500	mV
Low Level Output Voltage 3 (Noise Immunity), PULSE, COMP I, VCO OUT, 1C1, 2C1, COMP II	V_{OL3}	3007	Input conditions per Note 4 V_{IL}=4V, V_{IH}=11V, I_{OL}=0A V_{DD}=15V, V_{SS}=0V	-	1.5	V
High Level Output Voltage 1, PULSE, COMP I, VCO OUT, COMP II	V_{OH1}	3006	Input Conditions per Note 5 V_{IN}(R2)=15V V_{IN}(VCO IN, INH, R1, 1C1 and 2C1)=0V V_{DD}=15V, V_{SS}=0V	14.95	-	V
High Level Output Voltage 2 (Noise Immunity), PULSE, COMP I, VCO OUT, 1C1, 2C1, COMP II	V_{OH2}	3006	Input conditions per Note 5 V_{IL}=1.5V, V_{IH}=3.5V, I_{OH}=0A V_{DD}=5V, V_{SS}=0V	4.5	-	V
High Level Output Voltage 3 (Noise Immunity), PULSE, COMP I, VCO OUT, 1C1, 2C1, COMP II	V_{OH3}	3006	Input conditions per Note 5 V_{IL}=4V, V_{IH}=11V, I_{OH}=0A V_{DD}=15V, V_{SS}=0V	13.5	-	V

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Low Level Output Current 1, PULSE, COMP I, VCO OUT, 1C1, 2C1, COMP II	I_{OL1}	-	Input conditions per Note 4 V_{IN}(INH and R2)=5V V_{IN}(VCO IN and R1)=0V V_{OL}=0.4V V_{DD}=5V, V_{SS}=0V T_{amb}=+125°C T_{amb}=- 55°C	360 640	- -	µA
Low Level Output Current 2, PULSE, COMP I, VCO OUT, 1C1, 2C1, COMP II	I_{OL2}	-	Input conditions per Note 4 V_{IN}(INH and R2)=15V V_{IN}(VCO IN and R1)=0V V_{OL}=1.5V V_{DD}=15V, V_{SS}=0V Note 7 T_{amb}=+125°C T_{amb}=- 55°C	2.4 4.2	- -	mA
High Level Output Current 1, PULSE, COMP I, VCO OUT, COMP II	I_{OH1}	-	Input conditions per Note 5 V_{IN}(R2)=5V V_{IN}(VCO IN, INH, R1, 1C1 and 2C1)=0V V_{OH}=4.6V V_{DD}=5V, V_{SS}=0V Note 7 T_{amb}=+125°C T_{amb}=- 55°C	-360 -640	- -	µA
High Level Output Current 2, PULSE, COMP I, VCO OUT, COMP II	I_{OH2}	-	Input conditions per Note 5 V_{IN}(R2)=15V V_{IN}(VCO IN, INH, R1, 1C1 and 2C1)=0V V_{OH}=13.5V V_{DD}=15V, V_{SS}=0V Note 7 T_{amb}=+125°C T_{amb}=- 55°C	-2.4 -4.2	- -	mA
Bias Leakage Current 1, V_{SS}	I_{LB1}	-	V_{IN}(COMP and VCO IN)=0V V_{IN}(INH and R2)=15V SIG=Open V_{DD}=15V, V_{SS}=0V	-	-1.5	mA

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Bias Leakage Current 2, SIG	I_{LB2}	-	V_{IN}(SIG, COMP and VCO IN)=0V V_{IN}(INH and R2)=15V V_{DD}=15V, V_{SS}=0V			µA
			Tamb=+125°C	-	-120	
			Tamb=-55°C	-	-240	
Bias Leakage Current 3, SIG	I_{LB3}	-	V_{IN}(SIG, INH and R2)=15V V_{IN}(COMP and VCO IN)=0V V_{DD}=15V, V_{SS}=0V			µA
			Tamb=+125°C	-	120	
			Tamb=-55°C	-	240	
Threshold Voltage N-Channel, DEMOD	V_{THN}	-	V_{IN}(COMP, INH, 1C1, 2C1 and SIG)= V_{SS}=-5V I(DEMOD)=-10µA All Other Inputs: V_{IN}=V_{DD}=Ground			V
			T_{amb}=+125°C	-0.3	-3.5	
			T_{amb}=- 55°C	-0.7	-3.5	
Threshold Voltage P-Channel, R2	V_{THP}	-	V_{DD} at Ground I(R2)=-10µA All Other Inputs: V_{IN}=V_{SS}=-5V			V
			T_{amb}=+125°C	-0.3	-3.5	
			T_{amb}=- 55°C	-0.7	-3.5	
Output Leakage Current Third State, Low Level Applied, COMP II	I_{OZL}	3020	Input conditions per Note 6 V_{IN}(INH and R2)=15V V_{IN}(VCO IN)=0V V_{OL}=0V V_{DD}=15V, V_{SS}=0V			µA
			T_{amb}=+125°C	-	-12	
			T_{amb}=- 55°C	-	-0.4	
Output Leakage Current Third State, High Level Applied, COMP II	I_{OZH}	3021	Input conditions per Note 6 V_{IN}(INH and R2)=15V V_{IN}(VCO IN)=0V V_{OH}=15V V_{DD}=15V, V_{SS}=0V			µA
			T_{amb}=+125°C	-	12	
			T_{amb}=- 55°C	-	0.4	
Zener Voltage	V_Z	-	I_Z=50µA			V
			T_{amb}=+125°C	4.45	7.75	
			T_{amb}=- 55°C	4.45	7.5	

2.3.3 Notes to Electrical Measurement Tables

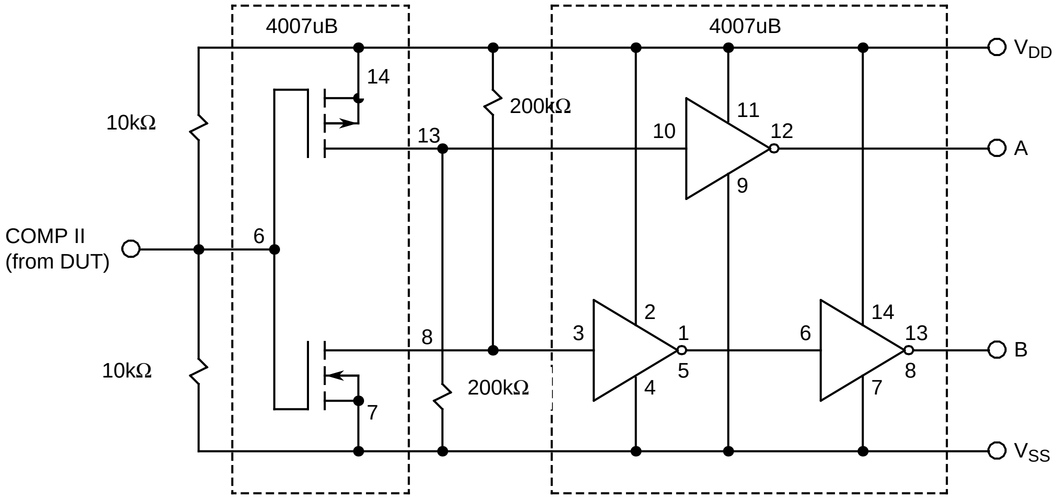
1. Unless otherwise specified all inputs and outputs shall be tested for each characteristic, inputs not under test shall be $V_{IN} = V_{SS}$ or V_{DD} and outputs not under test shall be open.
2. Functional tests shall be performed, GO-NO-GO, per the table below with $V_{OH} \geq V_{DD}$ -0.5V, $V_{OL} \leq 0.5V$. The Maximum time to output comparator strobe = 300µs.

Functional Test	Input Pattern No.	Input Conditions								Outputs	
		PULSE	COMP I	COMP	VCO OUT	INH	1C1	2C1	SIG	A	B
	1	X	0	0	0	1	0	0	0	X	X
	2	X	1	0	0	1	0	0	1	X	X
	3	X	0	0	0	1	0	0	0	X	X
(a)	4	0	1	0	1	0	1	1	1	1	0
(b)	5	0	0	0	0	0	0	1	0	1	0
(c)	6	1	1	1	0	0	0	0	0	0	0
(d)	7	0	0	1	1	0	1	0	1	1	0
(e)	8	0	1	0	1	0	0	0	1	1	0
	9	X	X	0	X	1	0	0	1	X	X
(f)	10	1	0	1	0	1	0	0	1	0	0
(g)	11	1	1	1	0	1	0	1	0	0	0
(h)	12	0	0	1	0	1	1	1	1	1	0
(i)	13	0	1	1	0	1	1	0	0	1	0
(j)	14	0	0	1	0	1	0	0	1	1	0
(k)	15	0	1	1	0	1	0	0	0	1	0
(l)	16	0	0	0	0	1	0	0	0	1	0
(m)	17	0	1	0	0	1	0	0	1	1	0
(n)	18	1	0	1	0	1	0	0	1	0	0
(o)	19	1	1	0	0	1	0	0	1	0	0
(p)	20	0	0	1	0	1	0	0	1	0	1
(q)	21	0	1	0	0	1	0	0	1	0	1
(r)	22	0	0	1	0	1	0	0	1	0	1
(s)	23	0	1	0	0	1	0	0	1	0	1
(t)	24	0	0	0	0	1	0	0	0	0	1
(u)	25	0	1	1	0	1	0	0	0	0	1
(v)	26	0	0	0	0	1	0	0	0	0	1
(w)	27	1	1	0	0	1	0	0	1	0	0
(x)	28	0	0	1	0	1	0	0	1	0	1
(y)	29	0	1	1	0	1	0	0	0	0	1
(z)	30	1	0	1	0	1	0	0	1	0	0
(aa)	31	1	1	0	0	1	0	0	1	0	0
(bb)	32	1	0	0	0	1	0	0	0	0	0
(cc)	33	0	1	1	0	1	0	0	0	0	1

Functional Test	Input Pattern No.	Input Conditions								Outputs	
		PULSE	COMP I	COMP	VCO OUT	INH	1C1	2C1	SIG	A	B
(dd)	34	1	0	1	0	1	0	0	1	0	0
(ee)	35	1	1	1	0	1	0	0	0	0	0
(ff)	36	1	0	0	0	1	0	0	0	0	0
(gg)	37	0	1	0	0	1	0	0	1	1	0

NOTES:

- Logic Level Definitions: 1 = V_{IH} = V_{DD}, 0 = V_{IL} = V_{SS}, X = Irrelevant.
- R2 is always connected to V_{DD}.
- Diagram for the connection of DUT to two 4007UB's for the formation of Outputs A and B:



NOTES:

Unused pins on the first 4007UB to be biased as follows:

- Pins 2 and 11 = V_{DD}.
- Pins 3, 4, 9, 10 = V_{SS}.

For the Low Voltage Functional Test, V_{DD} for external 4007UB's should be made higher to ensure correct operation.

3. Quiescent Current shall be tested at the twelve points shown using the following input conditions with 1 = V_{IH} = V_{DD} and 0 = V_{IL} = V_{SS}.
Tests (a) to (f) measure I_{DD} (positive leakage limits), with V_{SS} at Ground. Tests (g) to (l) measure I_{SS} (negative leakage limits), with V_{DD} = 15V.

Input Pattern No.	Input Conditions								I_{DD}, I_{SS} Test
	COMP	INH	1C1	2C1	VCO IN	R1	R2	SIG	
1	1	1	0	0	0	0	0	0	
2	1	1	0	0	0	0	0	1	

Input Pattern No.	Input Conditions								I_{DD}, I_{SS} Test
	COMP	INH	1C1	2C1	VCO IN	R1	R2	SIG	
3	1	1	0	0	0	0	0	0	
4	1	1	0	0	0	0	0	1	(a)
5	0	0	1	0	0	0	1	1	
6	0	0	0	0	0	0	1	1	(b)
7	1	0	0	1	0	0	1	1	
8	1	0	0	0	0	0	1	1	(c)
9	0	0	0	0	0	0	1	1	(d)
10	1	0	0	0	0	0	1	1	(e)
11	0	0	0	0	0	0	1	1	(f)
12	1	1	OPEN	OPEN	0	0	1	0	
13	1	1	OPEN	OPEN	0	0	1	1	
14	1	1	OPEN	OPEN	0	0	1	0	
15	1	1	OPEN	OPEN	0	0	1	1	
16	1	1	OPEN	OPEN	0	0	1	0	(g)
17	0	1	OPEN	OPEN	0	0	1	0	(h)
18	1	1	OPEN	OPEN	0	0	1	0	(i)
19	0	1	OPEN	OPEN	0	0	1	0	(j)
20	1	1	OPEN	OPEN	0	0	1	0	(k)
21	0	1	OPEN	OPEN	0	0	1	0	(l)

4. Test each designated output at the point shown using the following input conditions with 1 = V_{IH} = V_{DD} and 0 = V_{IL} = V_{SS}:

Test	Input Pattern No.	Input Conditions		
		COMP	1C1	SIG
	1	0	OPEN	1
	2	1	OPEN	1
	3	0	OPEN	1
(a)	4	1	OPEN	1

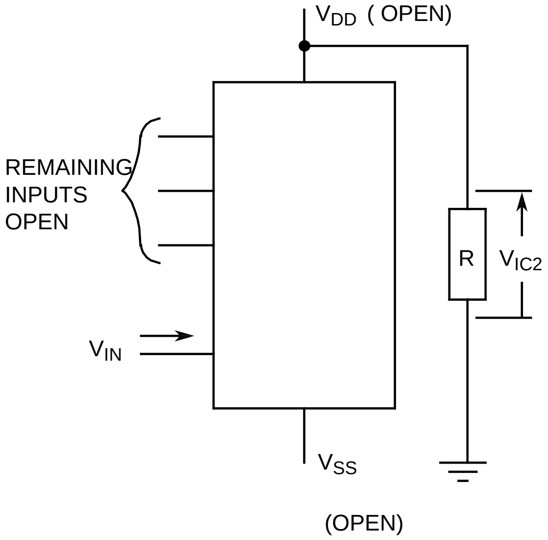
5. Test outputs COMP I, VCO OUT and COMP II at point (a) and output PULSE at point (b) using the following input conditions with 1 = V_{IH} = V_{DD} and 0 = V_{IL} = V_{SS}:

Test	Input Pattern No.	Input Conditions		
		COMP	1C1	SIG
	1	0	OPEN	1
	2	1	OPEN	1
	3	0	OPEN	1
	4	1	OPEN	1
	5	1	OPEN	1
	6	1	0	0
	7	1	1	1
	8	1	0	0
	9	1	0	1
(a)	10	1	0	0
	11	0	0	0
(b)	12	1	0	0

6. Output leakage Current Third State, Low Level Applied and Output Leakage Current Third State, High Level Applied shall be tested using the following input conditions with 1 = V_{IH} = V_{DD} and 0 = V_{IL} =V_{SS}:

Test	Input Pattern No.	Input Conditions	
		COMP	SIG
	1	0	0
	2	1	0
	3	0	0
	4	1	0
(a)	5	0	1

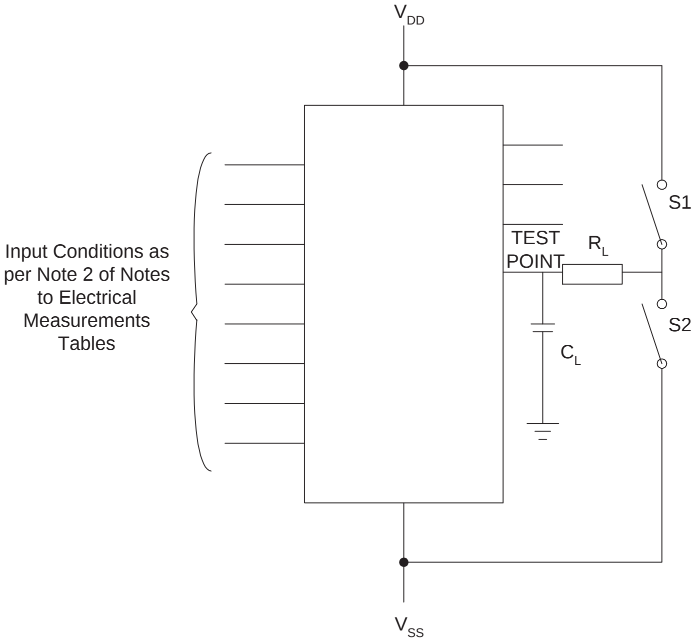
7. Interchange of forcing and measuring parameters is permitted.
8. Input Clamp Voltage 2 (to V_{DD}), V_{IC2}, shall be tested on each input as follows:-



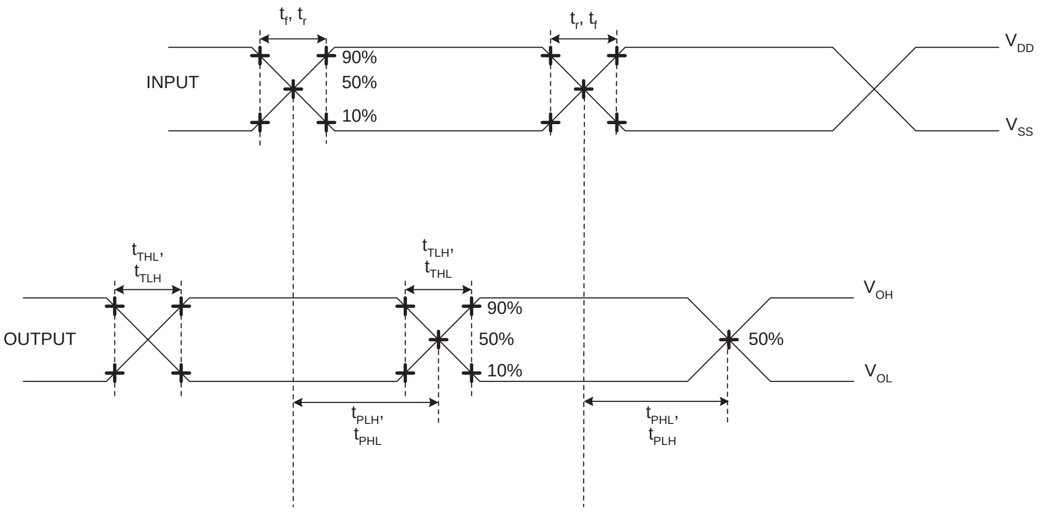
9. Guaranteed but not tested.
10. Read and record measurements shall be performed on a sample of 32 components with 0 failures permitted.
    The pulse generator shall have the following characteristics:

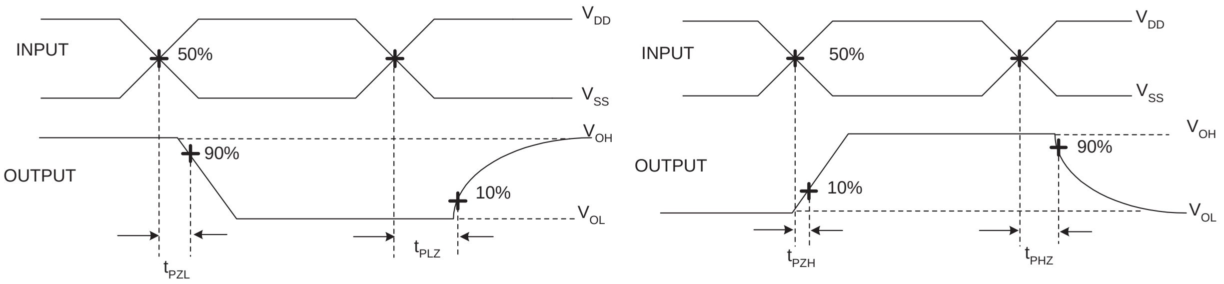
    V_{GEN} = 0 to V_{DD}; f = 500kHz; t_r and t_f ≤20 ns (10% to 90%); duty cycle = 50%. Output load capacitance C_L = 50pF ±5% including scope probe, wiring and stray capacitance without component in the test fixture.

    Propagation delay and transition time shall be measured as follows:



Parameter	R_L	S1	S2
t_{PZH}	1kΩ	Open	Closed
t_{PZL}		Closed	Open
t_{PHZ}		Open	Closed
t_{PLZ}		Closed	Open
t_{PHL}, t_{PLH}, t_{THL}, t_{TLH}	200kΩ	Open	Closed





11. Read and record measurements shall be performed on a sample of 32 components with 0 failures permitted.

2.4 PARAMETER DRIFT VALUES

Unless otherwise specified, the measurements shall be performed at T_{amb}=+22 ±3°C.

The test methods and test conditions shall be as per the corresponding test defined in Room Temperature Electrical Measurements.

The drift values (Δ) shall not be exceeded for each characteristic specified. The corresponding absolute limit values for each characteristic shall not be exceeded.

Characteristics	Symbols	Limits			Units
		Drift Value Δ	Absolute		
			Min	Max	
Quiescent Current	I_{DD}, I_{SS}	±12	-	±80	µA
Low Level Output Current 1	I_{OL1}	±15% (2)	510	-	µA
High Level Output Current 1	I_{OH1}	±15% (2)	-510	-	µA
Output Leakage Current Third State, Low Level Applied	I_{OZL}	±60	-	-400	nA
Output Leakage Current Third State, High Level Applied	I_{OZH}	±60	-	400	nA
Threshold Voltage N-Channel	V_{THN}	±0.3	-0.7	-3	V
Threshold Voltage P-Channel	V_{THP}	±0.3	-0.7	-3	V

NOTES:

1. Unless otherwise specified all inputs and outputs shall be tested for each characteristic.
2. Percentage of limit value if voltage is the measuring parameter.

2.5 INTERMEDIATE AND END-POINT ELECTRICAL MEASUREMENTS

Unless otherwise specified, the measurements shall be performed at T_{amb}=+22 ±3^{o}C.

The test methods and test conditions shall be as per the corresponding test defined in Room Temperature Electrical Measurements .

The drift values (Δ) shall not be exceeded for each characteristic where specified. The corresponding absolute limit values for each characteristic shall not be exceeded.

Characteristics	Symbols	Limits			Units
		Drift Value Δ	Absolute		
			Min	Max	
Functional Test 1	-	-	-	-	-
Quiescent Current	I_{DD}, I_{SS}	±12	-	±80	µA
Low Level Input Current	I_{IL}	-	-	-100	nA
High Level Input Current	I_{IH}	-	-	100	nA
Low Level Output Voltage 1	V_{OL1}	-	-	50	mV
Low Level Output Voltage 2 (Noise Immunity)	V_{OL2}	-	-	500	mV
High Level Output Voltage 1	V_{OH1}	-	14.95	-	V
High Level Output Voltage 2 (Noise Immunity)	V_{OH2}	-	4.5	-	V
Low Level Output Current 1	I_{OL1}	±15% (3)	510	-	µA
Low Level Output Current 2	I_{OL2}	±15% (3)	3.4	-	mA
High Level Output Current 1	I_{OH1}	±15% (3)	-510	-	µA
High Level Output Current 2	I_{OH2}	±15% (3)	-3.4	-	mA
Output Leakage Current Third State, Low Level Applied	I_{OZL}	±60	-	-400	nA
Output Leakage Current Third State, High Level Applied	I_{OZH}	±60	-	400	nA
Bias Leakage Current 1	I_{LB1}	–	-	-1.5	mA
Bias Leakage Current 2	I_{LB2}	–	-	-150	µA
Bias Leakage Current 3	I_{LB3}	–	-	150	µA
Threshold Voltage N-Channel	V_{THN}	±0.3	-0.7	-3	V
Threshold Voltage P-Channel	V_{THP}	±0.3	-0.7	-3	V
Zener Voltage	V_Z	–	4.45	7.5	V

NOTES:

1. Unless otherwise specified all inputs and outputs shall be tested for each characteristic.
2. The drift values (Δ) are applicable to the Operating Life test only.
3. Percentage of limit value if voltage is the measuring parameter.

2.6 HIGH TEMPERATURE REVERSE BIAS BURN-IN CONDITIONS

2.6.1 N-Channel HTRB

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	T_{amb}	+125 (+0 -5)	^{o}C
Outputs PULSE, COMP I, VCO OUT, 1C1, 2C1, DEMOD, COMP II, ZEN	V_{OUT}	Open	V
Inputs COMP, INH, VCO IN, R1, R2, SIG	V_{IN}	V_{SS}	V
Positive Supply Voltage	V_{DD}	15 (+0 -0.5)	V
Negative Supply Voltage	V_{SS}	0	V
Duration	t	72	Hours

NOTES:

1. Input Protection Resistor = 2kΩ min to 47kΩ max.

2.6.2 P-Channel HTRB

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	T_{amb}	+125 (+0 -5)	^{o}C
Outputs PULSE, COMP I, VCO OUT, 1C1, 2C1, DEMOD, COMP II, ZEN	V_{OUT}	Open	V
Inputs R1, R2	V_{IN}	V_{SS}	V
Inputs COMP, INH, VCO IN, SIG	V_{IN}	V_{DD}	V
Positive Supply Voltage	V_{DD}	15 (+0 -0.5)	V
Negative Supply Voltage	V_{SS}	0	V
Duration	t	72	Hours

NOTES:

1. Input Protection Resistor = 2kΩ min to 47kΩ max.

2.7 POWER BURN-IN CONDITIONS

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	T_{amb}	+125 (+0 -5)	^{o}C
Outputs PULSE, VCO OUT, DEMOD, COMP II, ZEN	V_{OUT}	$V_{DD}/2$	V
Output COMP I	V_{OUT}	6.25	V
Inputs R1, 1C1, 2C1	V_{IN}	Open	V
Inputs COMP, INH, R2	V_{IN}	V_{DD}	V
Input VCO IN	V_{IN}	V_{SS}	V
Input SIG	V_{IN}	V_{GEN}	V
Pulse Voltage	V_{GEN}	0V to V_{DD}	V
Pulse Frequency Square Wave	f_{GEN}	50k 50% Duty Cycle	Hz
Positive Supply Voltage	V_{DD}	15 (+0 -0.5)	V
Negative Supply Voltage	V_{SS}	0	V

NOTES:

1. Input Protection Resistor = Output Load = 2kΩ min to 47kΩ max.

2.8 OPERATING LIFE CONDITIONS

The conditions shall be as specified for Power Burn-in.

APPENDIX ‘A’

AGREED DEVIATIONS FOR STMICROELECTRONICS (F)

ITEMS AFFECTED	DESCRIPTION OF DEVIATIONS
Deviations from Screening Tests - Chart F3	External Visual Inspection: The criteria applicable to chip outs are those described in MIL-STD-883, Test Method 2009, Paras 3.3.6(b) and 3.3.7(a). High Temperature Reverse Bias Burn-in: The temperature limits of MIL-STD-883, Para. 4.5.8(c) may be used. Power Burn-in test is performed using STMicroelectronics Specification Ref: 0019255.
Deviations from Qualification and Periodic Tests - Chart F4	External Visual Inspection: The criteria applicable to chip outs are those described in MIL-STD-883, Test Method 2009, Paras 3.3.6(b) and 3.3.7(a). Operating Life: The temperature limits of MIL-STD-883, Para. 4.5.8(c) may be used.
Deviations from High and Low Temperatures Electrical Measurements	High and Low Temperatures Electrical Measurements may be considered guaranteed but not tested if successful pilot lot testing has been performed on the wafer lot which includes High and Low Temperatures Electrical Measurements per the Detail Specification. A summary of the pilot lot testing shall be provided if required by the Purchase Order.
Deviations from Room Temperature Electrical Measurements	All AC characteristics (Capacitance and Timings) may be considered guaranteed but not tested if successful pilot lot testing has been performed on the wafer lot which includes AC characteristic measurements per the Detail Specification. A summary of the pilot lot testing shall be provided if required by the Purchase Order.